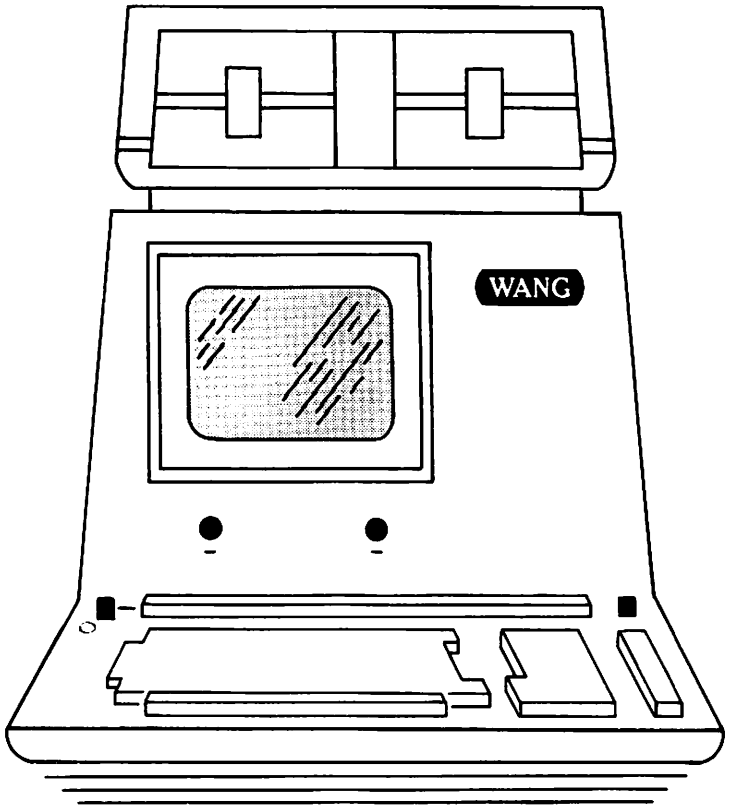
IV.A.2

VIDEO TRAINING WORKBOOK



PCS II/PCS IIA

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PCS II/PCS IIA

VIDEO TRAINING WORKBOOK

WANG LABORATORIES, INC
ONE INDUSTRIAL AVENUE LOWELL MASSACHUSETTS 01851 TEL (617) 459-5000, TWX 710 343-6769, TELEX 94-7421

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   SD D A SA

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   SD D A SA

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6. The Course provided the Basic Knowledge and Skills required for my work.
   SD D A SA

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* (If a correction is indicated above please include effected page numbers along with the necessary correction.)

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PREFACE

This workbook has been published as a training aid to be used with the viewing of the Wang Laboratories video program for the 2200 PCS II and PCS IIA personal computers. Support information for the video presentation as well as other pertinent reference material is contained in this book.

ACKNOWLEDGEMENTS

This VIDEO/WORKBOOK training program has been developed by the CURRICULUM DEVELOPMENT GROUP (Curriculum Maintenance) with assistance from the MEDIA SUPPORT GROUP, at the Customer Engineering Technical Training Center in Lawrence, Massachusetts.

Special appreciation is extended to the Instructors and Lab Technicians of the Customer Engineering 2200 Instructional Group who provided the technical support for development of this program.

CURRICULUM DEVELOPMENT GROUP

CURRICULUM DEVELOPMENT SPECIALIST: William L. Giglio
CURRICULUM DEVELOPMENT SUPERVISOR: Michael Durcan

COURSE OBJECTIVES

The contents of this workbook and the videotape presentation are presented in a convenient, compact and practical training package. The primary objective of this program is to provide Customer Engineering personnel with the practical knowledge required to operate, install and troubleshoot the PCS II and PCS IIA mini computers.

After completion of this comprehensive field level training program, the trainee will be able to identify the major components, understand the general theory of operation, perform field level maintenance, perform field level adjustments, and conduct diagnostic evaluations on these computers.

It is recommended that the 2200 MAINTENANCE MANUAL, the FIELD LEVEL MAINTENANCE GUIDE #2, and WANG SERVICE BULLETIN 75 A&B be available while viewing the presentation. These publications should answer any questions that are beyond the scope of this training program.

WORKBOOK STRUCTURE

PART 1 expands on the material presented in the video presentation with more detailed text, pictures and diagrams.

PART 2 contains laboratory exercises which will enhance the understanding of the material in Part 1.

PART 3 contains a comprehensive self-administered quiz applicable to all the material covered in the video presentation and the workbook. There are referrals to page(s) of the workbook where the correct answers to the questions may be found. The trainee should review the video presentation and/or the workbook whenever a question is answered incorrectly.

TABLE OF CONTENTS

REFERENCE MATERIAL

(TEXT OF VIDEO PRESENTATION)

PART 1

INTRODUCTION TO THE PCS II

The PCS II is marketed as a 2200 series portable personal computing system. It is a self contained unit with a CPU, a keyboard, a 9 inch video display and dual mini diskette drives. The unit is intended to be a "stand alone" single user computer with provisions for two output writing peripherals. There is also a PCS IIA model available with provisions for one output writer and one disk drive.

RAM may be expanded from the basic 8K up to 32K in 8K increments. The unit supports various printers and plotters. You should consult the latest Wang publications to determine which printers and plotters are compatible with the PCS II and PCS IIA personal computers.

DUAL MINI-DISKETTE DRIVES

The dual mini diskette drives accept the Wang #177-0064 single sided, single density 5 inch diskettes. A format button is installed on the front panel of the drive unit base. However, only the left drive can be used for formatting.

After inserting a diskette in the left drive, depress the format button for three (3) seconds. The red light on the left drive should illuminate for a short time and then disappear. A blinking red light indicates that formatting has not occurred.

For Wang product line compatability, the left drive, with an address of 310, is called the fixed drive and the right drive, with an address of B10, is called the removable drive.

TERMINAL COVER REMOVAL

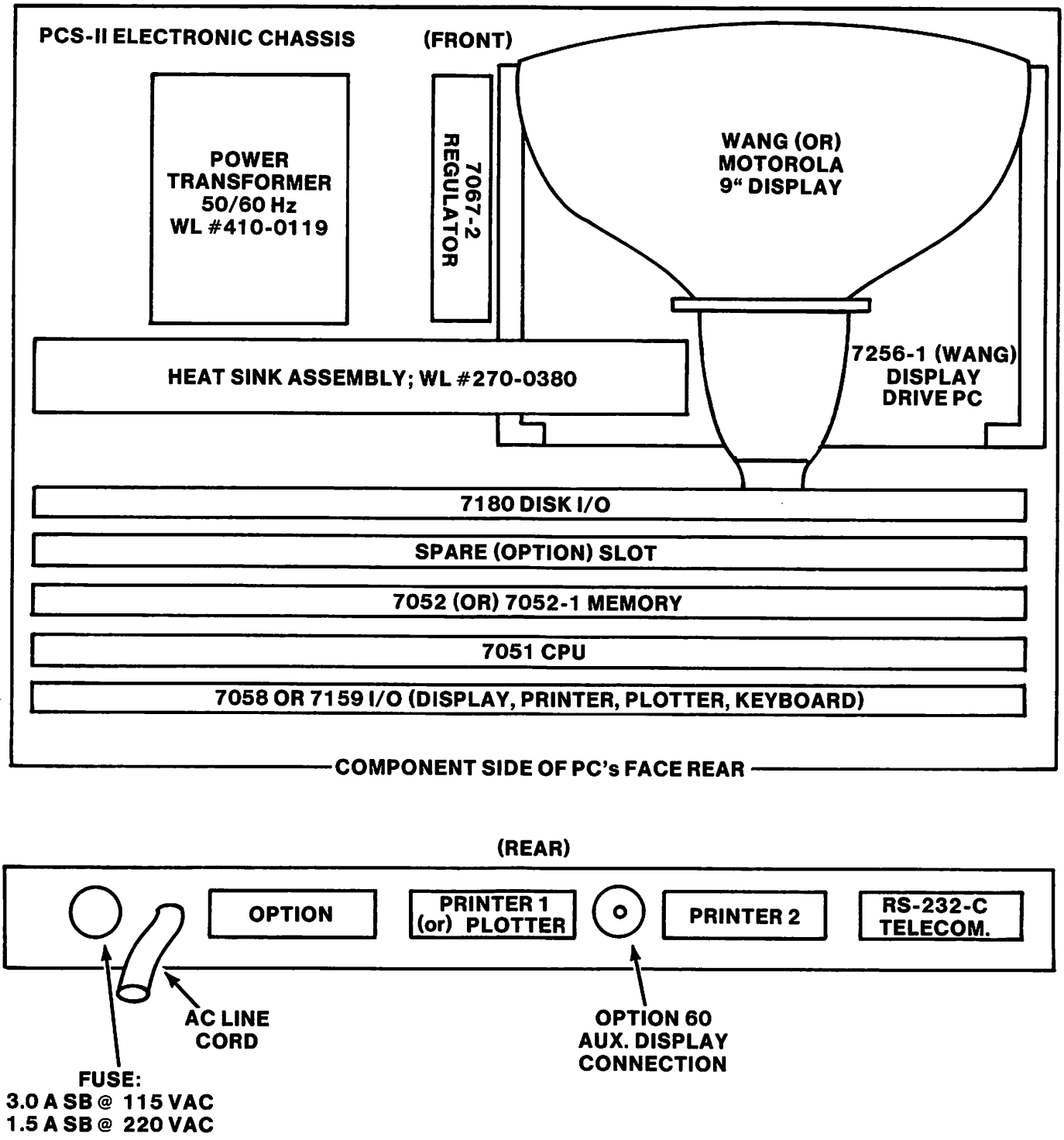
First, ensure that the power is turned off and the fan has stopped to prevent breaking the fan blades.

Remove the screw in the rear of the minidisk cover and lift up the cover. Remove the flat ribbon cables and the power cables from the rear of each drive. If there is a plug to the format switch, disconnect it. If there is no plug, unsolder the wires from the format switch. Remove the ground lug wire from the rear of either the left or right drive unit.

> CAUTION
> Ensure that the ground wire is prevented from falling into the unit as the wire may touch the heat sink causing a short to ground.

Remove the screws on the sides of the terminal cover. Loosen the two finger nuts on the keyboard assembly and remove the special function strip. Remove the two screws found under the function strip. Using the finger nuts, lift the keyboard cover off. Now, lift the terminal cover up slightly (with the diskette drives in place) to allow the removal of the contrast and brightness knob cable from the chassis. At this time, you may tilt the cover to the right and disconnect the fan power and ground cables.

Remove the terminal cover and drive assembly. All procedures are reversed for reassembly. After reassembly, ensure that the fan is actually operating by feeling the stream of ventilation air leaving the chassis. If the fan is not operating, excessive heat will eventually ruin any diskettes that are inserted in the drives as well as cause other problems.



CHASSIS LAYOUT

FIGURE 1

PCS II CHASSIS LAYOUT

(REFER TO FIGURE 1)

The PCS II boards are packaged similar to the 2200E personal computer and the 2200F work station terminal. The printed circuit board technology is basically the same as the 2200 A,B,C,S, or T CPU's. However, the hardware has been repackaged from the original ten (10) or more boards and layed out on several larger boards.

At the rear of the workstation is the I/O controller board. This is a 7058 board for a 64 by 16 character screen or a 7159 board for a 80 by 24 character screen. The first printer or plotter, the keyboard, and the CRT device addresses are hardwired from this board. However, there is a rocker type switch for a second printer or plotter device address.

Next in line from the controller board is the 7051 CPU board which, as explained earlier, is similar in theory to the A, B, C, S and T CPU's.

Forward of the CPU board is the RAM and ROM board. A 7052 board is installed for 8K or 16K of RAM. A 7052-1 board is installed for 24K or 32K. This board also contains the master system clock of 10 megacycles.

A slot just forward of the RAM board slot is available for any option boards. After this option slot, there is the 7180 mini disk controller board. This board must be carefully inserted or removed as the neck of the CRT goes through a portion of the board. The cables for the disk drives and the format switch are on this board.

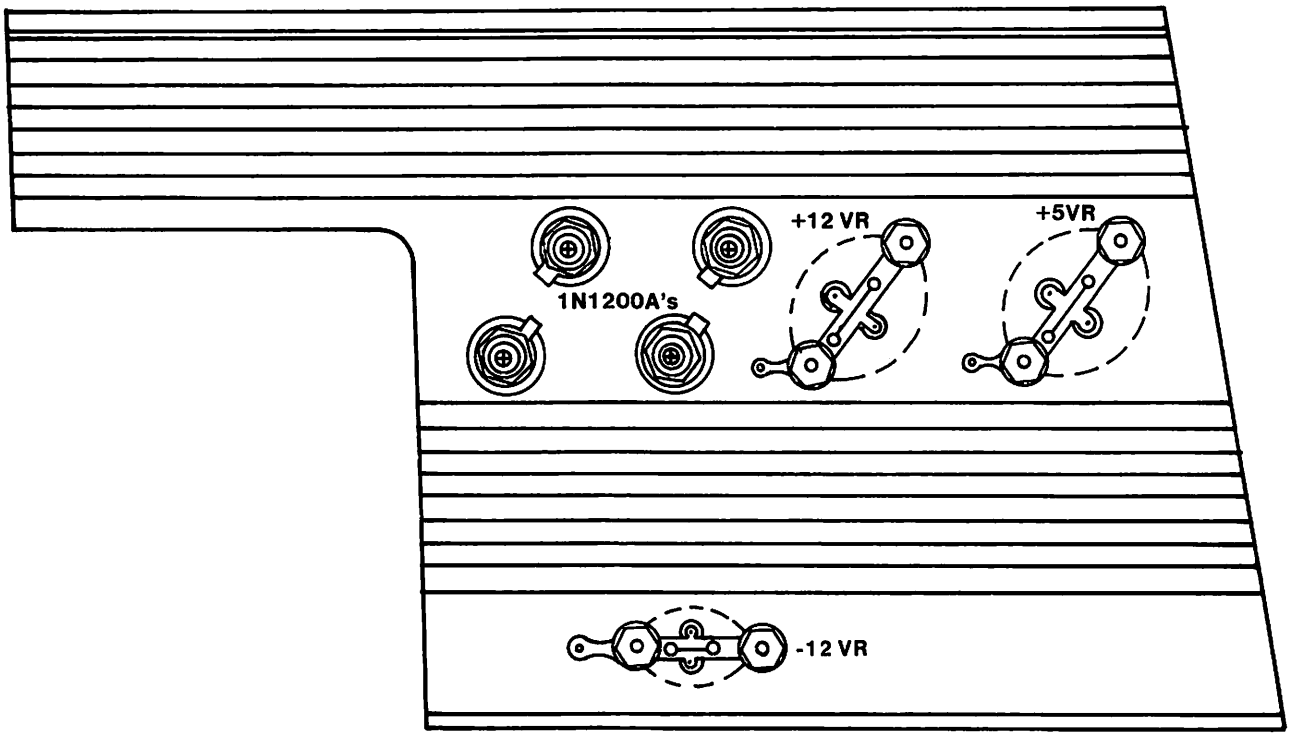
To the right of the CRT screen is the 7067-2 regulator board. This board produces regulated +5, -5, +12, and -12 volts and unregulated +18 and -18 volts.

A 115/230 AC input voltage selector switch is located just behind the 7067-2 regulator board.

The heat sink board, which is also behind the regulator board, contains the driver transistors for the 5 and 12 volt outputs.

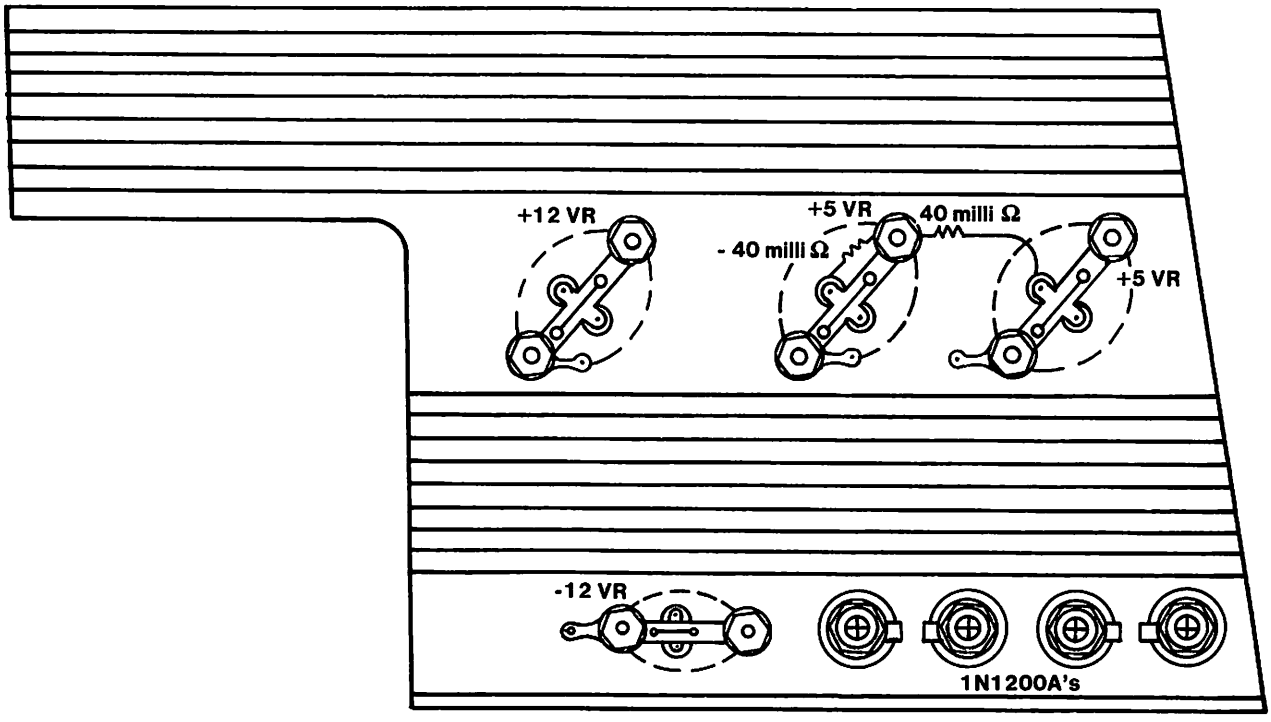
Heat sink boards of early manufacture had only one +5 volt pass transistor. These are easily identified because they have only three large power transistors installed. Later heat sink boards have an additional +5 volt transistor (REFER TO FIGURES 2A and 2B). This additional transistor was added because the single +5 volt transistor became very hot under normal use.

The unit should only be operated with the terminal cover in place since airflow is not supplied over the heat sink if the cover is removed (the fan is mounted on the cover). This precaution prevents excessive heat from building up around the heat sink and avoids the danger of severe burns to personnel and damage to the unit.



PCS II EARLIER VERSION HEAT SINK ASSEMBLY

FIGURE 2A



PCS II LATER VERSION HEAT SINK ASSEMBLY

FIGURE 2B

DATA FLOW
PCS II, IIA SYSTEM

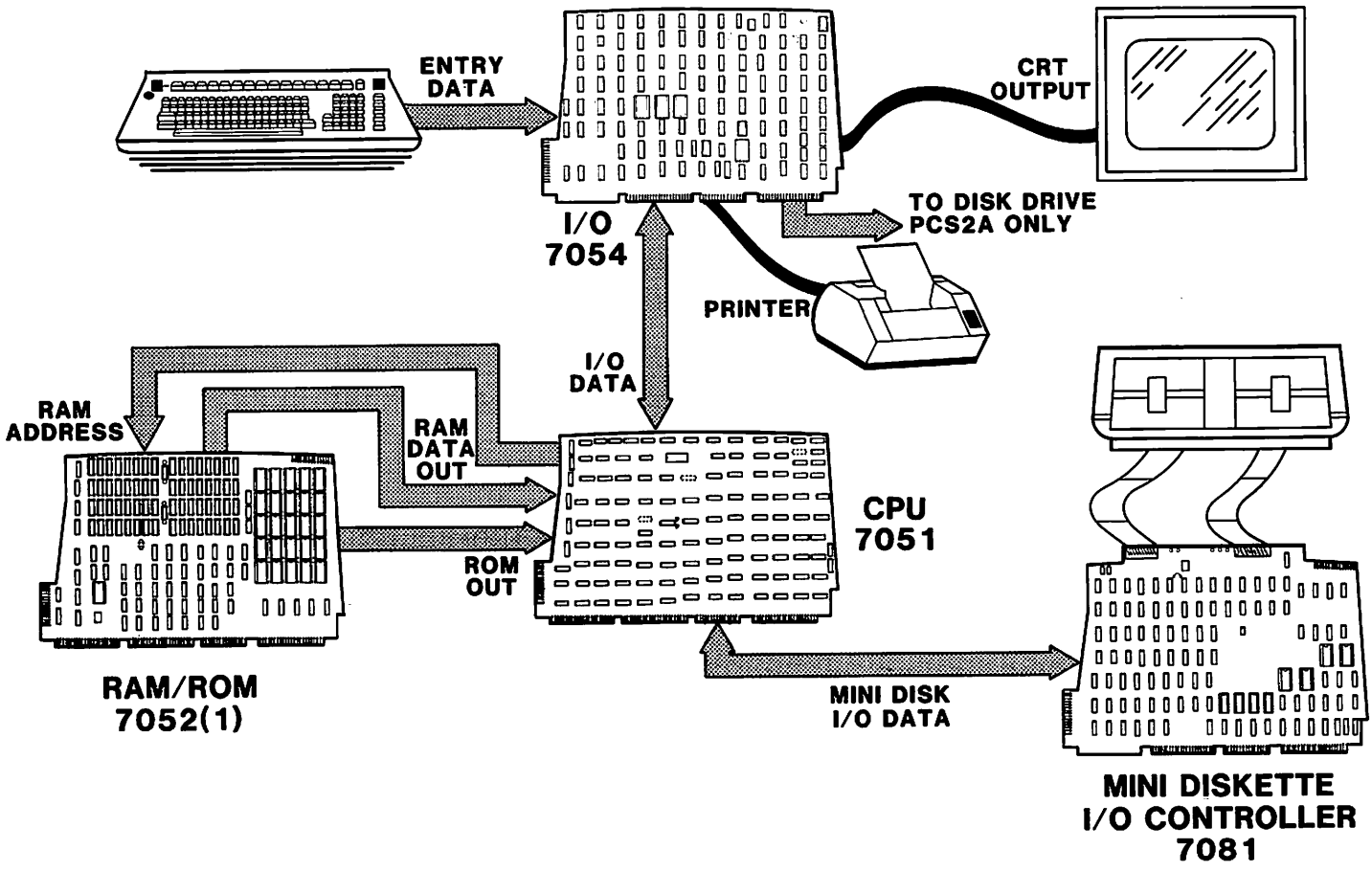


FIGURE 3

DATA FLOW DESCRIPTION

(REFER TO FIGURE 3)

FIGURE 3 is a simplified Data Flow diagram of the PCS II & IIA. A detailed block diagram and description of these units is found at the end of this section, beginning with page 1-30.

The Keyboard enters data into the Input Output Controller Board which in turn routes data to the CPU board. The CPU board will address the appropriate RAM portion of the RAM/ROM board which in turn sends data back to the CPU board. The ROM output is fed from the ROM portion of the RAM/ROM board as Control Memory instructions to the CPU.

The CPU board sends data back to the I/O board where it may be routed to a printer, a CRT, or in the case of the PCS 2A, a hard disk drive.

The CPU board may also send or receive data from the minidiskette controller I/O board. This I/O board sends data TO or receives data FROM the left or right mini diskette drives.

SETTING THE PRINTER ADDRESS ON THE PCS II

PCB 7058 is the standard I/O board installed on the PCS II. The first printer or plotter is hardwired to 215, the keyboard is hardwired to address 001, and the CRT is hardwired to address 005. The board contains an 8 bank switch which is used to provide an address for a second printer or plotter (REFER TO FIGURE 4A).

The first two digits of the hex address for this second printer or plotter are hardwired to 2 and 1 (21). The switch is positioned to complete the hex address. For example, select position number 6 to complete hex address 216. Exceptions are Hex addresses 215 and 218 which cannot be selected because positions 5 and 8 are not wired to the board.

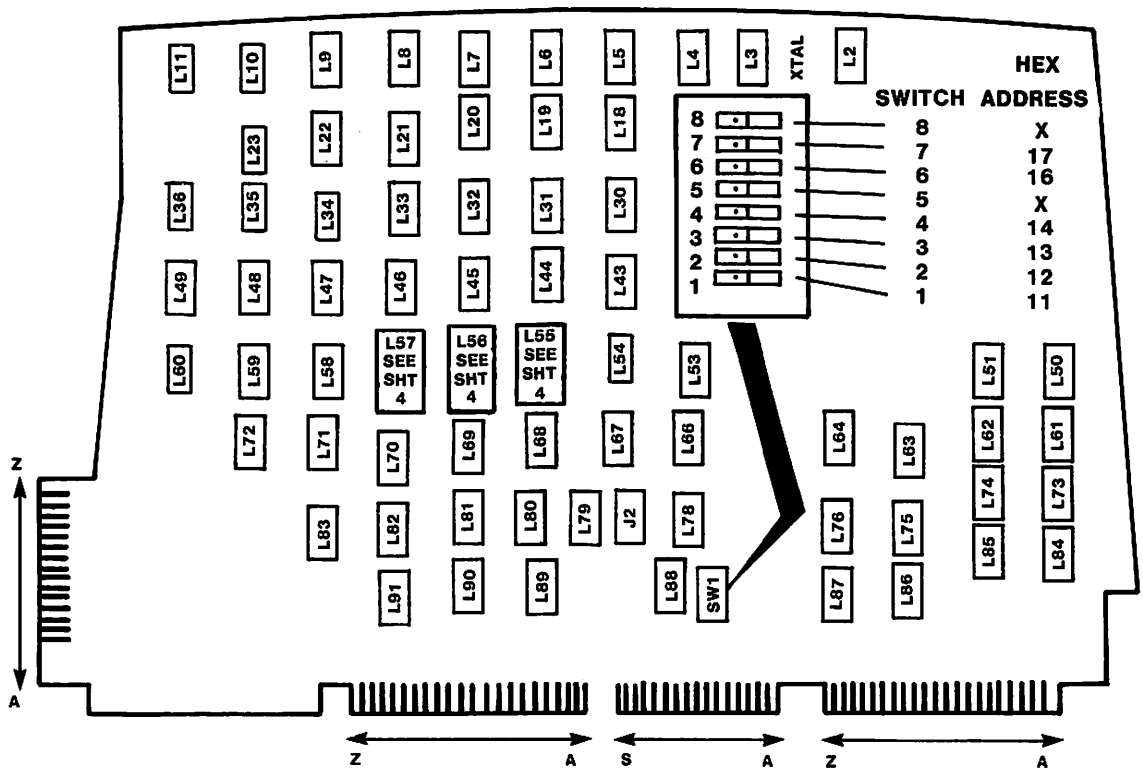
The mini diskette drive addresses are hardwired on the 7180 diskette controller board. Address 310 is for the left drive and B10 is for the right side.

SETTING ADDRESSES ON THE PCS IIA

The PCS IIA has either a 7054 (64x16 CRT) or a 7059 (80 x24 CRT) I/O board installed. These boards allow the PCS IIA to output to a disk drive. Two address switches are mounted on the bottom of their component side. Switch one is used to set the printer address while switch two sets the disk address. Addresses 001 and 005 are hardwired to the Keyboard and CRT respectively (REFER TO FIGURE 4B).

Be aware that numbering of the individual positions on the two switches are reversed from each other. Switch 1 has position 1 on the top while switch 2 has position 1 on the bottom.

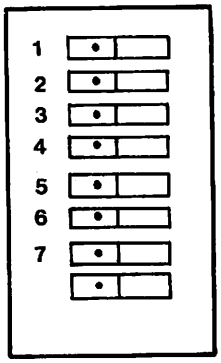
Switch number 1, which is the left switch on the bottom of the component side of the board, is used to set the printer address. Similar to the PCS II, the first two digits of the hex address for the printer are hardwired to 2 and 1 (21). The switch is positioned to complete the hex address.



DEVICE SWITCH ON THE 7058 I/O BOARD

FIGURE 4A

AS SEEN ON 7054 PC (COMPONENT SIDE)

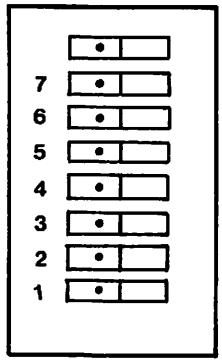


SWITCH	ADDRESS
1	11
2	12
3	13
4	14
5	15
6	16
7	17
X	X

SWITCH #1 (LEFT SIDE)

NOTE: IN GENERAL HEX XY$_1$ Y$_2$ FORMAT
Y$_1$ = HARDWIRED
Y$_2$ = SWITCH SELECTABLE

AS SEEN ON 7054 PC (COMPONENT SIDE)



SWITCH	HEX ADDRESS
8	X
7	40
6	70
5	30
4	60
3	20
2	50
1	10

SWITCH #2 (RIGHT SIDE)

NOTE: IN GENERAL HEX XY$_1$ Y$_2$ FORMAT:
Y$_1$ = SWITCH SELECTABLE
Y$_2$ = 0

DEVICE SWITCHES ON THE 7054/7059 I/O BOARD (NOT SHOWN)

FIGURE 4B

Position number 1 results in hex address 211 and onwards to position number 7 which results in hex address 217. Hex address 218 cannot be selected as positon 8 is not wired to the board.

Switch number 2, which is to the right of switch number 1, sets the disk address. Position 1 selects disk address 310, position 2 for address 350, position 3 for address 320, position 4 for address 360, position 5 for address 330, position 6 for address 370, and position 7 for address 340. Position 8 is not wired to the board. If two addresses are required, BOTH selections must be ON.

The disk drive address feature of the PCS IIA terminal allows the PCS IIA to be used as part of a multiple disk workstation system.

RAM LOADING OF THE 7052(A&B) or 7052-1(A&B) BOARDS

Data memory is expandable in 8K byte increments upwards to a total of 32K bytes by inserting additional RAM chips on the 7052 A and B or 7052-1A and 1B RAM boards (REFER TO FIGURE 5).

There are two rows of chip locations on the 7052 A and B boards and four rows on the 7052-1A and 1B boards. On the 7052-A Board, row 1 is loaded for 8K. On the 7052-B board, rows 1 and 2 are loaded for 16K. On the 7052-1A board, 1,2, and 3 are loaded for 24K. On the 7052-1B board, all four rows are loaded for 32K. The number after the dash (-) on the serial tag indicates the amount of RAM that is available from the RAM board installed on a particular unit (REFER TO FIGURE 6).

RAM SIZE SELECTION

Ram size selection is similar to the method used in previous 2200E and 2200F units in that two solder jumpers are used on the 7051 CPU board (near chip L60) for the four RAM size variations available. For 8K, leave out both jumpers. For 16K, install jumper number one. For 24K, install jumper number two. For 32K, install both jumpers (REFER TO FIGURE 7).

To Go From	To	Kit WL #200-	Remove	Add	Jumper Per Fig. 2-8	FROM PCS-II-	TO PCS-II-
8K	16K	EF08-16	———	——— ; L47-54, L56-63	Install 1	-2XY*	-4XY
8K	24K	EF08-24	7052-A	7052-1-A	Install 2	-2XY	-6XY
8K	32K	EF08-32	7052-A	7052-1-B	Add 1 & 2	-2XY	-8XY
16K	24K	EF16-24	7052-B	7052-1-A	Add 2 Remove 1	-4XY	-6XY
16K	32K	EF16-32	7052-B	7052-1-B	Add 2	-4XY	-6XY
24K	32K	EF24-32	———	——— ; L16-13, L15-22	Add 1	-6XY	-8XY

RAM Part No. = 377-0314; Quantity = 16 for each 8K

*where X = A number:

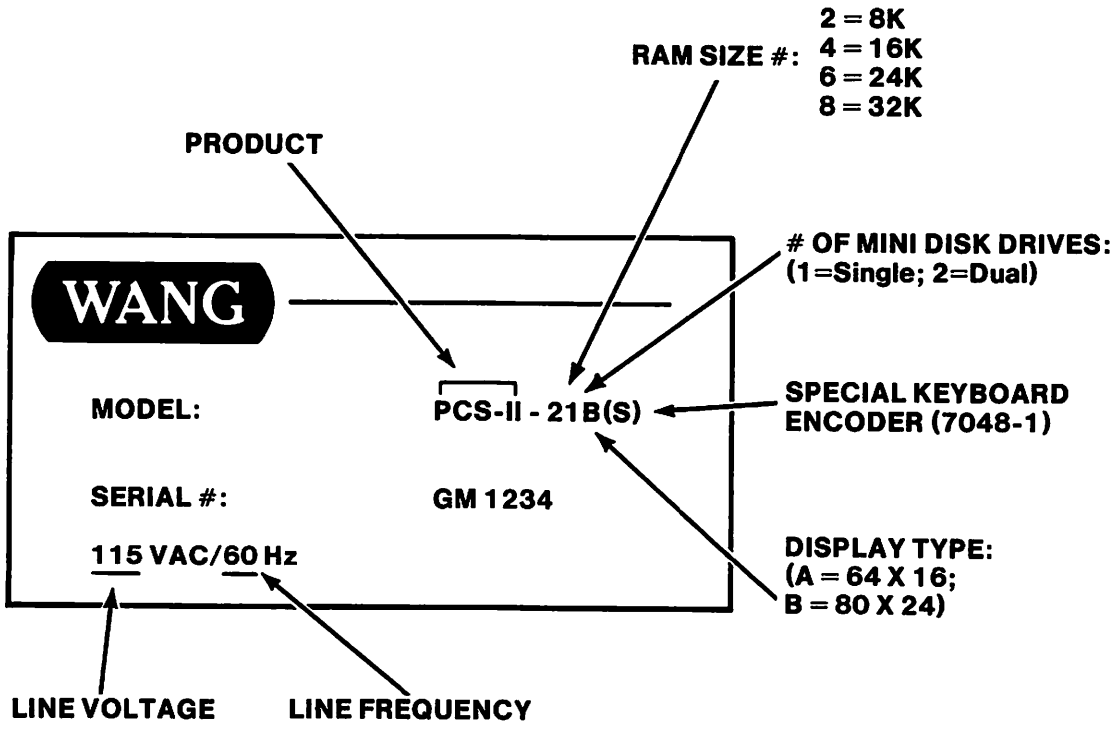
1 = Single Mini
2 = Dual Mini

and Y = A letter:

'A' = 64 X 16 Display
'B' = 80 X 24 Display

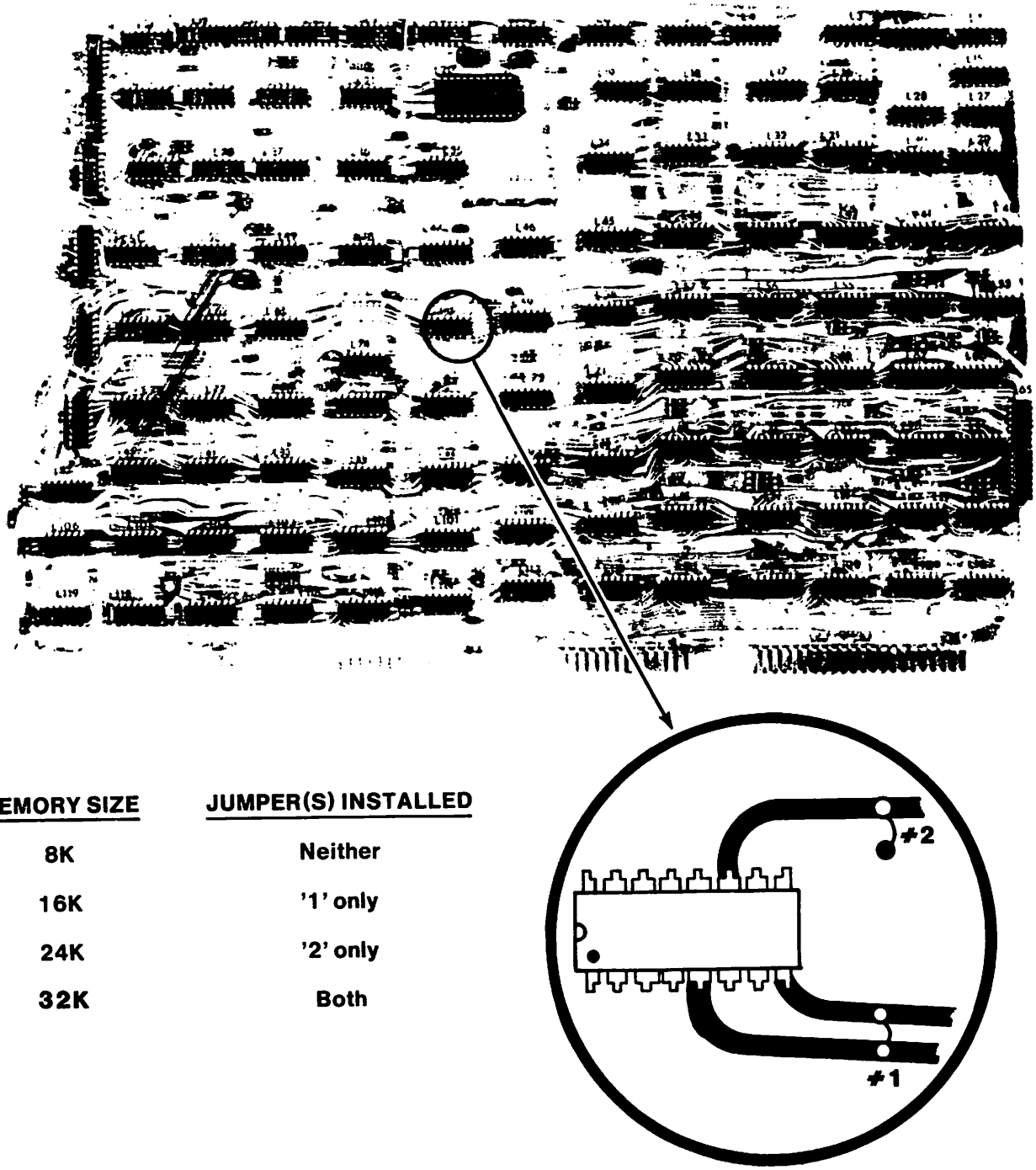
RAM UPGRADE TABLE

FIGURE 5



PCS II SERIAL TAG

FIGURE 6



MEMORY SIZE	JUMPER(S) INSTALLED
8K	Neither
16K	'1' only
24K	'2' only
32K	Both

RAM SIZE SELECTION
FIGURE 7

DIAGNOSTICS

The diagnostics for the PCS II and PCS IIA can be divided into three categories: CPU, Memory, and Peripherals.

The Memory diagnostics test the ability of the memory section to store, access, and transfer information. The memory diagnostic test prompts will ask the user to enter the RAM size configuration. The available free space of RAM, which is the RAM size jumper setting on the CPU board minus the housekeeping bytes, is displayed on the screen after the operator keys in END and RETURN.

Entering the END statement displays the RAM size SET BY THE JUMPERS. The display response is NOT an indication as to how much actual RAM is actually available from the 7052(1) board installed.

The operator may enter PRINT 2+2 and RETURN to verify if the RAM board is loaded adequately for the jumper settings. If the number 4 is presented on the screen, the RAM board installed will provide the RAM size selected by the jumpers. This is also a good indication that the chips that control the Math operations are functioning properly.

If a group of question marks or irrelevant figures are present on the screen after the PRINT 2+2 statement is entered, either the RAM board loading does not match the RAM size set by the jumpers or the RAM chips that provide the Math operations are not functioning properly.

DIAGNOSTIC DISKETTE #701-8000

Diagnostic diskette number 701-8000 can test the CPU hardware, memory, the CRT displays, and the mini diskette drives.

Insert the diskette into either drive. Depress CLEAR and EXECUTE to clear the system. Enter LOAD DCF "START" if using the left drive or LOAD DCR "START" if using the right drive. After a slight pause, key in RUN and EXECUTE. The screen will prompt the operator to key in the drive being utilized. Address 310 is the left drive requiring an entry of 1. Address B10 is the right drive requiring an entry of 2. Enter the drive that is being utilized and EXECUTE.

The next prompt asks the operator to select a test to be run. The CPU test is selected by entering 1. The Memory test is selected by entering 2. The Disk test is selected by entering 3. The 80x24 CRT display test is selected by entering 4. The 64x16 CRT display test is selected by entering 5. Continue from this point by referring to the following procedures on the diagnostic test you are performing.

(1) CPU DIAGNOSTICS

Enter 1 and EXECUTE for a CPU test. The screen prompt will ask if a hard copy of the test results is desired. Enter Y for yes or N for No, then EXECUTE.

Each individual test pass displays an OK or ERROR indication on the CRT. The cumulative Error Count will be displayed with the END OF PASS presentation at the end of the complete test.

The execution time for a CPU diagnostic test is approximately eleven and a half (11 1/2) minutes. The operator may terminate the program at any time by entering HALT, CLEAR and EXECUTE.

(2) MEMORY DIAGNOSTICS

Enter 2 and EXECUTE for a Memory test. The screen will prompt the operator to enter the system memory size configuration (set up by the RAM size jumpers). Enter either 8K, 16K, 24K, or 32K and EXECUTE.

The program will now provide endless RAM test loops until a failure occurs. A loop count will be displayed (for reference during a burn in procedure). You may terminate the program at any time by depressing HALT, CLEAR and EXECUTE.

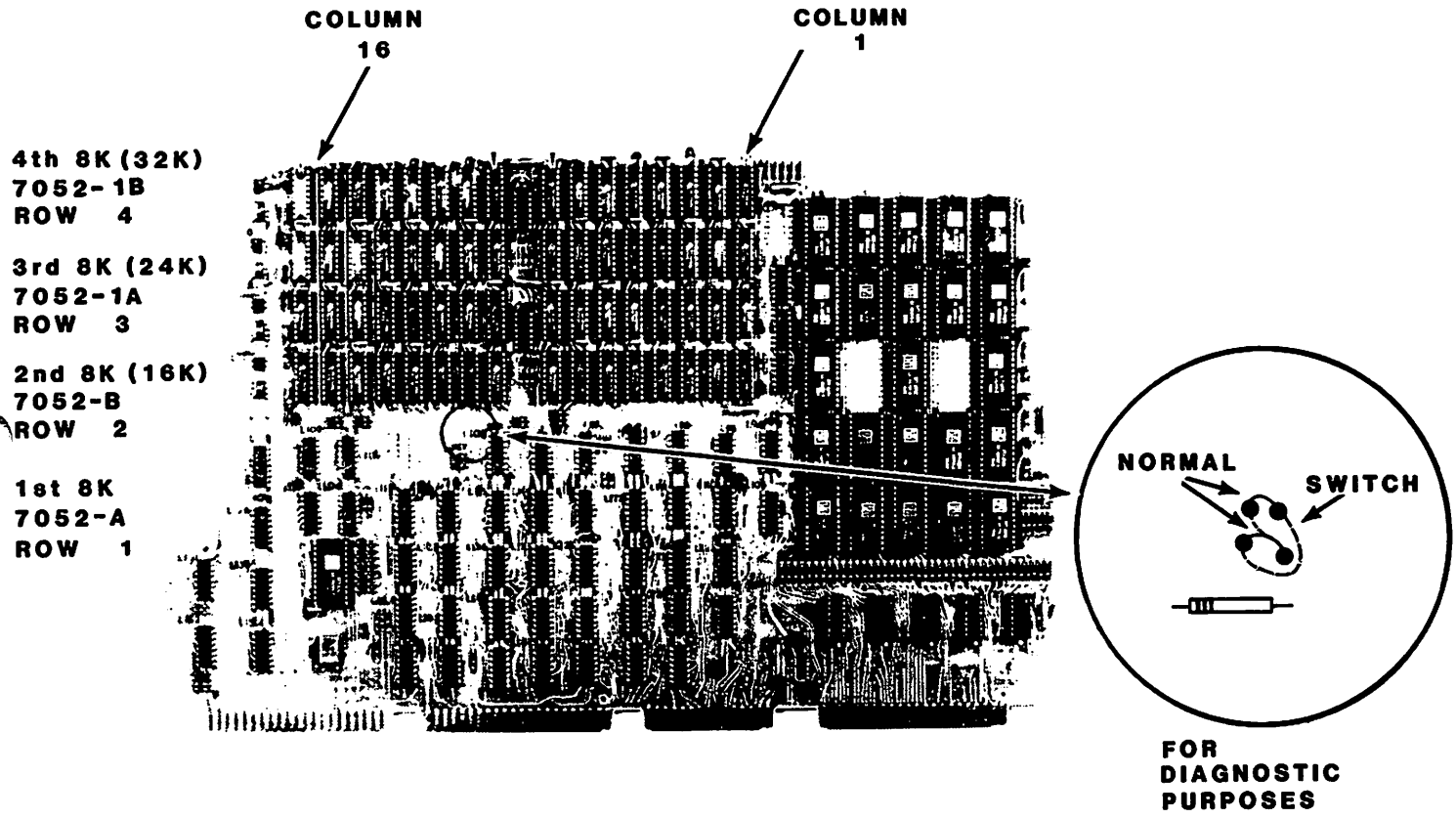
The CRT displays ER if a failure has been encountered. For hard failures, the program branches to a subroutine which displays the row and column numbers of the suspected faulty chip. Intermittent failures cause the program to branch to a subroutine which will designate several RAM chips as potentially faulty.

Vertical columns are numbered 1 thru 16 with the lowest numbers on the right side of the RAM array on the RAM/ROM board (REFER TO FIGURE 8). Horizontal rows are numbered 1 thru 4 with row 1 on the bottom.

700 bytes of memory from the bottom row of RAM chips are used for the diagnostic program itself and are not included in the actual diagnostics. These 700 bytes are probably functioning properly if the program is able to load correctly when the test diskette is inserted. However, by the reconfiguration of RAM board jumpers, these 700 bytes may be fully evaluated by the test program.

Two small jumpers are below the left side of the bottom row of RAM chips and to the left of chip L100 on the RAM/ROM board (REFER TO FIGURE 8). These jumpers allow you to switch the 1st and 2nd rows of RAM. The bottom row has now become the 2nd row in the circuit and therefore is capable of being fully evaluated.

Ensure that the jumpers are returned to normal. If a problem exits in a RAM data path (may be other than RAM chips), the program cannot load regardless of any jumpers. If that is the situation, the RAM/ROM board should be swapped with a known good unit for troubleshooting evaluation.



DIAGNOSTIC JUMPERS
FIGURE 8

(3) DISK DIAGNOSTICS

Enter 3 and EXECUTE for a disk test. A screen prompt will ask the operator to enter which drive or drives are to be tested. The operator may select the left drive by entering 1, the right drive by entering 2, or both by entering 3.

At this point, remove the diagnostic diskette from the drive. The screen will direct the operator to mount scratch platters (either blank or containing unimportant information). This is critical since data on inserted diskettes will be deleted and replaced by the test program.

After keying in EXECUTE, various disk operations are tested. The number of passes and errors are counted. The last system error is displayed. Error message appears to the right of the function that failed. Standard 2200 system error codes are utilized. If you selected a single drive test, the TESTING MOVE AND COPY function will not be a part of the diagnostic as this is a test between dual disk drives. The operator may terminate the program at any time by entering HALT, CLEAR and EXECUTE.

(4&5) CRT DISPLAY DIAGNOSTICS

Enter 4 for a 84x24 CRT DISPLAY test or 5 for a 64x16 CRT DISPLAY test. After the operater enters EXECUTE, the screen will be filled with similar characters on each alternate row. The program repeats a full screen of two characters at a time until all characters have been displayed.

If changes in pattern occur, try replacing the 7058 or 7159 Controller Board. If a character portion of the display is missing, try replacing the 7058 or 7159 board CRT display RAM chips.

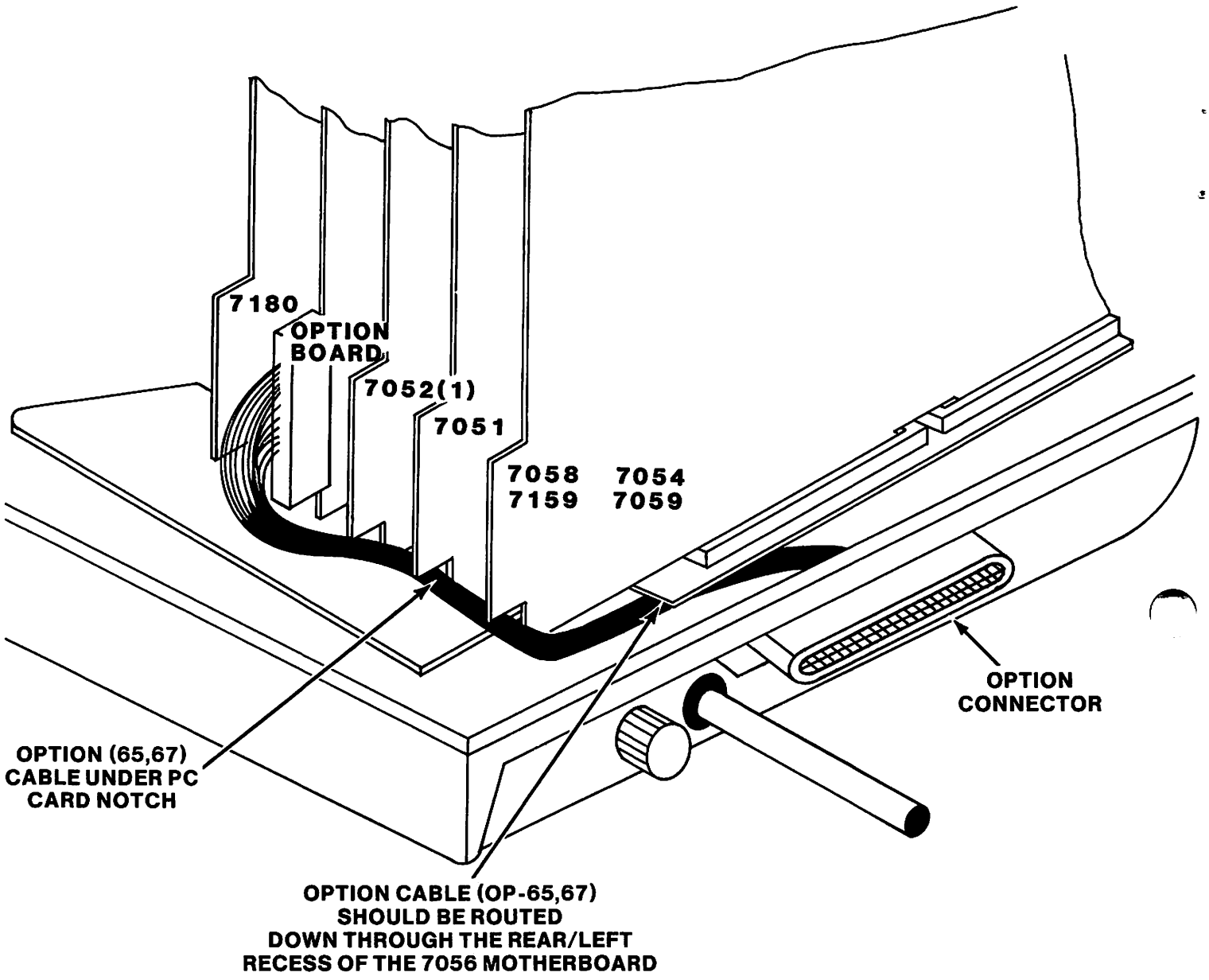
The operator may depress HALT to stop the screen for careful observation whenever necessary. The test is resumed by depressing CONTINUE and EXECUTE. The program may be terminated at any time by depressing HALT, CLEAR and EXECUTE.

OPTIONS

Below are some popular conversion options that are available for the PCS-II and PCS IIA units. However, the latest Wang publications should be consulted for the current list of available options.

OPTION	FEATURES
60	Adds an auxiliary diplay connector, an audio alarm, and a keyboard clicker.
60A	Converts the display to 80x24 characters.
61	Provides a connection to a 2201 output writer.
62	Provides an interface to A sync telecommunications.
62A	Provides an interface to Bi sync telecommunications.
65	Provides an interface to a 2242 controller.
67	Provides an interface to an 8 bit parallel I/O.

Mounting plates are available for options requiring the addition of a cable and rear panel connectors. These plates (P/N 451-4420 for 24 pin connectors and P/N 451-4421 for 36 pin connectors) replace the blank plate covering the optional I/O slot on the rear panel. Refer to FIGURE 9 for the routing of the option cable assembly.



OPTION CABLE ROUTING

FIGURE 9

CABLING BETWEEN PCS IIA WORKSTATIONS

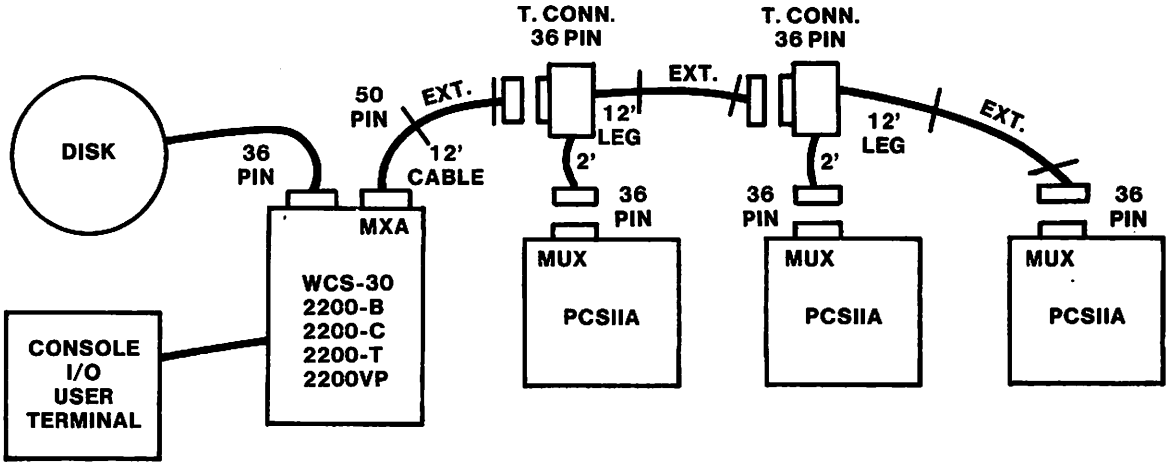


FIGURE 10

PCS IIA's may be used in multiple workstation systems as they have external drive capabilities. A 2200 chassis type CPU must be included in the total system configuration (REFER TO FIGURE 10). Any combination of chassis type CPU's and PCS IIA workstations (which have their own CPU) may be connected to a system provided a total of four (4) CPU's is not exceeded (REFER TO FIGURE 11).

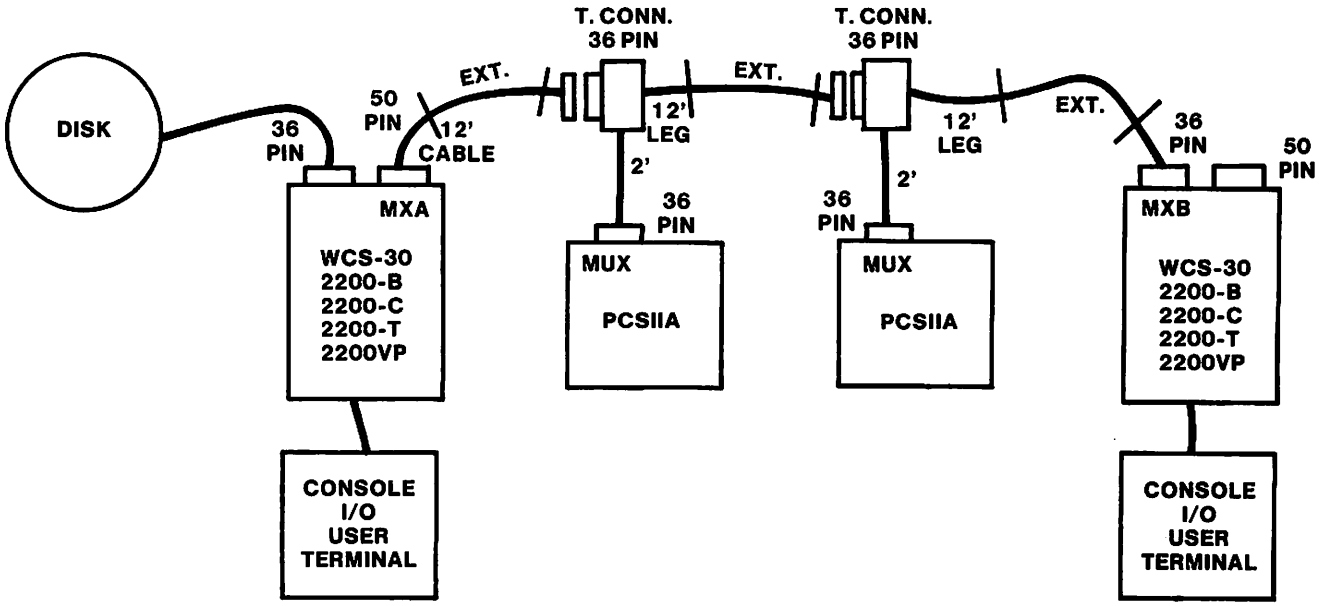


FIGURE 11

Cable extensions may be used in conjunction with the standard twelve (12) foot length cables used on the system. However, the cumulative EXTENSION LENGTH between all workstations and the master CPU cannot exceed five hundred (500) feet.

Extension cables are available in twenty five (25), fifty (50), one hundred (100), and two hundred (200) foot lengths. A T type connector on a standard twelve (12) foot cable is used for connections to PCS IIA workstations that are not at the end of the multiplexer chain. The two (2) foot section of the T connector cable must always go to the workstation. The twelve (12) foot sections are connected to the extensions.

The maximum distance between a 2200 chassis and the system disk is twelve (12) feet. This limitation disallows the use of an extension cable between a system disk and a 2200 CPU chassis.

A typical three (3) station configuration consists of a T chassis with a 2230 MXA board and two (2) PCS IIA units (REFER TO FIGURE 12). A disk drive and a user terminal is connected to the T chassis. A cable from the MXA board of the T chassis is connected to a T type connector. The two (2) foot section of the T connector goes directly to the MUX output plug on the first PCS IIA. The twelve (12) foot section of the T connector is connected to the MUX output plug of the second PCS IIA.

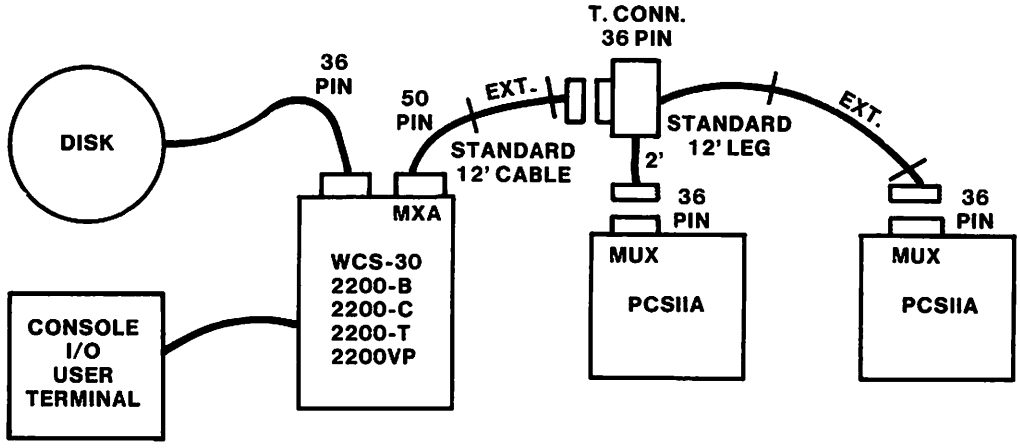


FIGURE 12

VOLTAGE ADJUSTMENTS

The voltages on the PCS II and PCS IIA are adjusted by trimpots on the 7156-2 regulator board (accessed with the front cover removed) while measurements are performed at the 7052(1) RAM/ROM board (accessed with the mini disk cover removed).

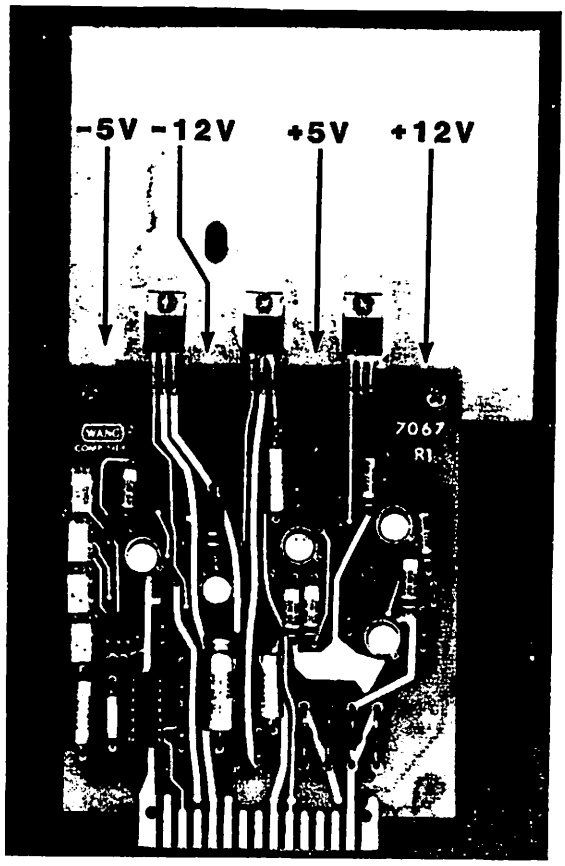
NOTE

a 7156-2 voltage regulator board must be installed. A 7156-1 board will probably burn out if inserted.

To remove the front cover, loosen the two finger nuts on the keyboard assembly and remove the special function strip. Remove the screws found under the function strip to permit removal of the keyboard cover. Remove the two screws found on the sides of the terminal cover.

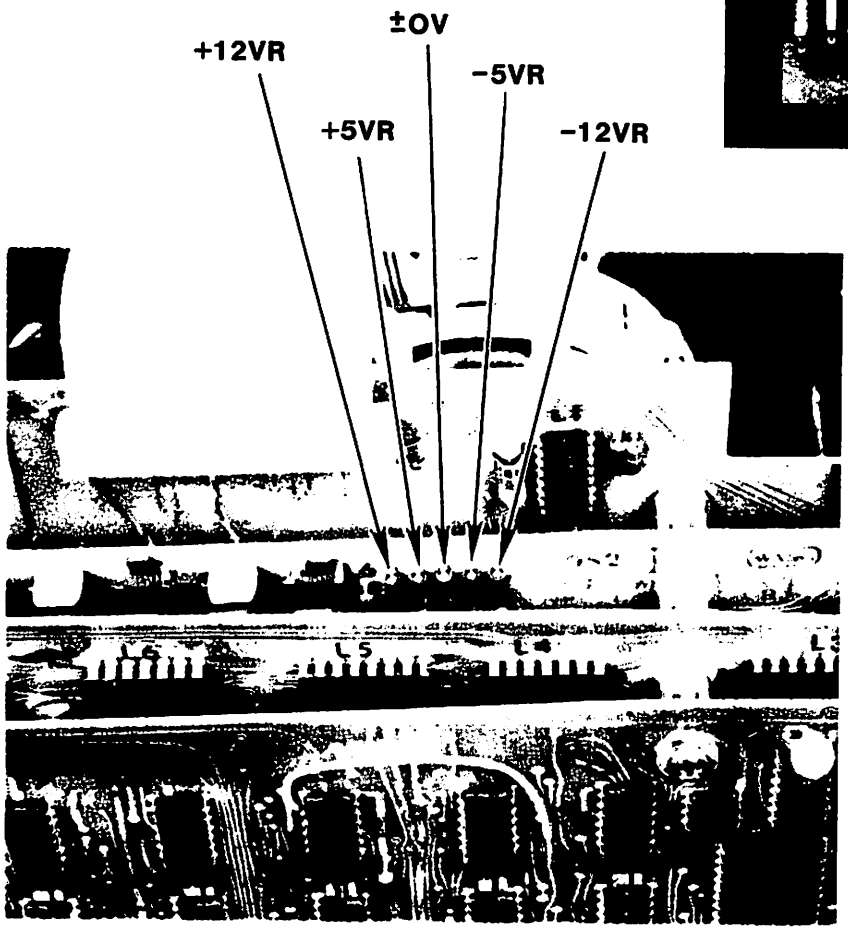
Carefully lift up the terminal cover enough to place a hand under the bottom of the front cover and then pop the front cover off. While leaving the contrast and brightness knob cable connected, place the front cover to the left side of the unit.

The -5 volt trimpot is closest to the front of the terminal, while the -12 volt trimpot is second from the front. The +5 volt trimpot is second from the rear, and the +12 volt trimpot is closest the rear of the terminal (REFER TO FIGURE 13).



7156-2 VOLTAGE REGULATOR

FIGURE 13



RAM/ROM (7052) BOARD VOLTAGE TEST POINTS

FIGURE 14

Connect the return (negative lead) probe of an AC/DC voltmeter to ground potential on the 7052 RAM board. This ground potential is located at the top of the middle resistor of the test point resistor cluster (REFER TO FIGURE 14).

Connect the positive probe of the meter to the top of the resistor found at the left end of the resistor cluster (while looking at the component side of the board). Adjust the +12 volt trimpot on the regulator board for +11.8 to +12.2 volts. Momentarily change the meter to read AC and observe that the ripple does not exceed 17.68 effective AC millivolts.

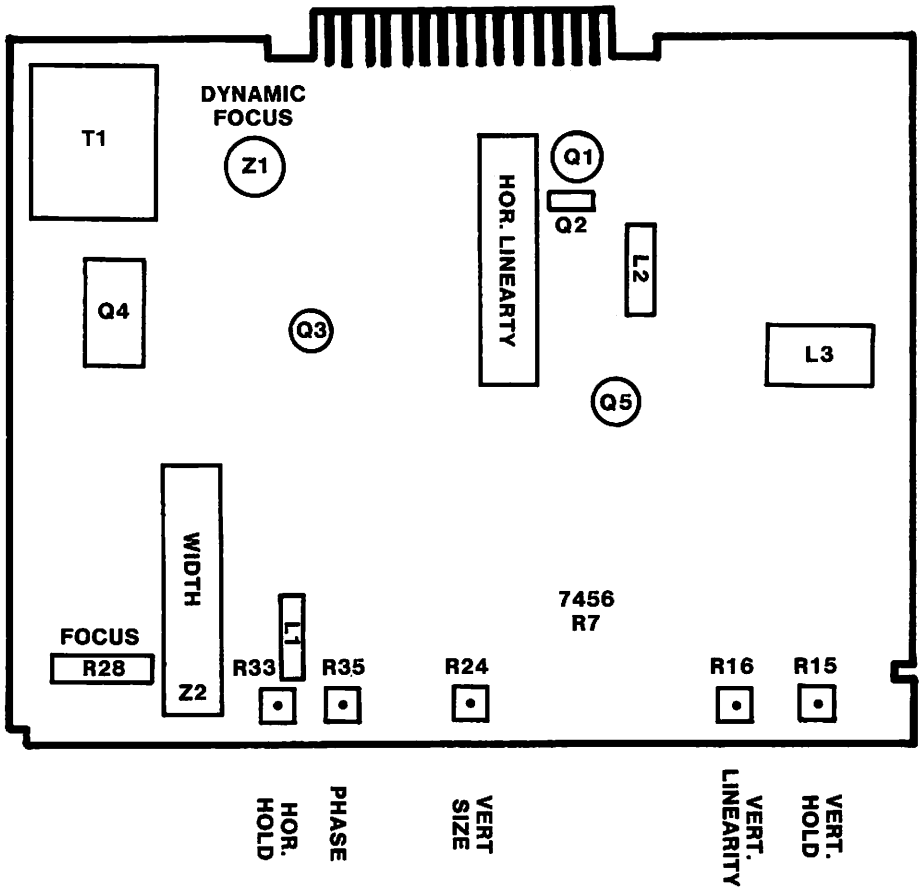
Connect the positive probe of the meter to the top of the resistor that is second from the left end of the resistor cluster. Adjust the +5 volt trimpot on the regulator board for +4.95 to +5.1 volts. Momentarily change the meter to read AC and observe that the ripple does not exceed 7.07 effective AC millivolts.

Connect the positive probe of the meter to the top of the resistor that is second from the right end of the resistor cluster. Adjust the -5 volt trimpot on the regulator board for -4.95 to -5.1 volts. Momentarily change the meter to read AC and observe that the ripple does not exceed 5.3 effective AC millivolts.

Connect the positive probe of the meter to the top of the resistor found at the right end of the resistor cluster. Adjust the -12 volt trimpot on the regulator board for -11.8 to -12.2 volts. Momentarily change the meter to read AC and observe that the ripple does not exceed 17.68 effective AC millivolts.

VIDEO ADJUSTMENTS

The video alignment controls are exposed when the front cover is removed. The video board is a 7456(1) and is the only board that will operate properly in either the PCS II or PCS IIA units (REFER TO FIGURE 15).



7256(1) VIDEO BOARD
FIGURE 15

At the extreme left end of the board are the focus, width, horizontal hold, horizontal phase, vertical size, vertical linearity, and the vertical hold.

The horizontal linearity adjustment coil is at the back of the board forward of the plug. The dynamic focus coil is at the left end of the back of the board and is adjusted at the repair depots for 250 volts AC peak to peak when the unit comes in for repair. It is not usually adjusted in the field.

Enter the following program to fill out the screen with HO's since the screen must be filled with characters before the picture can be adjusted.

```
10 PRINT "HO";
20 GO TO 10
30 RUN
```

Voltage adjustments should be performed prior to any video adjustment. The horizontal hold and vertical hold controls should be adjusted to the middle of their stable display range.

Adjust the vertical size control for a display height of 4 1/2 inches. Next, adjust the vertical linearity for character rows of equal height. Recheck the vertical size after the vertical linearity is adjusted and readjust if necessary.

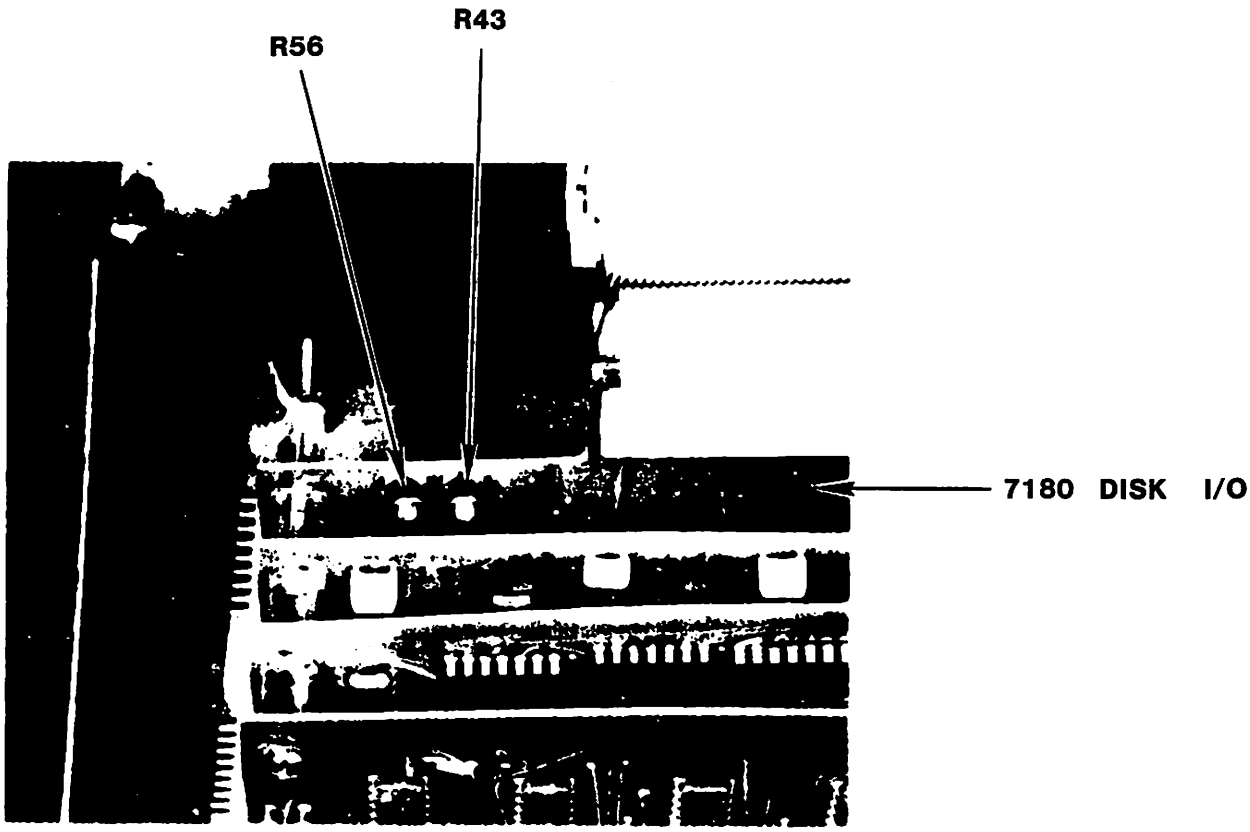
Adjust the width control for a display width of 6 1/2 inches. The horizontal linearity coil is then adjusted to give characters of equal width. Recheck the width after the horizontal linearity is adjusted and readjust if necessary. Increase the brightness to view the raster. Adjust the horizontal phase control to center the characters horizontally on the raster and then return to normal brightness.

Finally, adjust the focus control for best overall focus.

DISKETTE CONTROLLER ADJUSTMENTS

Two potentiometers on the top of the 7180 Diskette Controller Board adjust one shot pulse waveforms for a 5 microsecond duration pulse width signal (REFER TO FIGURE 16). These pulses ensure that data from the disks are sampled at the correct time. Adjustments to the potentiometers are not usually performed unless there are suspected disk problems.

Remove the terminal cover and diskette drive as described on page 1-3 to acccess these potentiometers. After the terminal cover is removed, remove the two screws holding the base of the diskette case to the terminal top. Catch the clamps from under each screw as the screws are removed.



DISKETTE ADJUSTMENT POTENTIOMENTERS
FIGURE 16

Place the diskette drive base, with the drives still fastened in place, carefully over the printed circuits boards. Reconnect the flat ribbon cables, the power cables, the ground wire, and the format switch plug (or resolder the format wire).

Insert a diskette in the left drive and enter the following verify statement:

```
10 VERIFY F (0,349)
20 GO TO 10
RUN
```

The verify statement has made it possible to adjust the pulse width on the left drive system. Without a diskette inserted in the drive, the pulse width can be adjusted. However, a listing of errors will occur on the screen because all sectors will be missing.

Place a positive scope probe to L18 pin 5 with the negative scope lead going to ground. L18 is the second chip from the left on the top row of the 7180 board (below the potentiometers). Adjust R56, which is the left potentiometer on the component side, for a 5 microsecond pulsewidth.

Repeat the same procedure for the right drive except that an R is used instead of an F on the verify statement. Place a positive scope probe to L18 pin 4 with the negative scope lead going to ground and adjust R43, which is the right potentiometer, for a 5 microsecond pulsewidth.

2200 E, F & PCS II
PCB BLOCK DIAGRAMS

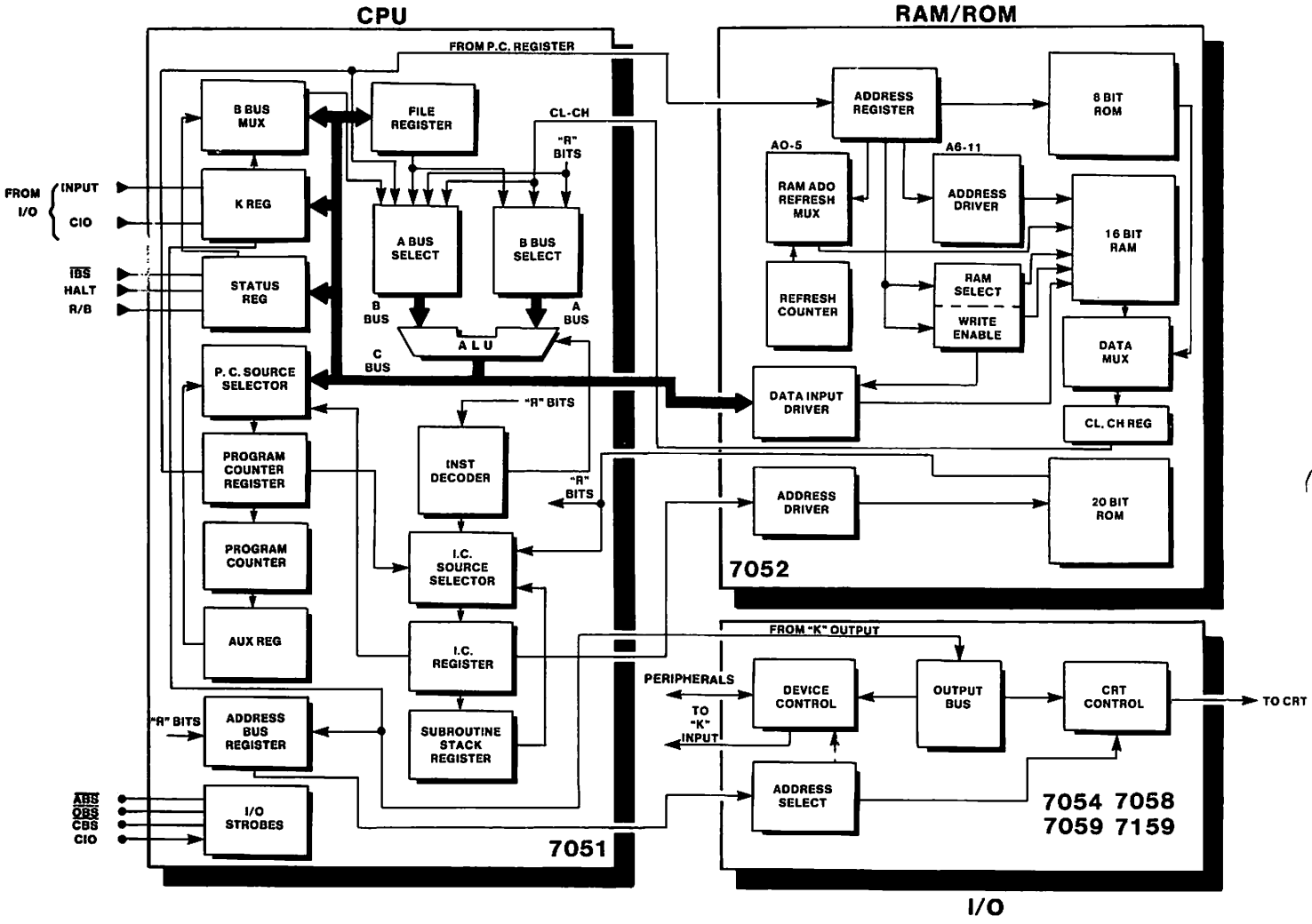


FIGURE 17

PCS II, IIA

CPU, RAM/ROM, I/O BLOCK DIAGRAM

PCB BLOCK DIAGRAM DESCRIPTIONS

Each of the three PCB block diagrams will be discussed individually. The purpose of each block on a board and its interaction with other blocks both within and outside the board will be explained.

CPU BOARD (7051)

The FILE REGISTER is at the upper right corner of the CPU block diagram (REFER TO THE CPU SECTION OF FIGURE 17). This register is used for general storage of intermediate A.L.U operations. The input to the register is from the C Bus (A.L.U.) The output is fed to either the A or B Bus Source Selectors for re-entry into the A.L.U.

The A and B BUS SOURCE SELECTORS are below the file register. The purpose of these source selectors is to direct any input to the A.L.U. via the A or B BUSSES.

Both the A and B Bus Source Selectors have inputs from the File Register, the "R" bits (direct from the Control Memory 20 Bit ROM), and the CL or CH Registers. Additionally, the B Bus Source Selector has inputs from the B Bus Multiplexer and the Program Counter.

The A.L.U. is below the A and B Bus Source Selectors. The Instruction Decoder decodes instructions from the Control Memory ROM ("R" bits) and applys them to the A.L.U. The A.L.U. then performs arithmetic or logical operations on information present on the A or B Busses and outputs the results to the C Bus.

The C BUS is the major output bus from the A.L.U. All information will usually reside in the C Bus at one time or another as it is processed through the C.P.U. The C Bus outputs to the "K" Register, the Status Register, the File Register, the Program Counter Source Selector, and the B Bus Multiplexer.

The C Bus will output A.L.U. data to the RAM/ROM board. This data is routed to the 16 Bit RAM (Data Memory) through the Data Input Driver on that board.

The INSTRUCTION DECODER is at the right center of the block diagram. This decoder receives information from the Control Memory ROM and directs the A.L.U. operations. Also, the decoder instructs the Instruction Counter Source Selector as to which input that selector will process.

The INSTRUCTION COUNTER SOURCE SELECTOR is below the Instruction Decoder. This Selector has inputs from the Program Counter Register, Control Memory ("R" bits"), and the Subroutine Stack Register. The output from the Instruction Counter Source Selector is fed to the Instruction Counter Register.

The INSTRUCTION COUNTER REGISTER receives the Control Memory ROM address from the Instruction Counter Source Selector and executes the instruction at the proper time. The output from this register becomes the Control Memory address to the 20 bit ROM (via the Address Driver).

The SUBROUTINE STACK REGISTER is at the bottom right side of the block diagram. This register is responsible for holding a Control Memory address instruction (the last instruction before a branch plus one) from the Instruction Counter Register while on a subroutine branch. When a subroutine return is being commanded, the stack will apply the "saved" instruction to the Instruction Counter Source Selector.

The PROGRAM COUNTER SOURCE SELECTOR is at the left center of the block diagram. The purpose of this selector is to route data from the C Bus, the Auxiliary Register, or the Instruction Counter Register to the Program Counter Register as an eventual address to Data Memory (16 Bit RAM).

The Instruction Counter Register input to the Program Counter Source Selector is an immediate address from Control Memory (20 Bit ROM). The C Bus provides an input from the A.L.U. The input from the Auxiliary Register will be discussed later.

The PROGRAM COUNTER is below the Program Counter Register. This Counter holds the next sequential Program Counter Register address by adding a count of one to the address being executed. The output is supplied to the Auxiliary Register for temporary storage.

The AUXILIARY REGISTER receives address data from the Program Counter while on a subroutine command. That "saved" address will be stored until the branch to the data memory subroutine is completed. The Auxiliary Register will output to the Program Counter Register when a return to the normal sequential flow is instructed.

The K REGISTER is the second block from the top of the left side of the block diagram. The K register is the register which controls both the input and output data. The inputs to the K register are from the peripheral (to be routed through the CPU) or from the C Bus (output to a peripheral).

The K Register outputs to the B Bus Multiplexer for entry into the flow of the CPU (Input) and to the Output Bus on the I/O Board for an instruction to an output device (Output).

The B BUS MULTIPLEXER is at the top left of the block diagram. This multiplexer has inputs from the C Bus, the K Register, and the Status Register. The output is to the B Bus Source Selector which then inputs to the A.L.U.

All input information from the K Register must pass through this multiplexer before entering the flow of the CPU. Also, C Bus data can be routed through the multiplexer before being reintroduced into the A.L.U. for more operations.

The STATUS REGISTER is the third block from the top of the left side of the block diagram. This register is used by the CPU to sense or control various hardware functions. One example of a hardware function is when the HALT key is depressed. The CPU can monitor this function (under program control) to determine when the operator has depressed that key. The Status Register can also be used to the indicate the CPU phase of processing, arithmetic logic operations, or other conditions. The output of this register is routed to the B Bus Multiplexer for entry into the CPU.

The ADDRESS BUS REGISTER is the section which is second from the bottom on the left side of the block diagram. The purpose of this register is to provide an address to the peripheral under CPU control. The input is from the K Register and control is under the instructional command ("R" bits) being executed. The output is routed to the Address Select circuitry on the I/O board.

The I/O STROBE section is at the bottom left side of the block diagram. The strobe circuitry generates strobes which enable the address bus, the output bus, and the control bus. The control bus strobe will command a peripheral (if conditions are met) to generate an input bus strobe. The main command to generate any strobe is the CIO strobe, which is command in/out.

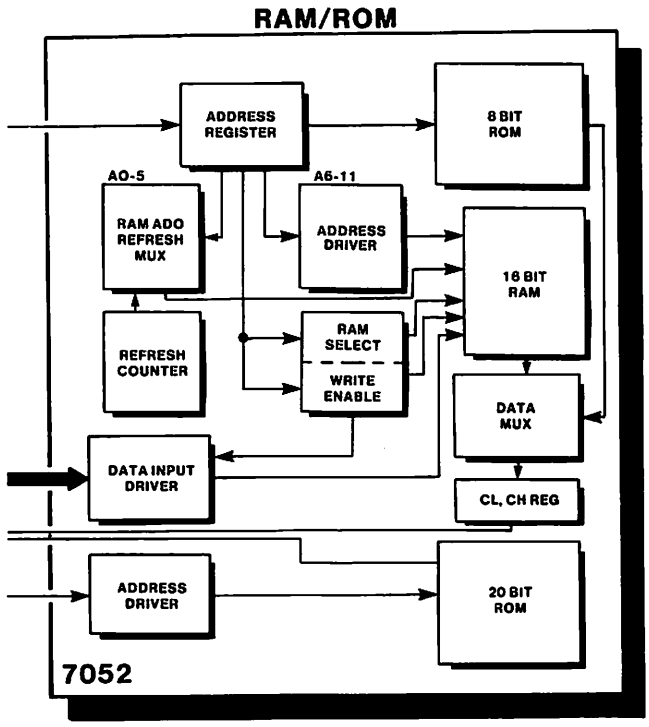


FIGURE 18

The 8 BIT ROM is at the upper right corner of the RAM/ROM diagram (REFER TO FIGURE 18). This ROM outputs predetermined instructions when an operator depresses complete verbs (LOAD, PRINT, RUN, etc.) or the math constant Pi.

The 8 bit ROM is addressed by the Program Counter Register (via the Address Register) and eventually outputs to the CL or CH Registers (discussed later).

The ADDRESS REGISTER is located at the upper left corner of the block diagram. This register receives address information from the Program Counter Register on the CPU board and outputs address data to the RAM Address/Refresh Multiplexer, the RAM Select and Write Enable circuitry, and the Address Driver for the 16 Bit RAM. These circuits will be discussed shortly.

The REFRESH COUNTER is located at the center of the right side of the block diagram. This counter provides periodic refresh pulses to selected rows of dynamic chips of the 16 Bit RAM array.

The RAM SELECT/WRITE ENABLE circuits are to the right of the Refresh Counter. These circuits are fed data from the Address Register. The RAM select will allow addressing of specified rows of RAM chips. The Write Enable will place the Data Input Register and the 16 BIT RAM in the write mode of operation.

The RAM ADDRESS/REFRESH MULTIPLEXER is below the Address Register near the top left corner of the block diagram. This multiplexer has inputs from the Refresh Counter and the Address Register. The output will either be the actual ROW address from the Address Register or refresh pulses from the Refresh Counter.

The ADDRESS DRIVER is located at the center near the top of the block diagram. This driver ensures an adequate address input to the 16 BIT RAM (Data Memory). The input to the driver is from the Address Register and the output is directly routed to the 16 bit RAM array.

The 16 BIT RAM (DATA MEMORY) is located at the right side of the block diagram. RAM is addressed by the Program Counter Register on the CPU Board through the Address Register, Address Driver, and the RAM Address Multiplexer. The RAM select input determines which row of chips is to be addressed. The Write Enable input determines if the RAM chips will be in a Read mode or a Write mode. The data input is sent from the A.L.U. on the CPU board to the Data Input Driver and then routed to the RAM itself.

The DATA INPUT DRIVER is located near the bottom of the left side of the block diagram. This driver an ensures an adequate drive level between the C bus (A.L.U.) and the 16 Bit RAM. The Write Enable circuitry is routed to the Data Input Driver allowing data input to RAM only during a write instruction.

The DATA MULTIPLEXER is located just below the 16 Bit RAM on the block diagram. This multiplexer selects either the 16 Bit RAM or the 8 bit ROM as an input to the CL or CH Registers.

The CL and CH REGISTERS receive data inputs from the 16 Bit RAM and 8 Bit ROM through the Data Multiplexer. The output from these registers is routed to the A and B Bus Source Selectors on the CPU Board. From the A and B Busses, the data is routed to the A.L.U. where arithmetic or logical operations are performed and the resultant passed on the C Bus.

The 20 BIT ROM (CONTROL MEMORY) is located at the bottom right of the block diagram. This ROM has address inputs from the Instruction Counter Register (CPU Board) via the Address Driver. The ROM output is the "R" bits which are routed throughout the CPU. These "R" bits are the instructions for CPU operation. The ROM also outputs to the Instruction Counter Source Selector (CPU Board) during the execution of an unconditional branch instruction.

The ADDRESS DRIVER for the 20 Bit ROM (Control Memory) is at the bottom left of the block diagram. The input is from the Instruction Counter Register on the CPU board. The driver output is routed to the ROM to maintain an adequate drive level to the address inputs.

Although not shown on the block diagram, a Master Clock of 10 megahertz is located on the 7052 RAM/ROM Board. This is the source of all the timing pulses for the various circuitry in the PCS II and PCS II mini-computers.

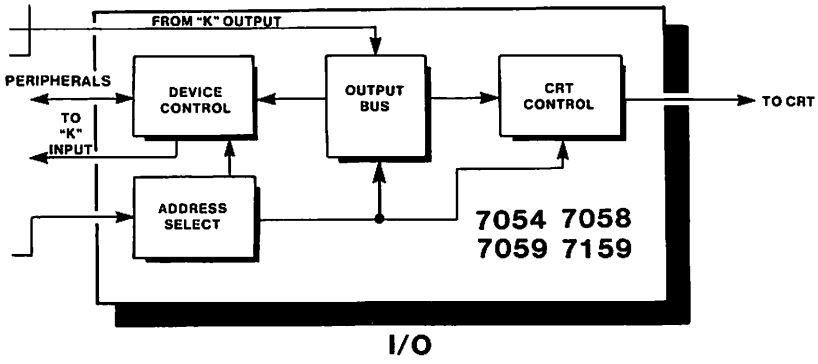


FIGURE 19

The ADDRESS SELECT is at the bottom left of the I/O block diagram (REFER TO FIGURE 19). This section receives data from the Address Bus Register on the CPU board and routes the address to either the CRT CONTROL or the DEVICE CONTROL (peripherals).

The OUTPUT BUS is at the top center of the block diagram. This Bus receives input data from the K Register on the CPU board and, under the control of the Address Select circuitry, sends that data to devices (printers, plotters, disks, etc.) or the CRT. The Device Control also routes input data to the K Register.

PREVENTIVE MAINTENANCE

PCS II and PCS IIA units must be properly maintained for trouble free operation. This requires periodic cleaning as well as the visual and electrical checks.

Cleaning intervals are determined by the amount of use and environmental conditions. Under normal conditions, cleaning should be performed every nine (9) to twelve (12) months. More frequent cleaning may be advantageous in areas of excessive air contamination.

TROUBLESHOOTING TIPS

Below are some troubleshooting techniques that are useful in keeping the equipment up to operational efficiency and the customer satisfied. Keeping customers satisfied is our primary goal.

Observe the equipment carefully. Look for any visual error indications, or error messages on the screen. Ensure that all switches are on. Sometimes noises or smells will allow you to zero in on the problem area.

Ask the customer to explain all the symptoms that were noticed. Do not argue with the customer. Customers do not call for service unless they sincerely believe there is a problem. Try to talk to the person who experienced the problem since second hand information is not always reliable.

Determine whether it is a hardware or software problem. If it is software, determine whether it is Wang software or customer software that caused the problem.

Protect customer data. Ensure that customer data is backed up. Use scratch packs whenever possible. Remove customer data if it is not needed for servicing.

Check all cables, plugs, and connectors for loose connections. Measure voltage and ripple. Out of tolerance voltages or ripples can cause intermittent problems or random errors.

Swap boards carefully. Ensure that all replacement boards are the same revision levels and that RAM and ROM loadings are similar to the original board. Carefully ensure that all jumper settings are identical between the original and replacement boards.

Swap peripherals with known good units for potentionally quick problem solving. Even if you have intermittent problems, swap the likely components. It is better to swap a component with hope for a fix (and to avoid a repeat service call) than to do nothing at all.

When leaving the customer's site, ensure that all switches are set correctly and that all equipment is left exactly the way you first saw it. Examples of this are: customer packs in drives, paper in printers, equipment in same location, etc.

SUMMARY

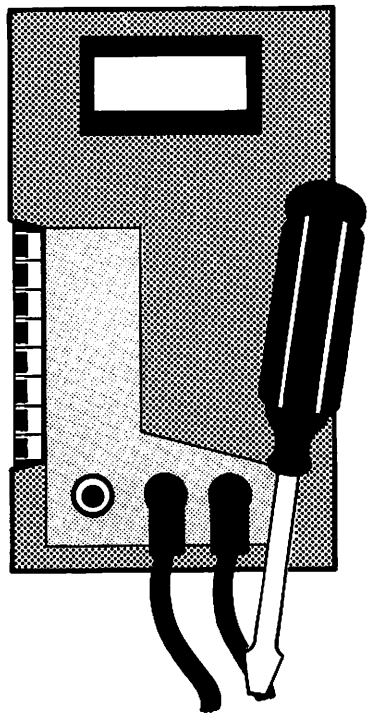
The laboratory exercises in Part 2 are intended to further the reader's understanding of the information presented in this workbook. Part 3 of the workbook contains a comprehensive self-administered quiz. The completion of this quiz will give the reader a good feedback as to how much information was retained from this training program.

The troubleshooting tips and procedures described in this workbook are sample guides for servicing the PCS II and PCS IIA personal computers.

The problems encountered will no doubt be varied. Therefore, maintenance manuals and service bulletins should always be consulted while servicing these units. This workbook and the video presentation are aids for use with those publications. Good luck in servicing these Wang products.

LABORATORY EXERCISES

PART 2



LAB EXERCISE #1

TERMINAL COVER REMOVAL(REFER TO PAGE 1-2)

The following steps compile a capsule version of the terminal cover disassembly/reassembly procedure found on page 1-2 of this workbook.

1) Turn Power Off.
2) Ensure that the fan is not rotating.
3) Remove the screw on the back of the minidisk cover.
4) Remove a flat ribbon connector and power connector from each disk drive.
5) Disconnect the format switch.
6) Remove the ground wire from either the left or right disk drive.
7) Remove the screws on the side of the terminal cover.
8) Loosen the finger nuts and remove the special function strip.
9) Remove the screws under the special function strip.
10) Using the finger nuts, lift the keyboard cover off the unit.
11) Lift up the terminal cover (with the disk drives mounted) and hold the cover up while disconnecting the fan plug and fan ground.
12) While still holding the cover up, disconnect the contrast and brightness cable.
13) Lift the cover completely off the unit and set it aside.
14) Reassemble the terminal cover to the unit by reversing the preceding procedural steps.

(Continued)

COMMENTS

LAB EXERCISE #2

IDENTIFICATION OF PCB's (REFER TO PAGES 1-4 and 1-5)

This exercise provides familiarization with the removal and replacement of Printed Circuit Boards as well as Board identification. First, remove the terminal cover by referring to the procedural steps in Lab Exercise #1. Remove the PCB's starting from the rear of the chassis. Figure 1 on page 1-3 is a graphic layout of the location of the Boards.

1) I/O BOARD Disconnect the video cable and remove the I/O board. After entering the board part/rev numbers and address setting, reconnect the video cable and reinsert the board.

P/N _____ REV _____

Address Switch setting(s) #1 _____ Hex #2 _____ Hex

2) CPU BOARD Remove the CPU Board. Note the manner in which the RAM size jumpers are configured (Refer to Figure 9 on page 1-20). Reinsert the board after entering the board part/rev numbers and the RAM size jumper configuration.

P/N _____ REV _____

_____ K

RAM SIZE JUMPER SETTING

3) RAM BOARD Remove the RAM board. Note how many RAM rows are filled with chips (Refer to Figure 10 on page 1-24). Also, note the two jumpers located under the bottom row of RAM chips, to the left of L100. Reinsert the board after entering the board part/rev numbers, RAM loading, and jumper configuration. P/N _____ REV _____

How many rows of RAM? _____ Equals _____ K of Memory

Jumpers, normal or swapped? _____

(Continued)

4) OPTION SLOT If there is an option board inserted in the third slot from the rear, remove the board and enter the board part/rev number. Refer to the Field Level Maintenance Guide #2, pages 167 thru 182 and enter the title of the option. Reinsert the board.
OPTION TITLE: _____

_____
P/N REV

5) DISK BOARD Disconnect the flat ribbon and format cables and remove the Disk Controller board. After entering the board part/rev numbers, reconnect all cables and reinsert the board.

_____
P/N REV

6) VOLTAGE REGULATOR BOARD Remove the voltage regulator board. After entering the board part/rev numbers, reinsert the board.

_____
P/N REV

7) HEAT SINK BOARD (Refer to Figures 2A and 2B on page 1-6) Visually inspect the heat sink board and enter whether 3 or 4 large power transistors are mounted on the board.
Number of Power Transistors? _____

8) VIDEO BOARD Remove the Video Board (Refer to page 1-33). After entering the board part/rev numbers, reinsert the board.

_____
P/N REV

9) Reassemble the Terminal Cover by reversing the procedural steps in Laboratory Exercise #1.

LAB EXERCISE #3

VOLTAGE ADJUSTMENTS (Refer to pages 1-23 thru 1-25)

Refer to page 1-23 and remove the diskette drive cover and the front cover of the terminal.

Locate the voltage adjustment trimpots on the voltage regulator board and the voltage test points on the RAM board by referring to Figures 13 and 14 on page 1-24.

While the meter is connected to the indiviudal test points, Position the function switch on the meter to measure DC voltage, then reposition the switch to measure the AC ripple voltage. Enter the readings on this sheet.

VOLTAGE	DC READING	AC RIPPLE (RMS)
+5v	_____ v (+4.95 to +5.1)	_____ mv (7.07 max)
-5v	_____ v (-4.95 to -5.1)	_____ mv (5.3 max)
+12v	_____ v (+11.8 to +12.2)	_____ mv (17.68 max)
-12v	_____ v (-11.8 to -12.2)	_____ mv (17.68 max)

Reassemble the front and diskette drive covers at the completion of this exercise.

(Continued)

COMMENTS

LAB EXERCISE #4

VIDEO ADJUSTMENTS (Refer to page 1-26 and 1-27

Remove the front cover the same manner as that used in the voltage adjustment exercise (Refer to page 1-23).

Note

Lab exercise 3 (voltage adjustments) should be performed prior to this exercise to ensure stable voltages.

Turn the brightness knob up to allow the raster to be seen. Center the raster both horizontally and vertically by adjusting the trim tabs on the CRT. Reset brightness to normal.

Fill the screen with HO's as described on page 1-27.

Follow the procedures described on pages 1-27 for the following adjustments:

1) Horizontal Hold - center of its range
2) Vertical Hold - center of its range
3) Vertical size for a height of 4 1/2 inches
4) Vertical linearity for characters of equal height
5) Repeat steps 3 and 4 until both are correct
6) Adjust the width to 6 1/2 inches
7) Adjust the horizontal linearity for characters of equal width
8) Repeat steps 6 and 7 until both are correct
9) Adjust the horizontal phase to center the characters horizontally on the raster (turn brightness up to see the raster)
10) Adjust the focus for best overall picture quality
11) Reassemble the front cover

(Continued)

COMMENTS

LAB EXERCISE #5

DIAGNOSTICS (Refer to Pages 1-14 thru 1-18)

This workbook gives specifics on how to perform diagnostic tests on the PCS II and PCS IIA. Therefore, this exercise relies heavily on the written material in the workbook.

Follow the instructions on page 1-14 and enter the END statement. This procedure will tell the operator how the RAM size jumpers on the CPU board are configured.

1) Insert Diagnostic Diskette #701-8000. Refer to page 1-15

2) Perform CPU Diagnostics. Refer to page 1-15

_____(Initial)

2) Perform Memory Diagnostics. Refer to page 1-16

_____(Initial)

3) Perform Disk Diagnostics. Refer to Page 1-18

_____(Initial)

4) Perform Display Diagnostics. Refer to Page 1-18

_____(Initial)

(Continued)

COMMENTS

LAB EXERCISE #6

DISK CONTROLLER SAMPLING RATE ADJUSTMENTS

(Refer to Pages 1-28 and 1-29)

Access the two disk controller pulse width potentiometers by following the cover removal procedures on page 1-28.

Refer to page 1-29 to expand the following procedures which are accomplished after the terminal cover is removed.

1) Position the disk drive assembly on top of the PCB's.

2) Insert a diskette in the left drive and enter the following verify statement:

```
10 VERIFY F (0,349)
20 GO TO 10
RUN
```

3) Place a scope across L18 pin 5 to ground on the 7180 diskette controller board.

4) Adjust R56 for a 5 microsecond pulse width.

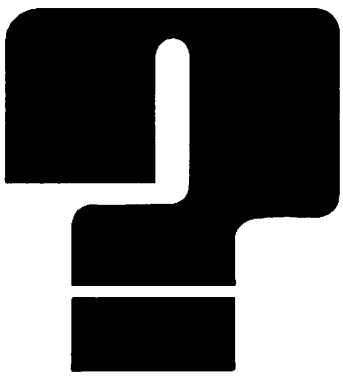
5) Repeat steps 1 thru 4 with the following modifications:
A diskette is inserted into the right drive, and R instead of F is used on the verify statement (step 2).
A scope is placed from L18 pin 4 to ground (step 3).
R43 is used to adjust the pulse width for the right drive (step 4).

6) Reassemble all covers by reversing the disassembly procedures.

(Continued)

COMMENTS

SELF-ADMINISTERED QUIZ



PART 3

SELF-ADMINISTERED QUIZ

1) What is the first precaution to be observed before removing the terminal cover on the PCS-II?

2) What is a reason for inserting a 7159 I/O Controller board?

3) Name the boards that are found in a PCS-II which has a 64x16 character CRT and a 32K Memory (without conversion options).

4) Identify the cables that are connected to the 7180 mini-diskette controller board.

5) Identify the voltages that may be adjusted on the 7067-2 voltage regulator board.

6) Why is the operation of a PCS II or IIA with a three (3) power transistor heat sink board hazardous to personnel when the cover is removed?

7) Which PCB contains the the I/O strobe circuitry?

8) Which PCB contains the CRT video control?

9) Which PCB contains the system timing?

10) What functions do the two address switches perform on the 7054 or 7059 I/O Board?

11) A PCS II has a serial tag of MODEL PCS II - 82B. With that information, identify: (A) RAM size____K,
(B) Number of mini-drives____,(C) Display size___x___
(D) What RAM board is installed?_____ (E) Rows of RAM____

12) How do you adjust RAM size circuitry on the PCS II?

13) What is a critical precaution to be observed when performing Disk Diagnostics?

14) What is the maximum length of ADDED Cabling Extensions that may be installed in a three workstation configuration, using a T chassis, and two PCS IIA's?

15) What covers must be removed to allow adjusting the regulated voltages on the PCS II?

16) Which video control adjusts the characters rows for equal height?

17) Which video control centers the characters horizontally on the raster?

18) How would you format a diskette on the PCS II?

19) On the RAM board, there are two jumpers for diagnostic purposes. What do these jumpers do?

20) How is the disk controller sampling rate adjusted?

Answers are found in the paragraphs and pages of the workbook as defined on page 3-4.

ANSWERS TO SELF-ADMINISTERED QUIZ

Refer to the following pages to discover the correct answers

1) Page 1-3, caution note
2) Page 1-4, par 2
3) Page 1-4, par 2 & 4
4) Page 1-4, par 5
5) Page 1-24, figure 14
6) Page 1-5, par 6
7) Page 1-34, par 3
8) Page 1-38, par 2
9) Page 1-37, par 5
10) Page 1-9, par 4
11) Page 1-12, figure 6
12) Page 1-11, par 6
13) Page 1-18, par 2
14) Page 1-22, par 1
15) Page 1-23, par 1
16) Page 1-27, par 5
17) Page 1-27, par 6
18) Page 1-1, par 4
19) Page 1-16, par 6
20) Page 1-28, par 1

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