

SPECIAL PRODUCT 9036

Introduction

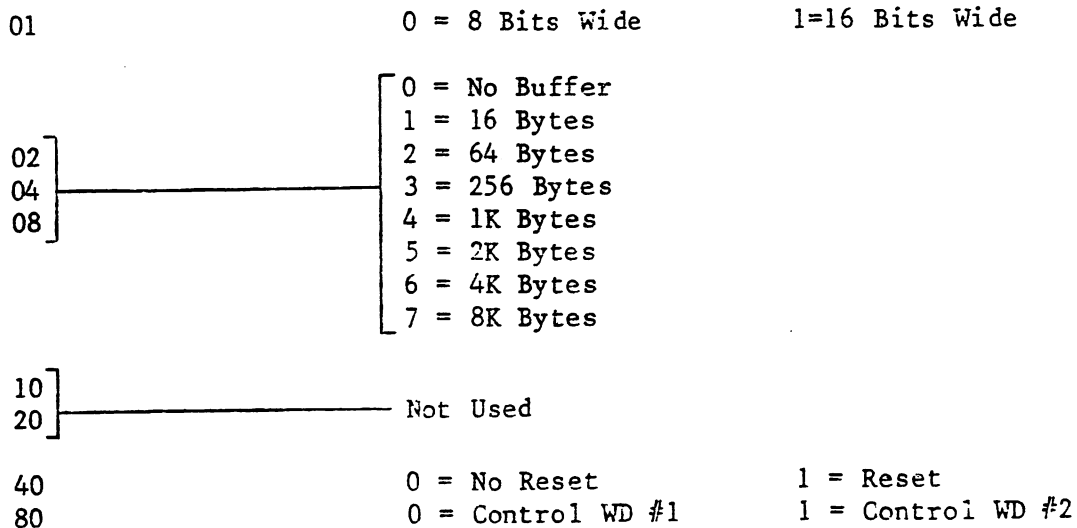
The 9036B buffered interface is designed to be upwardly compatible (functionally) with the 2250 8-bit parallel interface. The main feature/difference being that the 9036B is programmable to an 8 or 16 bit wide input with selectable buffer size and an 8 or 16 bit wide output with selectable buffer size. Also, the number of control output lines (COB's) is 8 VS 4 on the 2250.

Programming

The 9036B uses a control Word to select word length and buffer size. After initial power on or a reset the status word will be Hex (OF), indicating that the interface is looking for a control word. Control is accomplished through the use of \$GIO statements of the form:

```
$ GIO/265 (4h3h4 4h3h4, A$)
```

h<sub>3</sub>h<sub>4</sub> Bit Position



NOTES:

1. Control WD #1 is for Data Transfers from the CPU to the external Device.
2. Control WD #2 is for Data Transfers from the external device to the CPU.
3. Total combined buffer size cannot exceed 12K. The maximum combination is 8K in, 4K out or 4K in, 8K out.

Example: \$GIO/265 (4406 4487, A\$)

Hex (06) = Control WD #1  
256 Bytes Buffer  
8 Bits Wide Output

Hex (87) = Control WD #2  
256 Byte Buffer  
16 Bits Wide Input

- \* A one (1) in the reset position of either control word will cause the 9036B to issue a 1.2 us PRMS strobe to the external device, and to clear its own memory requiring that new control words be sent. Pressing the reset button on the CPU has the same result except that the PRMS strobe is 5 us long.

Status

The current status of the 9036B is obtaining by using a \$GIO statement of the form:

\$GIO/264 (7601, A\$)

Byte 1 of A\$, (STR (A\$, 1,1)), is the status.

## Bit Position

01	1 = Full	] [ Buffer from external device ] [ To CPU
02	1 = Empty	
04	1 = Full	] [ Buffer from CPU to ] [ External Device
08	1 = Empty	
10	1 = OBS strobe waiting. The 9036B hasn't processed the last data transfer from the CPU.	
20	1 = CPU Busy. The 9036B has data to transfer to the CPU but the CPU is busy.	
40	1 = Device not ready. The 9036B has data to transfer to the device but the device is busy	
80	1 = Device hasn't accepted the last data transfer. No ACK has been received.	

When the device is first powered or after a reset, the status word will be Hex (OF). This indicates that the device is looking for both control words. A status of Hex (OB) indicates waiting on control WD #2, while Hex (OE) indicates waiting on control WD #1. A status of Hex (OA) indicates that the device is ready to go.

## Addressing

As in the 2250 the 9036B uses 2 sequential addresses. The even address (264) is used for outputting data & for inputting status. The odd address (265) is used inputting data and for outputting the control word.

## Data

Data can be brought into the CPU via the following statements:

1. \$GIO
2. KEYIN
3. INPUT
4. Dataload BT/6 - Not for VP or MVP

Data can be sent from the CPU by using:

1. \$GIO
2. Data Save BT

The control BUS (COB1-COB8) is loaded by using a \$GIO statement of the Form:

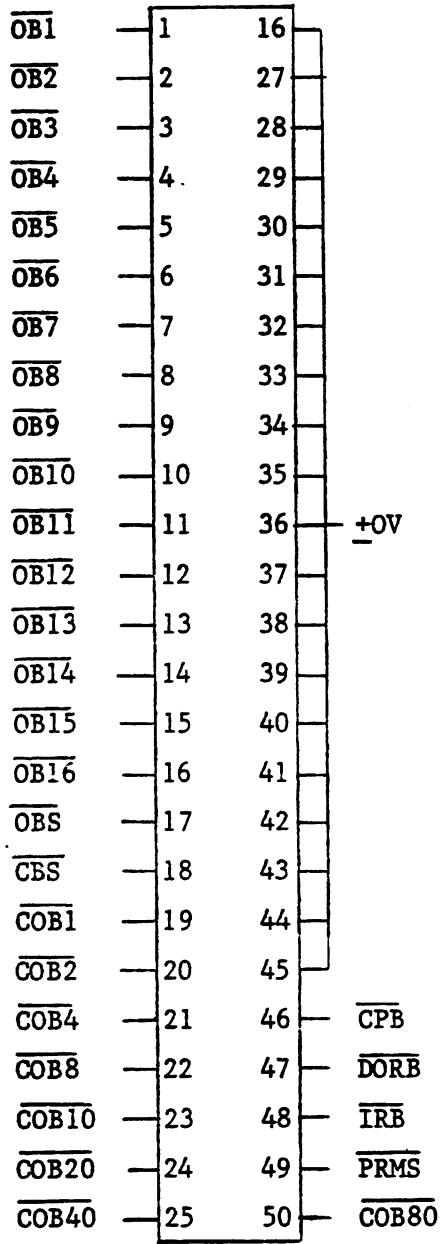
\$GIO/264 (44h<sub>3</sub>h<sub>4</sub>, A\$)

where h<sub>3</sub> h<sub>4</sub> is the BYTE to be loaded or

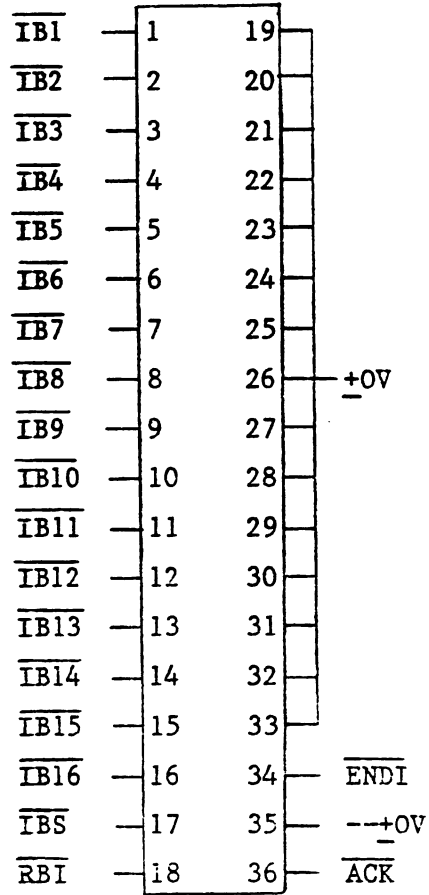
\$GIO/264 (46h<sub>3</sub>0, A\$)

where h<sub>3</sub> points to the BYTE in A\$ to be loaded.

J2



J1



## SIGNAL MNEMONICS AND DESCRIPTION

### A. INPUT CONTROL SIGNALS

IBS                    Input Strobe - A strobe received from an external device, indicating that data is available on IB1 - IB8, or IB1 - IB16, and the optional ENDI level. Data is latched in on the leading edge of the strobe.

IB1-IB16            Input Data (Buffered) - 8 or 16 bits from external device. These levels must be available at the leading edge of the IBS Strobe.

ENDI                    End-of-input or special-control level - an optional input level received from an external device. High (Logic "1", or open) = standard data, Low (Logic "0")= Special Byte. Some BASIC statements are designed to test the buffered END I level and execute alternate procedures if the level is low. If used, the level must be available at the leading edge of the IBS strobe.

CPB                    CPU Ready/Busy - High Level (Logic "1") indicates two conditions: 1) CPU awaiting input, and 2) interface enabled. This signal is not necessary when the 9036 is in the buffered mode, and should not be used in MVP applications.

IRB Input buffer Empty/Full - this level indicates the status of the input data latch on the 9036. High (Logic "1") = Empty, Low (Logic "0") = Full

PRMS Prime output strobe. A 5 uSEC strobe generated when the reset button is pressed. (Can also be generated under program control for MVP use, see Page 2). Generally the signal is used by peripheral devices as a reset/initialization signal.

B. OUTPUT CONTROL SIGNALS

ACK External Device Acknowledge - This strobe resets the DORB level to high (Logic "1"), Ready. Generally, if ACK is used, Dorb is tied to RBI so that the 9036 provides its own Ready/Busy level for output operations. The leading edge of the strobe should not occur before the trailing edge of an OBS or CBS Strobe

CBS Control output strobe - A 5 uSEC output strobe produced when 1 byte of control information is strobed to the control output buffer.

$\overline{\text{COB1-COB8}}$  Control Output Buffer - Contains the information latched by the  $\overline{\text{CBS}}$  strobe. These levels are latched until a subsequent  $\overline{\text{CBS}}$  strobe occurs.

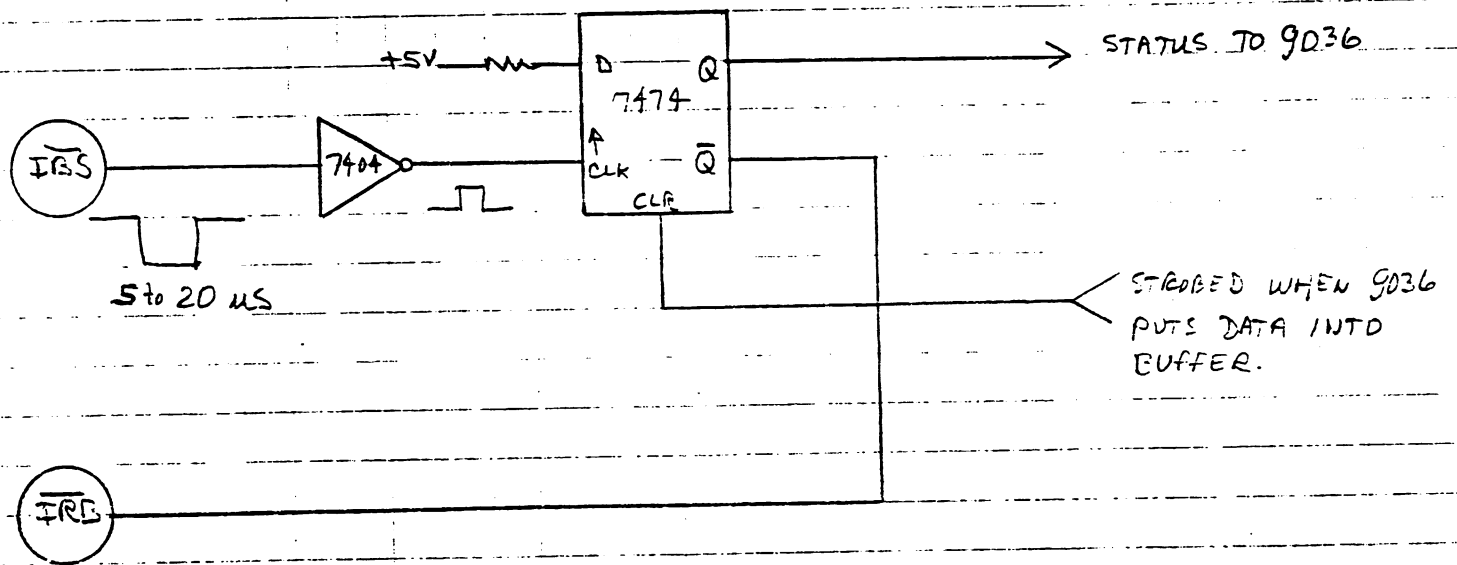
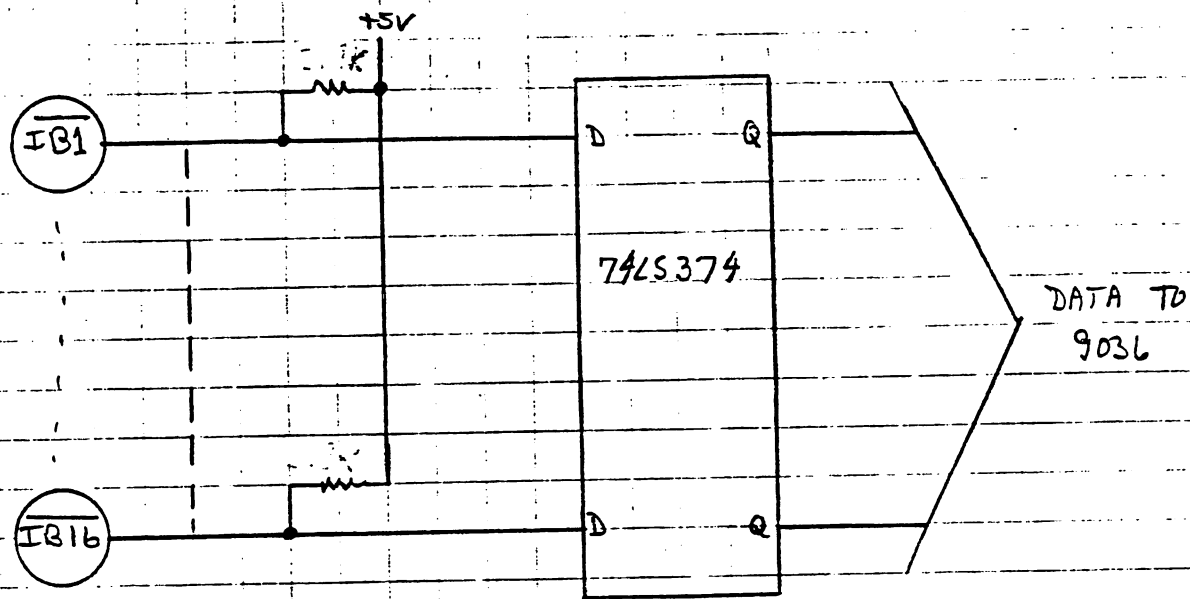
$\overline{\text{OBS}}$  Data output strobe - A 5 uSEC output strobe produced by the 9036 to signify that the 8 or 16 bits in the output buffer is valid data.

$\overline{\text{OB1 - OB16}}$  Output Data (buffered) - 8 or 16 bits of data that is sent to the output buffer just prior to an OBS Strobe.

$\overline{\text{DORB}}$  Data output buffer Empty/Full - this level is set low (Logic "0", Full) when an  $\overline{\text{OBS}}$  or  $\overline{\text{CBS}}$  strobe sends data to the output latches. Reset high (Logic "1", Empty) when the  $\overline{\text{ACK}}$  Strobe, rising edge, is received from the external device.

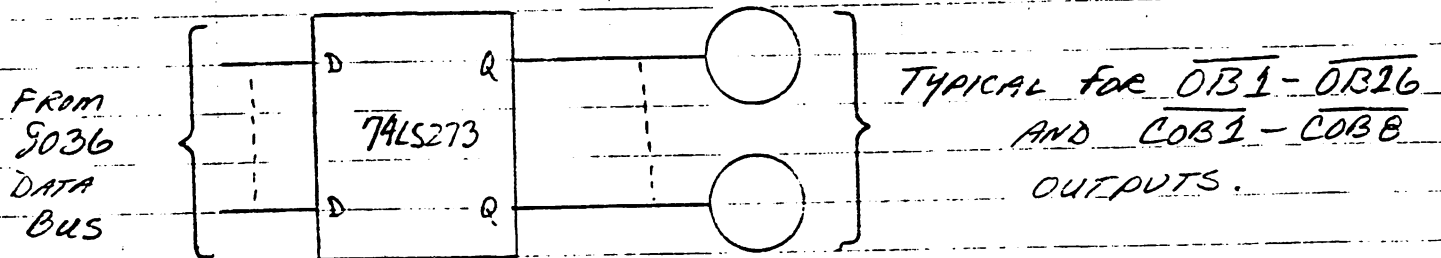
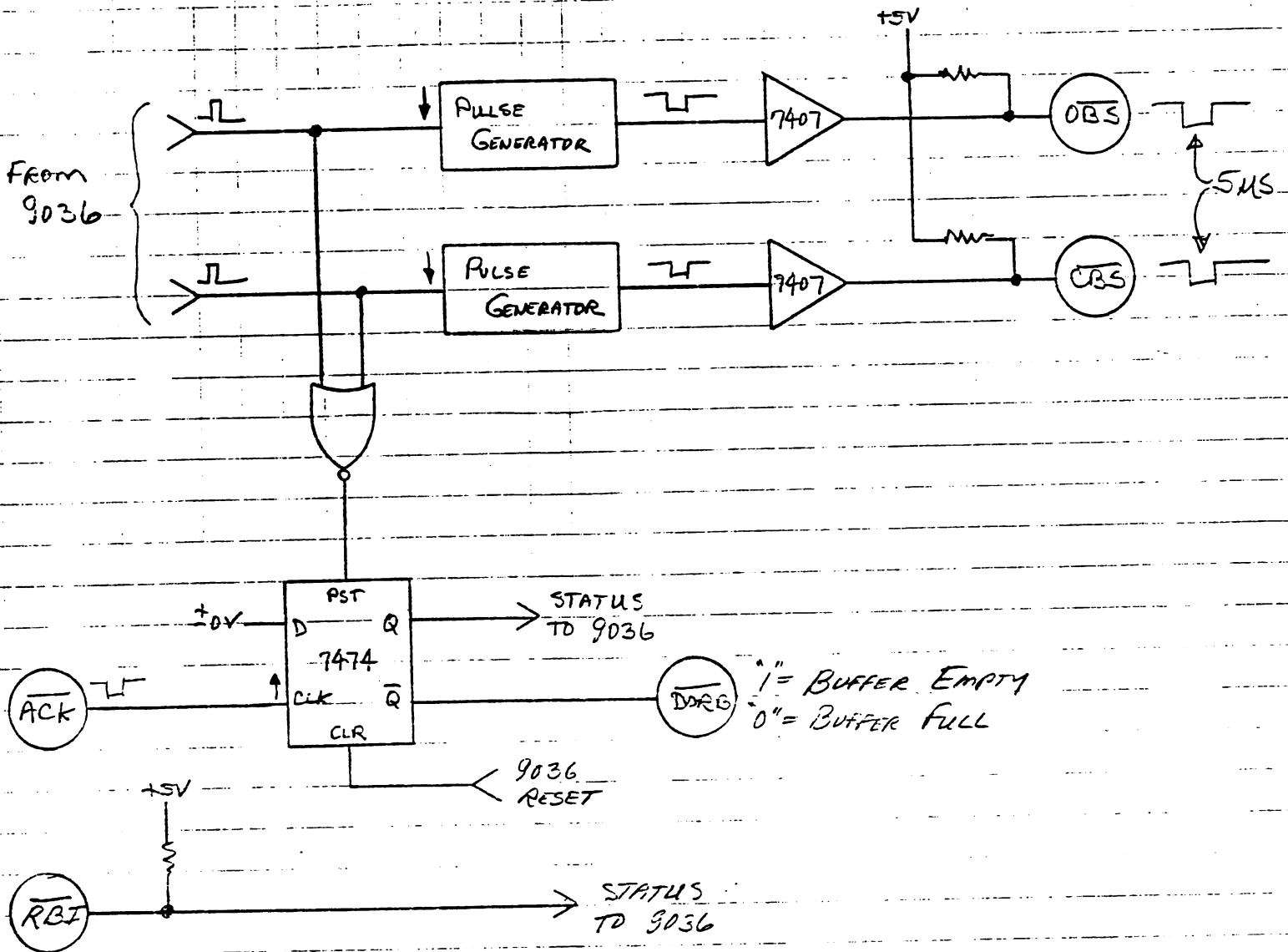
$\overline{\text{RBI}}$  External Device Ready/Busy - Level high (Logic "1" Ready) indicates that the device is ready to receive output from the 9036/2200 system. Level low (Logic "0" Busy) indicates that the device is not ready to receive data. This level should be set to low (Logic "0", Busy) by the external device within 2 USEC of the trailing edge of an  $\overline{\text{OBS}}$  or  $\overline{\text{CBS}}$  strobe, otherwise a second strobe may result from one ready level.





BLOCK DIAGRAM

9036 INPUTS



BLOCK DIAGRAM

9036 OUTPUTS