WANG

Micro VP Computer System

Models:

Micro VP-1
Micro VP-2

Customer Engineering
Product Maintenance Manual   **741-1668**

PUBLICATION UPDATE BULLETIN

TITLE: Micro VP Computer System

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Previous Notice(s):   741-1668-1

REASON FOR CHANGE:

This PUB. provides updated information to the appropriate sections of the Micro VP Computer System Product Maintenance Manual.

INSTRUCTIONS:

Remove and insert attached pages and/or microfiche as follows:

REMOVE PAGES	INSERT PAGES
v/vi	v/vi
	Appendix B

1.
2.
3.
4.
5.
6.
7.
8.
9.
10.

REMOVE FICHE	INSERT FICHE
Fiche 1	Fiche 1
Fiche 2	Fiche 2

1.
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4.

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WANG

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Models:

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Customer Engineering
Product Maintenance Manual   **741-1668**

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PREFACE

This document is the Product Maintenance Manual (PMM) for the Wang Micro VP Computer Systems. The manual is organized in accordance with Customer Engineering Technical Documentation's approved PMM outline. The scope of this manual reflects the type of maintenance philosophy selected for this product.

The purpose of this manual is to provide the Wang-trained Customer Engineer (CE) with sufficient instructions to operate, troubleshoot, and repair the Wang Micro VP Computer System. The manual will be updated on a regular schedule or as necessary. Such updates will be published either as Publication Update Bulletins (PUBs) or as full revisions.

First Edition (June, 1985)

Use of the material in this document is authorized only for the purpose stated in the Preface, above.

CUSTOMER ENGINEERING

PUBLICATION UPDATE BULLETIN

TITLE: 2275 MULTIPLEXER/MULTIPLEXER EXTENDER OPTION   DATE: 02/23/87

This PUB affects: 741-1668 ?*MicRovP* *WHAT MNL IS THIS,* CLASS CODE: 4103
742-1668 . *MNL TITLE.*

Previous Notice(s):   None

REASON FOR CHANGE:

To provide installation, checkout, troubleshooting, and parts-replacement data for the 2275 Multiplexer and 2275 Multiplexer Extender option for the Micro VP Computer System.

INSTRUCTIONS:

Remove and insert attached pages and/or microfiche as follows:

	REMOVE PAGES	INSERT PAGES
1.	v, vi	v, vi
2.		A-1 through A-15
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4.		
5.		
6.		
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8.		
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10.		

	REMOVE FICHE	INSERT FICHE
1.	1, 2	1, 2
2.		
3.		
4.		

This page constitutes a permanent record of revisions; place it directly following title page.

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741-1668-1

WARNING

Do not open the switching power supply under any
circumstance. Extremely dangerous voltage and
current levels (in excess of 300 volts DC and
unlimited current) are present within the power
supply.

Do not attempt to repair the switching power supply;
it is field replaceable only.

After powering the unit down and disconnecting the
AC power connector from the power source receptacle,
allow one minute before removing the power supply to
provide adequate time for any residual voltage to
drain through the bleeder resistors.

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CHAPTER 1

INTRODUCTION

1.1 SCOPE AND PURPOSE

This Product Maintenance Manual (PMM) concerns the the Wang Micro VP Computer System, and provides field personnel with the information necessary to:

- Unpack and Install the System
- Perform Preventive Maintenance Procedures
- Perform Diagnostic Tests
- Analyze Failure Indications
- Replaced Failed Assemblies

1.2 APPLICABLE DOCUMENTATION

A complete listing of Wang technical documentation is presented in the Technical Documentation Catalog/Index (742-0000). Other product documentation is identified in the Corporate Resource Catalog (700-7647).

1.3 SYSTEM DESCRIPTION

The Wang Micro VP is an interactive, multi-user, multi-task, disk-based computer system, utilizing VLSI (Very Large Scale Integration) technology. The Micro VP supports up to thirteen terminals and sixteen jobs (partitions) concurrently as well as a wide range of peripheral devices, such as printers, plotters, disk drives, tape drives, and TC devices.

By utilizing VLSI, the Micro VP processor design is incorporated into a single chip. This allows the Micro VP CPU, control memory, and user memory to reside on a single PC board. There are two models of Micro VP Computer systems. The Micro VP-1 contains 128K of data memory while the Micro VP-2 contains 512K. In addition, both systems contain 32K of control memory.

1.4 SYSTEM SPECIFICATIONS

Physical Dimensions:

Width: 15-1/8 in. (38.4 cm)
Depth: 21-3/4 in. (55.25 cm)
Height: 8-3/4 in. (22.24 cm)

Power and Environmental Requirements:

Input Circuit: Dedicated 20A circuit
Voltage: 115/230 VAC ± 10%
Frequency: 50/60 HZ.
Running Current: 2.0 amps @ 115 vac
1.0 amps @ 230 vac

Operating Environment:

Ambient Temp.: 60 to 80 degrees Fahrenheit
15 to 28 degrees Celsius

Government and Industry Standards and Approvals:

Domestic: UL Standard 114
FCC Class A
Int'l: CSA Standard C22.2 NO 154
IEC 435
VDE Standard for Germany

Service Space Required:

Allow 30" between wall and each unit in
system.

Special Specifications:

None

1.5 SYSTEM OPTIONS

Both the Micro VP-1 and Micro VP -2 Computer Systems require a minimum
configuration of one workstation, one disk drive, and one printer. A number of
peripherals are supported, a list of which follows;

Model	Description
2201L	Character Printer
2209AV	Nine-Track Mag. Tape Drive
2211M	Printer Multiplexer
2221W	Matrix Line Printer

1.5 SYSTEM OPTIONS CONT.

Model	Description
2227B	Buffered Asyncronous Communications Controller
2228B,C,D,E,F	Binary Syncronous Communications Controller
2229	Tape Controller
2230MXA	Master Daisy Chain Disk Mux Controller
2230MXB	Slave Daisy Chain Disk Mux Controller
2231	Line Printer
2231W-1,2,6	Matrix Line Printers
2231W-3	Aux. Printer for the X2282 Graphics Terminal
2232A/B	Digital Flatbed Plotter
2233	Matrix Line Printers
2234,34A	Hopper-Feed Punched Card Reader
2235	Matrix Line Printer
2236MXD	Multiplexer
2236MXE	Multiplexer
2236D,DE,DW	Interactive Terminal
2336DE,DW	Ergo Interactive Terminal
2240-1,-2	Dual Removable Flexible Disk Drive
2241	Thermal Printer
2244A,44B	Hopper-Feed, Mark-Sense Punched Card Reader
2245	Matrix Line Printer
2251	Matrix Line Printer
2260,60BC,60C	Fixed/Removable Disk Drives
2261,61W	Matrix Line Printer (240 lpm)
2262-1,-2,-3	Digitizer
2270	Removable Diskette Disk Drive
2270A-1,-2,-3	IBM 3740-Compatible Diskette Drive
2271,2271-P	Bidirectional Output Writer
2272-1,-2	Triple Pen Drum Plotter
2273	Band Printer
2275	Disk
2280-1,-2,-3	Fixed Removable Disk Drive (Pheonix)
2281	Daisy Output Writer
2281P	Daisy Plotting Output Writer
2281W	Wang Daisy Output Writer
2282	Graphics CRT Plotter

CHAPTER 2

THEORY OF OPERATION

2.1 INTRODUCTION

Overall operation of the Micro VP CPU (Micro VP-1 and Micro VP-2) is controlled by the CPU/Memory board (210-8034). This chapter provides a brief description of this CPU.

2.2 CPU FUNCTIONAL THEORY

The Micro VP CPU/Memory board contains the Micro 2200 chip, a 121 pin gate-array which comprises the entire CPU. The chip requires +5 volts at VDD1-2 (pins B7 and M7) and ground at VSS1-2 (pins G2 and G12). A 5 MHZ square wave at pin F1 provides the system clock.

2.2.1 Control Memory

The CPU/Memory Board contains 32K of Control Memory. This is accomplished by loading 12 memory chips in board locations L13 through L18 and L20 through L25 (ref. Fig. 2-1).
Locations L1 through L12 of the CPU/Memory board are not loaded with memory chips. These locations are for possible future expansion.
The Control Memory is made up of 8k x 8 Static RAM configured in groups of three so that each group forms 8K of 24 bit words (one bank). Four of these groups (banks) produce 32K of control memory.

2.2.2 Bootstrap Proms

Three 2K x 8 proms, configured to form 24 bit words, comprise the bootstrap prom. If the address decoded on the system bus is between 8000 and 83FF the bootstrap proms are enabled and chip select for the control memory store is inhibited.

2.2.3 Data Memory

2.2.3.1 128K Data Memory (Micro VP-1)
With a 128K Data Memory configuration there are 2 banks, with 9 chips in each bank, for a total of 18 chips. Each chip contains 64K x 1 bit which produces 64K x 9 bits (8 bits data plus 1 bit parity) in each bank. Together the two banks produce 128K 8 bit bytes plus parity.

2.2.3.2 512K Data Memory (Micro VP-2)
With a 512K memory configuration, there are 2 banks, with 9 chips in each bank, for a total of 18 chips. Each chip contains 256K x 1 bit which produces 256K x 9 bits (8 bits data plus 1 bit parity) in each bank. Together the two banks produce 512K 8 bit bytes plus parity.

BOOTSTRAP
PROMS

CONTROL
MEMORY
(32K)

DATA
MEMORY
(128K or 512K)

XTAL
CLOCK

B-02381-FY85-3

DATA MEMORY
CONTROLLER

VLSI
CPU CHIP
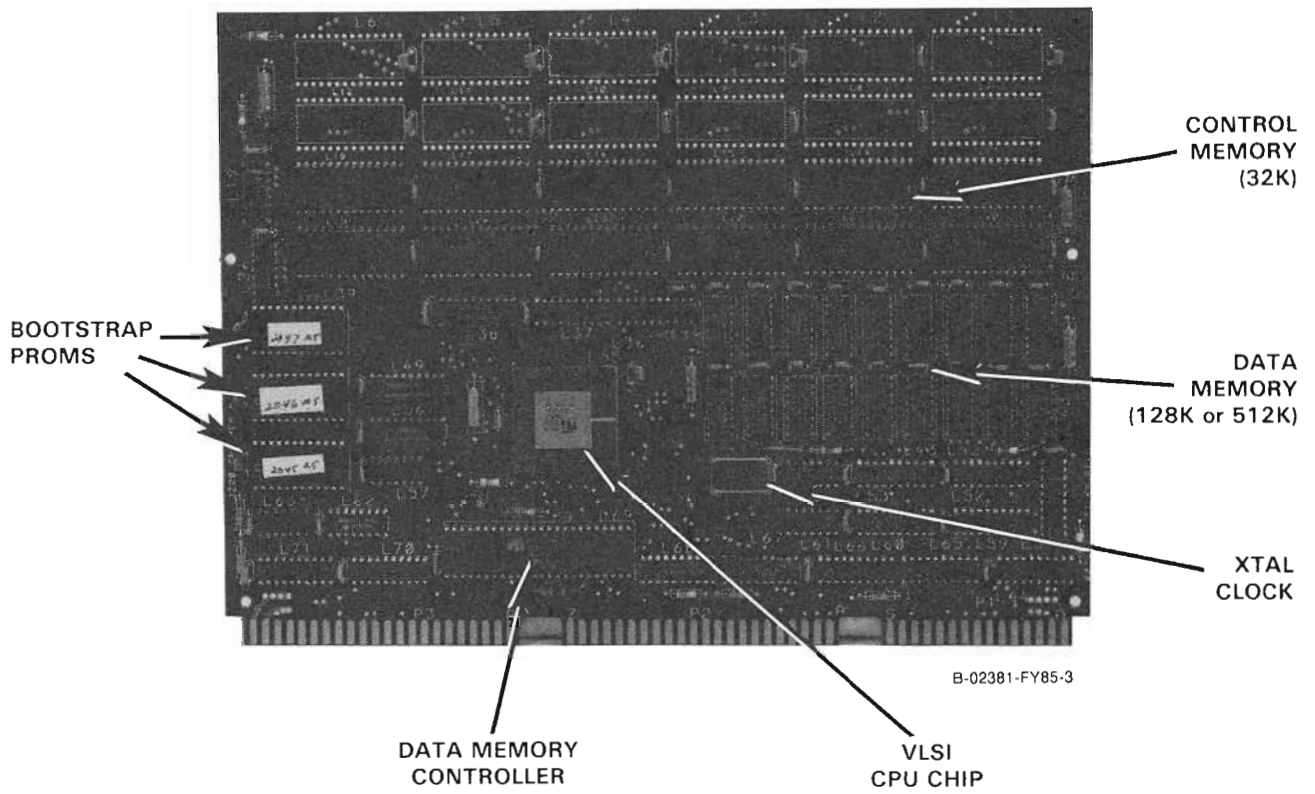
Fig. 2-1 CPU/Memory Board

2.2.4 Memory Partitioning

Memory Partitioning is a technique used in the allocation of available data (user) memory space. Each "partition" represents a block of memory space with specified address boundaries. The Micro VP is configured such that each user is allocated one or more blocks (partitions) of data memory which belong exclusively to him.

2.2.5 Generating Partitions

The number of partitions to be created and the amount of data memory to be allocated to each partition are specified by the user in a process called "partition generation". This process involves specifying certain attributes for each partition and supplying the addresses of peripheral devices connected to the system (ref. Chapter 4).

Once the Operating System has been loaded into Control Memory, a special utility program called @GENPART is loaded and executed at workstation #1. This program, through a series of display prompts, guides the system operator through the necessary steps for "partition generation" (ref Chapter 4).

With partition generation implemented, the system handles each partition as it would the entire data memory space of a single-user system, with space allocated for housekeeping, user program, work areas, and data tables. (See Fig. 2-2.)

LOWEST PARTITION ADDRESS ("Beginning" of Partition)

HIGHEST PARTITION ADDRESS ("End" of Partition)
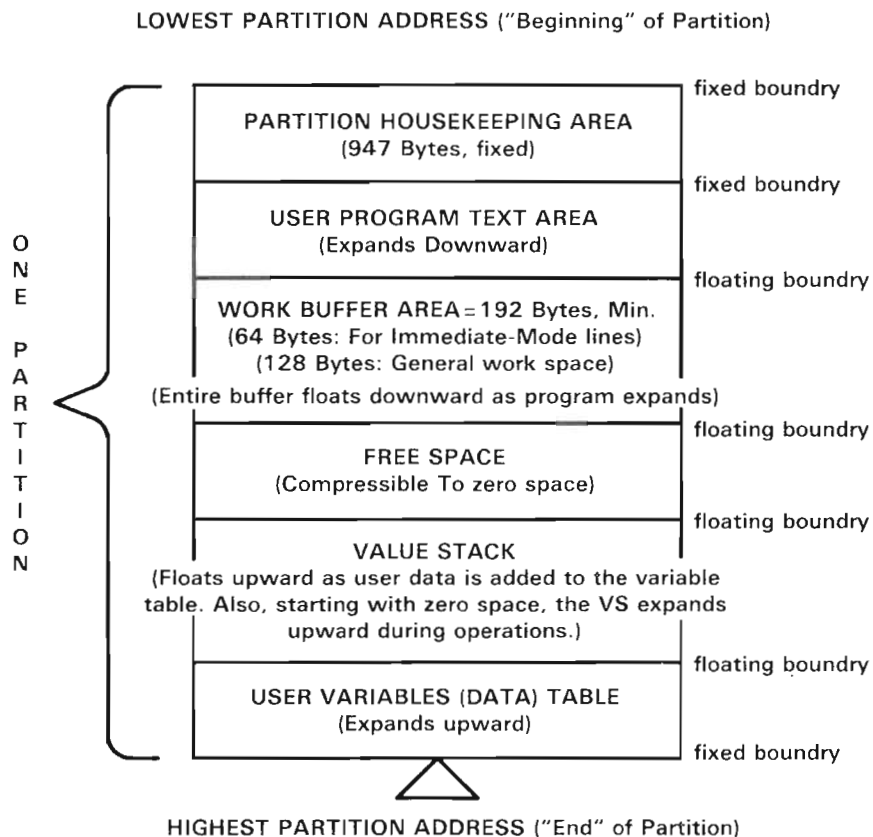
B-02381-FY85-2

Figure 2-2 Memory Partition

2.2.5 Partition Generation (Cont.)

The Micro VP Operating System will support a maximum of 16 partitions and 13 system users. All 16 partitions may be allocated to a single user, or multiple-partition configurations may be created. Partition sizes are specified in 256 byte increments. The minimum size that may be specified for a partition is 1.25K (1280 bytes), with some portion of each partition accessable to all users (ref. 2.2.6). The guideline for maximum size, is that each partition must be defined wholly within the confines of one memory bank; no user partition is allowed to extend from one bank to another. The Micro VP-1 system contains 2 banks of user data memory, with each bank comprised of 64K of memory space, while the Micro VP-2 system has 8 banks of user data memory, also comprised of 64K each. (Ref. Fig. 2-1.)

2.2.6 "Global Partitions"

Although partitions function independently, there are situations in which it is highly expedient for two or more partitions to cooperate with one another, to share common information, common programs. This sharing eliminates needless duplication of applications software and data, thus allowing more efficient use of available data memory space.

Partitions can therefore be "global"; that is, each partition designated as such, contains programs and/or data which become conditionally shareable. A foreground or background program that is running in a partition in one bank can access any global partition residing in that same bank. Additionally, a user terminal that is attached to a partition in that same bank can access those global routines and/or data.

Another form of "Global Partition" is an area in memory which contains programs and/or data which must be accessible to all system users. This area is restricted to the first 5K block of data memory and is called a "Universal Global Partition".

2.2.7 CPU, Memory, and I/O Interface

As previously mentioned, the CPU functions are handled by a single VLSI chip (L55) on the CPU/Memory Board. Control Ram is accessed through Control Memory Access Lines CA0 through CA15 and bi-directional data is passed through Control Memory Data Lines CD0 through CD23. Two rows of data ram are accessed through Dynamic Ram Control and Data Address Lines DA0-DA18. Data is then transfered through memory data lines DD0-17, with DD9-17 being used as input for 16 bit read operations (18 if parity bits are included) only. Data lines DD0-8 are bi-directional and are used for both read and write operations.

I/O devices are accessed through an 8 bit address bus AB1-AB8 and data is passed through an 8 bit output data bus OB1-OB8. A 9-bit input bus, IB1-IB9, from the I/O devices to the CPU completes the interface. Overall control of the address bus, output bus, and input Bus is accomplished by the CPU pulses OBS, IBS, ABS, and CBS. (Ref. Fig. 2-3).

2.2.8 Switching Power Supply

The SPS255 Switching Power Supply is capable of outputting four supply voltages +5, -5, +12, and -12 volts dc. The power supply input circuit converts the ac line voltage (either 115 or 230 vac) into rectified and

2.2.8 Switching Power Supply (Cont.)

filtered high voltage dc. The high voltage dc is chopped at a frequency of 25 KHz by a pulse width modulator presenting high voltage pulsating dc to a multiple output transformer. This transformer steps down the high voltage pulsating dc.

All output voltages are full-wave rectified through their associated diode rectifier circuits. The power-on reset signal (WOLFTRAP) is an output of a comparator circuit that forward-biases a NPN transistor once the output voltages are stabilized.

Two voltages are adjustable; +5 and +12 volts. The voltage adjustment pots are accessible from the outside of the power supply enclosure. Refer to Chapter 5 of this document for adjustment procedures and voltage measurement locations.

WARNING

Do not open the switching power supply under any circumstance. Extremely dangerous voltage and current levels (in excess of 300 volts DC and unlimited current) are present within the power supply.

Do not attempt to repair the switching power supply; it is field replaceable only.

After powering the unit down and disconnecting the AC power connector from the power source receptacle, allow one minute before removing the power supply to provide adequate time for any residual voltage to drain through the bleeder resistors.
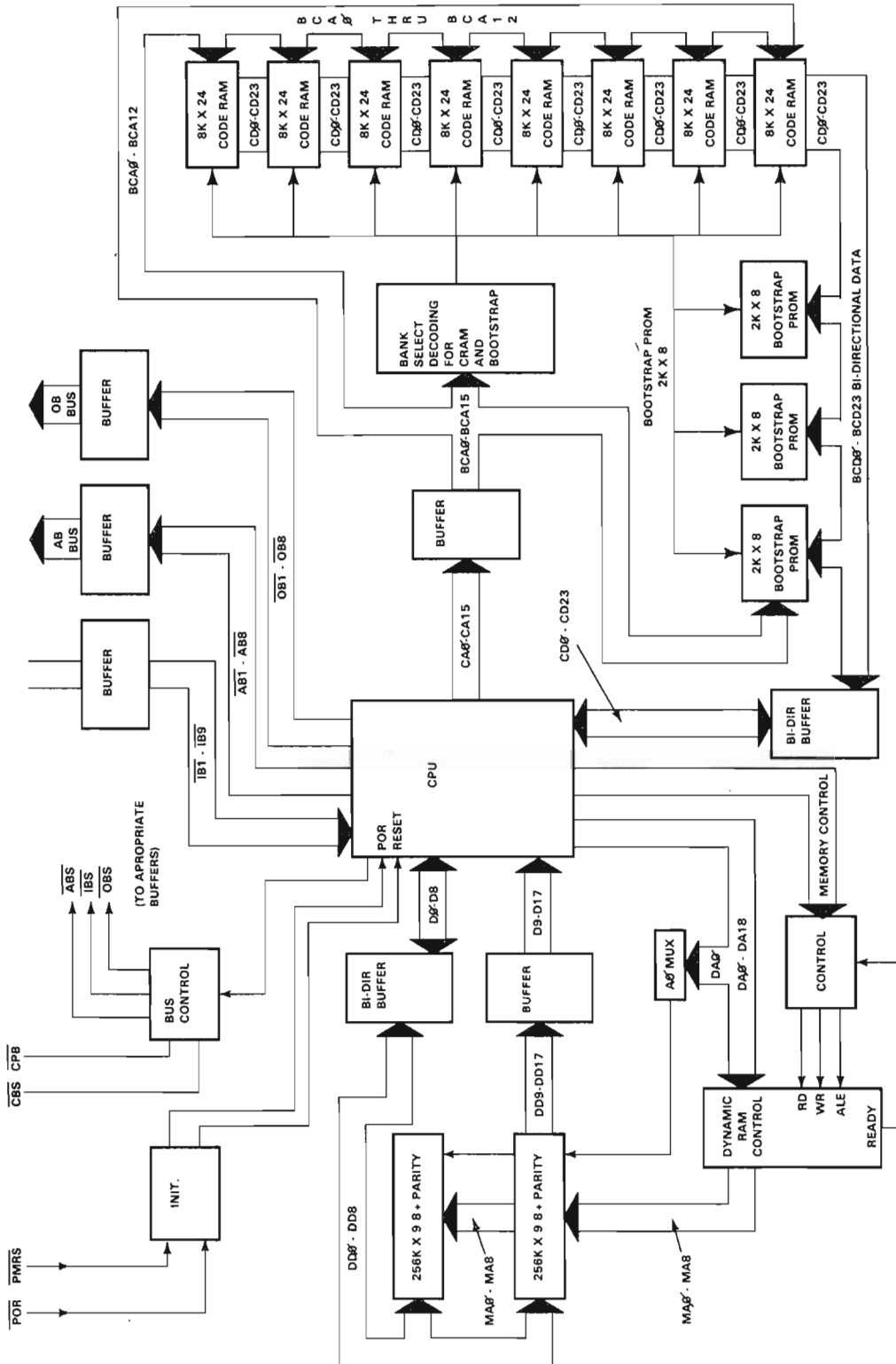
Figure 2-3   CPU/Memory Bd. Block Diagram

CHAPTER 3

OPERATION

3.1 SCOPE

This Chapter outlines the operation of the Micro VP-1 and Micro VP-2 Computer Systems. Included in this chapter are the daily-turn on and normal and emergency shut-down procedures.

3.2 CONTROLS AND INDICATORS

3.2.1 Power On/Off

The ac power On/Off switch is mounted on the side of the Micro VP cabinet. (Ref. Fig. 3-1.)

B-02381-FY85-5

AC POWER
ON/OFF
SWITCH
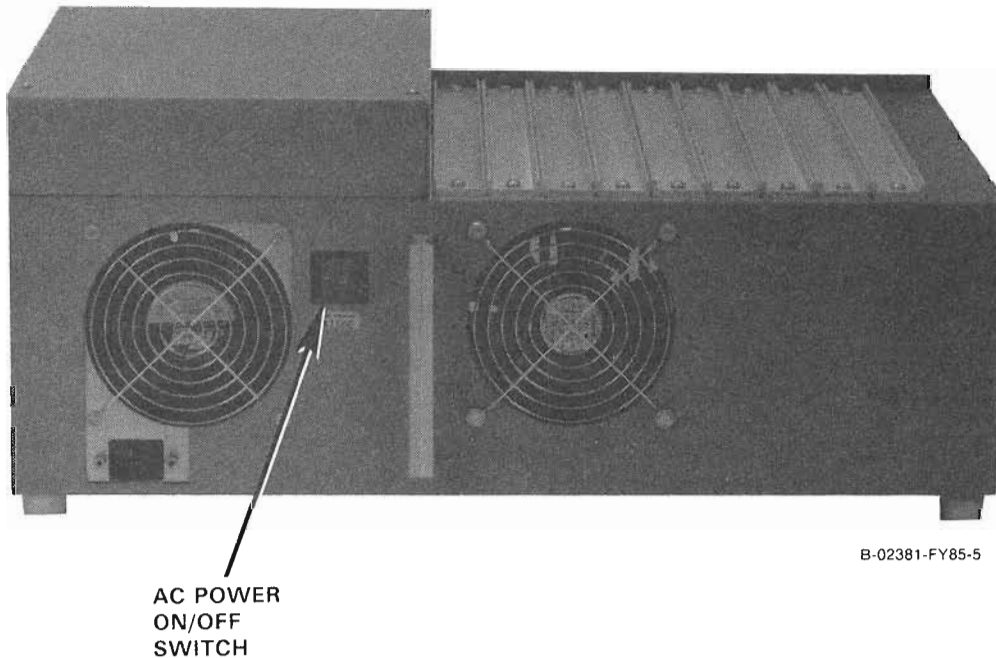
Figure 3-1 AC Power On/Off Switch

3.3 INITIAL POWER-ON PROCEDURE

1.   Remove the covers from the Micro VP. (Ref. Chapter 5).
2.   Ensure that the 120/240 ac voltage switch is set correctly.
3.   Ensure that all boards are seated properly in the motherboard.
4.   Plug the unit in and depress the ac power switch to the "1" position.
5.   Check voltages and adjust if necessary as outlined in Chapter 5 of this document.
6.   Remove power from the system, and replace covers.

3.4 DAILY POWER-ON PROCEDURE

1.   Whenever powering on the CPU and accociated peripherals, always Apply power first to terminal 1, then to the Micro VP, and finally the system disk.

3.5 NORMAL POWER-DOWN PROCEDURE

1.   Ensure that all users have logged off the system.
2.   Remove power from the system disk and any other drives configured into the system.
3.   Depress the ac power On/Off switch to the "0" position.

3.6 EMERGENCY POWER-DOWN PROCEDURE

1.   Depress the ac power On/Off switch to the "0" position.
2.   Remove ac plug from the power recepticle.

CHAPTER 4

INSTALLATION

4.1 SCOPE

This chapter describes the procedures for unpacking, inspecting, and installing the Micro VP Computer System. Included in this chapter are instructions for system interconnection and power-up. Actual installation should not begin until all site requirements detailed in the Customer Site Planning Guide (700-5978), and System Installation Guide (729-0907), have been met.

4.2 INSTALLATION SITE CHECK

The following conditions must be met prior to installation:

1. All site plans must have been approved by both the customer and a Wang service representative.
2. All building alterations must have been completed and inspected.
3. All electrical wiring, air conditioning, and telecommunications modifications must have been installed and tested.
4. The CE will perform a preinstallation inspection two weeks prior to delivery. At this time, the CE will check the site for compliance with Micro VP site specifications. The CE will bring any unsatisfactory condition noted to the attention of the customer for correction.

4.3 UNPACKING AND INSPECTION

Each peripheral device has its own unpacking and inspection procedures. Refer to section 1.2 of this document for applicable documentation.

1. Before unpacking any equipment, check all packing slips to make sure that the proper equipment has been delivered. After checking packing slips, inspect all shipping containers for damage (crushed corners, punctures, etc.).

2. If damage is discovered during inspection, file an appropriate claim promptly with the carrier involved, and Wang Laboratories, Inc.

3. Remove the Micro VP from its shipping container. Remove the outer covers
    as outlined in Chapter 5. Inspect the unit for damaged or loosened
    assemblies. Also check for loose hardware. Be certain that each PC board
    is in its proper location and fully seated. Insure that the 120/230 volt
    switch is in its proper position. (Ref. Fig. 4-1)

120/240
AC VOLTAGE
SWITCH

115V
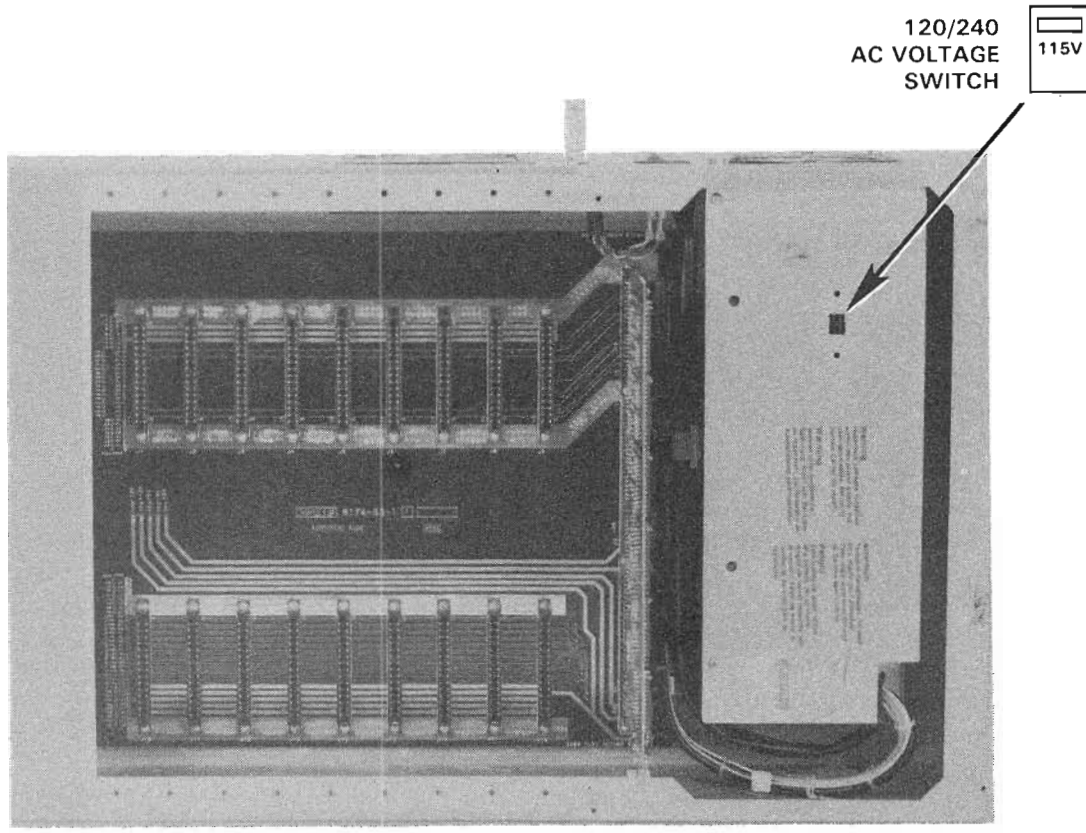
B-02381-FY85-8

Figure 4-1   120/240 AC Voltage Switch

4.4   INSTALLATION

1.   Assemble all peripherals as required for the system configuration. Refer
     to the applicable maintenance manual for each peripheral.

4.4.1   Switch Settings

1.   Each peripheral device must be assigned a unique address as specified in
     Table 4-1. A configuration with one device in a class will use the first
     device address for that class. Additional devices belonging to that class
     will have addresses sequentially assigned. Refer to Table 4-1 and assign a
     device address for each peripheral to be configured into the system.

Device	Address(es)
Keyboards	001, 002, 003, 004
CRT Units	005, 006, 007, 008
A.C. Tape Drive	018
Tape Cassette Units	10A, 10B, 10C, 10D, 10E, 10F
Printers	215, 216
Disk Units	310, 320, 330
Card Reader	517
Hopper-Feed Card Readers	628, 629
Paper Tape Readers	618
Teletype	019, 01A, 01B
	Input: 01D, 01E, 01F Output
Teletype Tape Units	41D, 41E, 41F
Telecommunications Output	219, 21A, 21B
	Input: 21D
	Output: 21E, 21F
Parallel I/O Interface	23A, 23C, 23E,
	Input: 23B,
	Output: 23D, 23F
BCD Input Interface	25A, 25B, 25C, 25D, 25E, 25F
Nine-Track Tape Unit	07B, 07D, 07F
Triple Controller	001, 005, 009, 013 (Workstation)
	310, 320, 330 (Disk)
	215, 216, 217 (Printer)

Table 4-1   Typical Device Addressing

2.   Once an address has been assigned to each peripheral, the addresses must be
     inserted into the address switches located on each device controller board.

3.   The most significant digit of the device address is used by the Operating
     System to identify the device type. It is not used in the device-address
     switch settings.

4.   The last two digits of the device address correspond to the actual unit's
     address which must be set on each device controller board in the Micro VP.
     These digits must be broken down into binary bits and these bits are selected
     using the appropriate switch. (Ref Fig. 4-2 and Table 4-2.)

ADDRESS SETTING ON PERIPHERAL DEVICE I/O CONTROLLER BOARDS
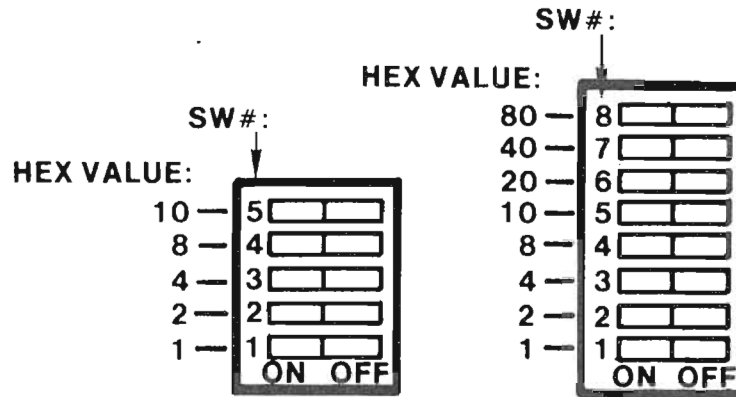
B-02381-FY85-9

Figure 4-2   Device Address Switches

Switch Numbers

Digit (Hex)	Second Digit				Last Digit			
	8	7	6	5	4	3	2	1
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	0	1	1	1
8	1	0	0	0	1	0	0	0
9	1	0	0	1	1	0	0	1
A	1	0	1	0	1	0	1	0
B	1	0	1	1	1	0	1	1
C	1	1	0	0	1	1	0	0
D	1	1	0	1	1	1	0	1
E	1	1	1	0	1	1	1	0
F	1	1	1	1	1	1	1	1

Table 4-2   Device Address Switch Setting

For example, when inserting an printer address of 215, switches 5, 3, and 1 would be set to ON.

5. Other switch settings (baud rate, etc.) may be required depending on the I/O Controllers installed in the Micro VP. Some examples of these are as follows;

MXD MULTIPLEXER DEVICE ADDRESS AND BAUD-RATE SWITCHES

CONNECTOR FOR TERMINAL #1

7290-1 BOARD

1	9600
2	4800
3	2400
4	1200
5	600
6	300
7	9600
8	4800

#1

19.2K
L 19   L 18
4800
JUMPER

J6

#2

1	2400
2	1200
3	600
4	300
5	9600
6	4800
7	2400
8	1200

BAUD RATE SWITCHES

DEVICE ADDRESS SWITCHES

#3

1	600
2	300
3	9600
4	4800
5	2400
6	1200
7	600
8	300

#4

NOT USED   80   40

ON

NUMBER OF MXDS
1st 80,40 OFF
2nd 80 (OFF) 40 (ON)
3rd 80 (ON) 40 (OFF)
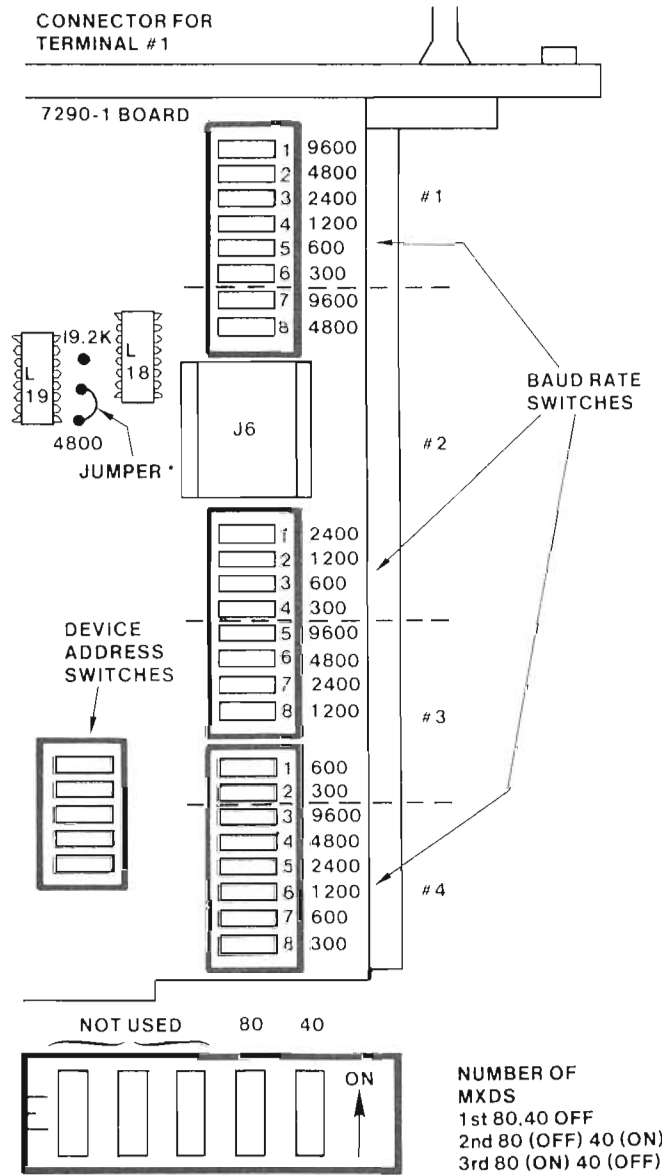
For 19.2K set switches to 4800 and jumper to 19.2K

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Fig. 4-3 MXD Multiplexer Device Address and Baud Rate Switches

Z80A
DART

L19   L18

SWITCH 1
DEVICE ADDRESS
(CONTROLLER NUMBER)

CONTROLLER #	SWITCH POSITIONS
1	ALL SWITCHES OFF
2	SWITCH ONE ON ONLY
3	SWITCH TWO ON ONLY

L45   L44

Z80A
CTC

MXE MOTHER PCB 210-7874

SWITCH 3
PORTS 1 & 2
BAUD RATE

SWITCH 2
PORTS 3 & 4
BAUD RATE
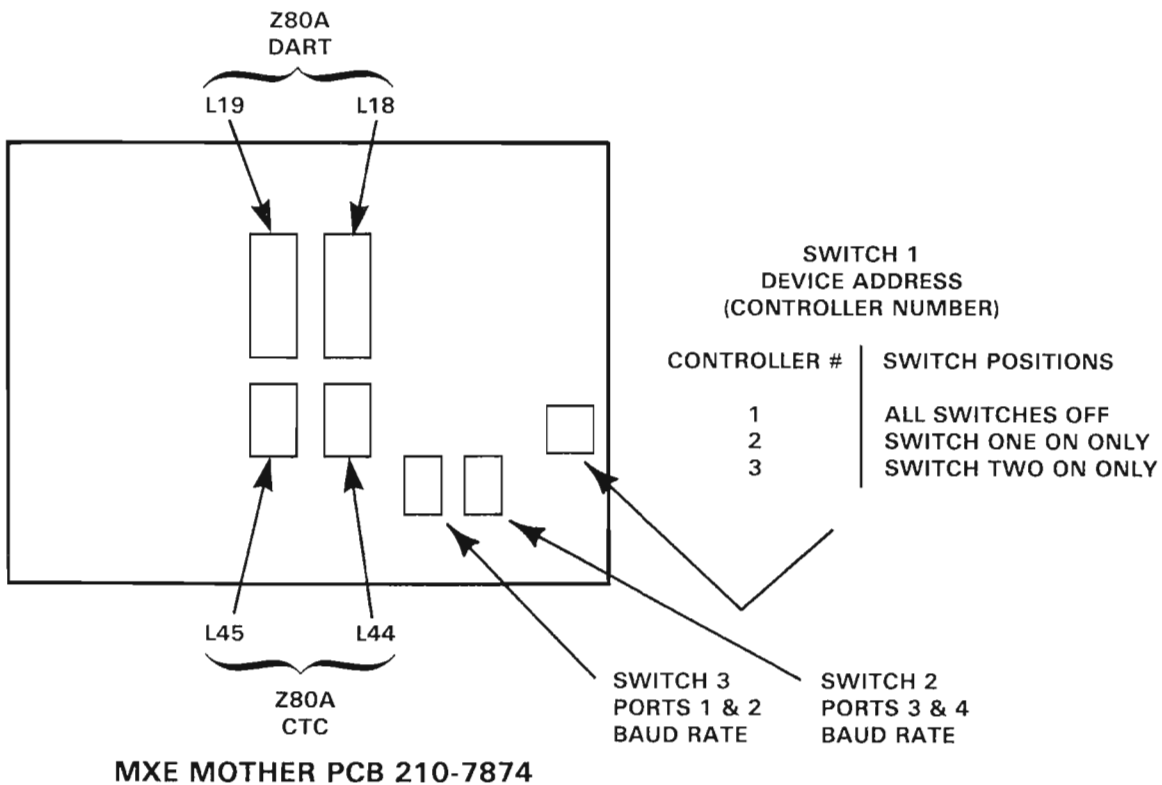
B-02381-FY85-27

Fig. 4-4   MXE Multiplexer Device Address and Baud Rate Switches

MXE HARDWARE SWITCH SETTINGS

Baud Rate	|Switch 3 Port 1| 1	2	3	4	Port 2 5	6	7	8	Switch 2 Port 3 1	2	3	4	Port 4 5	6	7	8
110	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
134.5	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
150	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
200	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
300	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
600	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF
1200	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF
2400	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
4800	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON
9600	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON
19600	ON	OFF	ON	ON	ON	OFF	ON	ON	ON	OFF	ON	ON	ON	OFF	ON	ON

SWITCH 3
TERMINAL ADDRESS

TERMINAL	SWITCH POSITIONS
1	SWITCH ONE ON ONLY
5	SWITCH ONE AND FOUR ON
9	SWITCH ONE AND FIVE ON
13	SWITCH ONE, FOUR, AND FIVE ON

SWITCH 2
PRINTER ADDRESS*

SWITCH 1
DISK ADDRESS*
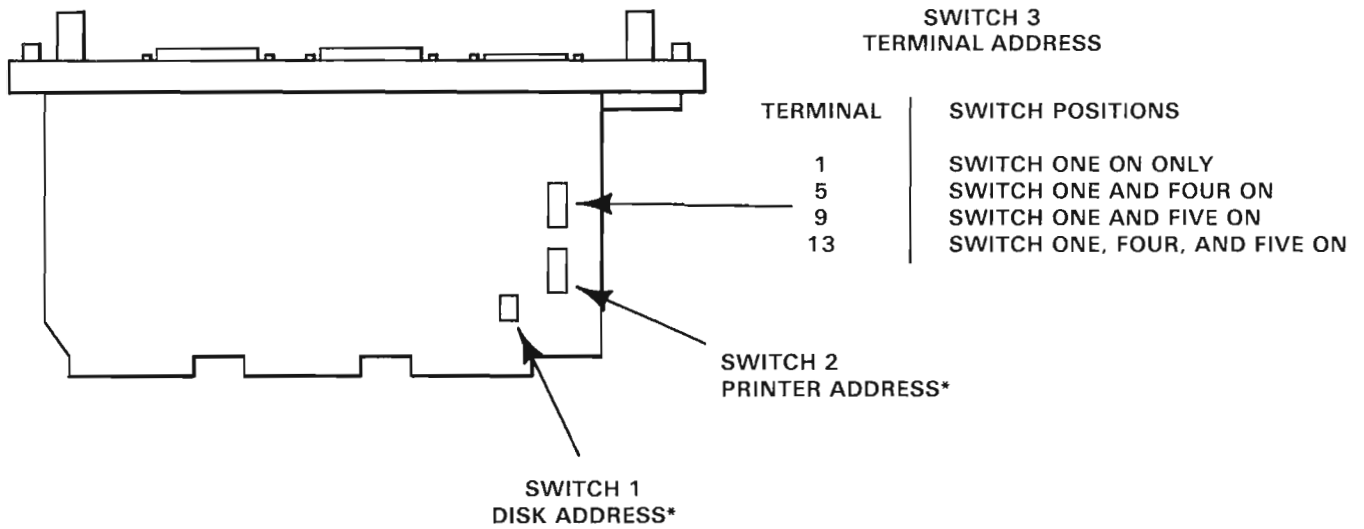
*SWITCH SETTINGS ARE IDENTICAL TO NORMAL HARDWARE
SWITCH SETTINGS (REF. FIG. 4-2).

B-02381-FY85-28

Fig. 4-5   22C32 Triple Controller Switches

4.4.2 Cabling

1. Exact system cabling will differ with each system configuration. Below are some examples of the cabling required for typical configurations.

Printer Interface

CONTROLLER BUFFERS	Cable	Device
22C01;210-6561 J1	220-0181 120-2201-25(25' EXT.) 120-2201-50(50' EXT.)	2201L CHARACTER PRINTER
22C02;210-7079 J1 (22C11;210-7042-2) J2) (22C11;210-7342) J1)	220-105-3 120-2225-25(25' EXT.) 120-2225-50(50' EXT.)	2221W MATRIX PRINTER 120 CPS
SAME AS 2221W	220-0105-1 EXT. SAME AS 2221W	2231W MATRIX PRINTER 120 CPS
SAME AS 2221W	220-0156 EXT. SAME AS 2221W	2251 MATRIX PRINTER 110 CPS
SAME AS 2221W	220-0171 EXT. SAME AS 2221W	2261W MATRIX PRINTER 240 LPM
SAME AS 2221W	220-0105-3 EXT. SAME AS 2221W	2263 CHAIN PRINTER 400/600 LPM
SAME AS 2221W	220-0156 EXT. SAME AS 2221W	2271/2271P BI-DIRECTIONAL WRITER/PLOTTER 15 CPS
SAME AS 2221W	220-0161 EXT. SAME AS 2221W	2281/2281P DAISY WRITER/ PLOTTER 30CPS
SAME AS 2221W 2231W-3	220-0105-3 EXT. SAME AS 2221W	2282 GRAPHIC CRT PLOTTER
	220-0105-3 EXT. SAME AS 2221W	PRINTER MATRIX/ PLOTTER 120 CPS

Fig. 4-6 Printer Interface Cabling

CONTROLLERS

22C03;210-6541-2   J1   220-0066-4   2270A-1D,-2D,-3D
(22C11;210-7042-2   J3   NO EXT. CABLE   IBM COMPATIBLE
(22C11;210-7342)   J2   DISKETTE DRIVE

22C03;210-6541-2   J1   220-0066   2260B, 1/4, 1/2   220-0151   2260B
(22C11;210-7042-2) J3   NO EXT. CABLE   10, 2.5, 5 MEG.   NO EXT.   10 MEG
(22C11;210-7342)   J2   DISK DRIVE   CABLE   DISK DRIVE
                                                                     (2260BC-2   (2260B-2 ONLY)
                                                                     ONLY)
22C1Z;212-2260C,C1,CZ J1 220-0188   2260C, 1/4, 1/2   220-0187   2260C
                       J2 NO EXT. CABLE 10, 2.5, 5, MEG.   NO EXT.   10 MEG
                                          DISK DRIVE   CABLE   DISK DRIVE
                                                                     (2260C-2   (2260C-2 ONLY)
                                                                     ONLY)
22C13;212-2260C3,C4,C5 J1 220-0188   2260BC, 1/4, 1/2,   220-0187   2260BC
                        J2 NO EXT. CABLE 10, 2.5, 5, MEG.   NO EXT.   10 MEG
                            (220-0169 FOR (DISK DRIVE)   CABLE   DISK DRIVE
                            2260C-2)   (2260BC-2   (2260 BC-2 ONLY)
                                                                     ONLY)
22C03;210-6541-2   J1 J3   "B" CABLE   "B" CABLE
(22C11;210-7042-2) J3   220-3066   220-3033-36   3033-36
(22C11;210-7342)   J2
(210-7287)   J1)
22C03;210-6541-2   J1   220-0105-2   2280   2280-1, -2, -3,   2280-3
(22C11;210-7042-2) J3)   NO EXT. CABLE   MICROPROC.   27, 54, 81 MEG.   81 MEG.
(22C11;210-7342   J2)   CARTRIDGE   CARTRIDGE
                                          220-3041-22 "A" CABLE   DISK DRIVE   DISK DRIVE

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Fig. 4-7 Disk Interface Cabling

BUFFERS
177-2227B
(177-2228B)
(177-2228C)

J1 | 220-0113 (12')
220-0219 (25')
220-0220 (50')
120-2227-25 (25' EXT.)
120-2228-50 (50' EXT.)

BELL MODEM/
NULL MODEM
177-2227N
177-2228N

9 TRACK
TAPE CONTROLLER
212-2209A

J1
J2 | 220-0168
NO EXT. CABLE

2209A
9 TRACK
TAPE DRIVE
1600 BP1

BUFFER
22C01;210-6561

J1 | 220-0178

2232B
PLOTTER
CONTROLLER

220-01792

2232B
LARGE
FLATBED
PLOTTER

CONTROLLER

22C0Z;210-7079
(22C11;210-7042-2
(22C11;210-7342

J1
J2 | 220-0146
J1) | 120-2225-25 (25' EXT.)
120-2225-50 (50' EXT.)

2272-2
DRUM
PLOTTER

MULTIPLEXER
177-3236-1

J1 | 120-2236-25 (25')
120-2236-50 (50')
120-2236-(1-10) FOR
100' TO 1000'

2236D
INTERACTIVE
TERMINAL

MULTIPLEXER
177-3236-1

J1 | 220-0113 (12')
220-0219 (25')
220-0220 (50')
120-2227-25 (25' EXT.)
120-2227-50 (50' EXT.)

BELL
MODEM

BELL
MODEM

220-0113 (12')
220-0219 (25')
220-0220 (50')
120-2227-25 (25' EXT.)
120-2227-50 (50' EXT)

2236D
INTERACTIVE
TERMINAL

B-02381-FY85-12

Fig. 4-8 Telecommunications, Tapes, Plotters, and Terminal Interface Cabling

Fig. 4-9 Multiplexer Cabling

4.5 INITIAL POWER-UP

1. With the covers removed from the system (ref. chapter 5), ensure that the 120/240 ac line voltage switch is set correctly. (Ref. Fig. 4-9).

2. Ensure that the CPU/Memory Bd. is seated properly in slot 1 and all I/O controllers are fully seated in the motherboard.

3. Apply power to terminal 1, the Micro VP, and finally the system disk.

4. Check operating voltages and adjust if necessary as outlined in Chapter 5.

5. With the operating voltages set, replace all system covers. (Ref. chapter 5).
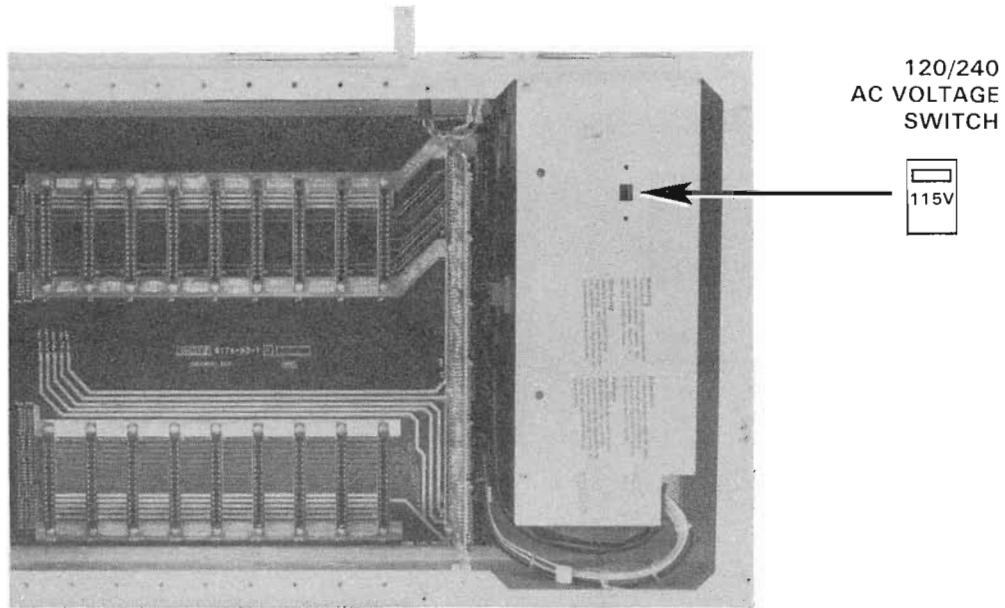
120/240
AC VOLTAGE
SWITCH

115V

Fig. 4-10 120/230 AC Line Voltage Select Switch

NOTE

Operating voltages must be checked and adjusted if
necessary on all peripherals attached to the
system. Please refer to the appropriate
maintenance manual (section 1.2) for detailed
instructions on checking and adjusting these
voltages.

4.6 SYSTEM VERIFICATION

4.6.1 System Diagnostics

1.   Once power has been applied, the terminal connected as workstation 0
     should be displaying the following screen;

        MOUNT SYSTEM PLATTER
        PRESS RESET

2.   Place the System Platter Disk into the system drive and press the RESET
     key on the keyboard. (Press RESET if the terminal is model #2336DE, and
     SHIFT RESET if the terminal is model #2336DW.)

3.   The following screen should now be displayed;

```
/ ‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾
|
|    KEY SF'?
|
|
```

4.   Depress the special function key which corresponds to the drive you wish
     to IPL from. Disk addresses start with SF'00 and increment thereafter.
     For example; SF'00 accesses a disk address of 310, SF'01 an address of
     B10, SF'02 an address of 320, SF'03 an address of B20, etc.

5.   The screen should display;

```
/ ‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾
|
|                      ****SYSTEM 2200****
|
| Select item with SPACE & BACKSPACE                       MEMORY XXXXK
| Key RUN to execute, CLEAR or PREV SCRN for previous screen   Terminal X
|
|
|
|                    ■  MVP BASIC-2
|                    _  Diagnostics
```

6.   Space down to Diagnostic and key RUN. The screen will appear as follows;

```
/ ‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾
|
|                ****CUSTOMER DIAGNOSTIC MENU****
|
| Select item with SPACE & BACKSPACE                       MEMORY XXXXK
| Key RUN to execute, CLEAR or PREV SCRN for previous screen   Terminal X
|
|
|                    ■  CPU Instructions
|                    _  Control Memory
|                    _  Data Memory
|                    _  CPU Registers
|
|                    _  All of the above
```

7. Space down to All of the above and key RUN. The diagnostics will begin immediatly. As each set of tests are completed the Chain Mode Pass will increment. These tests will run continuously until RESET is keyed to terminate the diagnostics.

NOTE

Please refer to Chapter 7 of this document for interpretations of all CPU diagnostics mentioned here.

8. When a sufficient number of successful test passes have occured (5 to 10 passes), key RESET.

9. The system software must now be configured to support the attached peripherals.

4.7 PARTITION GENERATION

1. After all required system diagnostics have successfully completed the partitions must be generated. Apply power to the system or key RESET. The screen will appear as follows;

```
MOUNT SYSTEM PLATTER
PRESS RESET
```

3. Mount the system disk and press RESET. The screen appears;

```
KEY SF'?
```

4. Depress the special function key which corresponds to the drive containing the operating system. Disk addresses start with SF'00 and increment thereafter. For example; SF'00 accesses a disk address of 310, SF'01 an address of B10, SF'02 an address of 320, SF'03 an address of B20, etc.

NOTE

If the wrong SF key was depressed (there was no system disk at the device specified), the following screen will appear;

```
***SYSTEM ERROR (DISK 00XX)***

PRESS RESET
```

If this error occurs, press RESET, then the correct SF key.

5.   The screen will now appear:

```
                        ****SYSTEM 2200****

Select item with SPACE & BACKSPACE                    MEMORY xxxxK
Key RUN to execute, CLEAR or PREV SCRN for previous screen     Terminal X



                        ■  MVP BASIC-2
                        _  Diagnostics
```

6. Select MVP BASIC-2 and key RUN. The following screens will now appear:

```
        LOADING:  MVP BASIC-2 RELEASE X.X
```

```
                    ***WANG 2200MVP PARTITION GENERATION PROGRAM***

LIST OF STORED CONFIGURATIONS    (# PARTITIONS)
     1.   current                    (X)              LIST OF OPTIONS
     2.   ...                                     SF'00 - CLEAR PARTITIONS
                                                  SF'01 - CLEAR DEVICE TABLE

                                                  SF'02 - DIVIDE MEM. EVENLY

                                                  SF'04 - EDIT PARTITIONS
                                                  SF'05 - EDIT DEVICE TABLE
                                                  SF'06 - EDIT $MSG

                                                  SF'08 - LOAD CONFIGURATION
                                                  SF'09 - SAVE CONFIGURATION
                                                  SF'10 - DELETE CONFIGURATION

                                                  SF'15 - EXECUTE
                                                     FN - HELP


CONFIGURATION "CURRENT" LOADED.   NAME OF CONFIGURATION TO LOAD?  _____
```

7. Configuration parameters must now be entered into the Operating System. If partition-generation modules have been previously defined, a list of those module names will appear in the @GENPART menu screen. The user can select and load one of these modules by typing in the name of the module and pressing RETURN, and SF'15. If the user wishes to define a new partition module, he can do so by depressing the appropriate Special Function keys. This will initiate partition generation.

        Descriptions of @GENPART SF Key Options:

SF'00 – Clear Partitions: Clears partition configuration parameters currently in memory, allowing the user to specify the total number of terminals and partitions in each bank, then automatically advances to SF'04 (Edit Partitions). Any number of partitions between 1 and 16 is allowable.

SF'01 – Clear Device Table: Clears Master Device Table parameters currently stored in memory, resets the default peripheral addresses to 215 (printer), 310 (system disk), and 320 (secondary disk), allocates these devices to all users, then advances to SF'05 (Edit Device Table). Default device addresses can then be edited.

SF'02 – Divide Memory Evenly: Divides remaining User Memory equally among the number of partitions specified with SF'04.

SF'04 – Edit Partitions: Displays and allows editing of partition parameters such as size, terminal assignment, programmability, and name of bootstrap program. SF'04 does not allow addition or deletion of defined partitions in an existing configuration.

SF'05 – Edit Device Table: Displays and allows editing of device addresses for all peripherals. All peripherals connected directly to I/O controllers must be specified in the Master Device Table.

SF'06 – Edit $MSG: Displays and allows editing of a user-defined broadcast message that will be displayed on each terminal's CRT whenever the READY message is displayed. This message appears on line 0 of the CRT, immediately above the READY message.

SF'08 – Load Configuration: Loads a named configuration from the Configuration File, which is located on the system disk. To modify and/or execute any previously defined configuration other than "current", this option must be used.

SF'09 – Save Configuration: Used to save a system configuration in the Configuration File under a user-specified name (up to eight characters in length). If the user specifies a configuration name already used, @GENPART will verify that the user desires to replace the old configuration on disk file with the configuration currently in memory.

SF'10 – Delete Configuration: Deletes a configuration from the Configuration File on the System Disk.

SF'15 – Execute Configuration: Allows the operator to first review, and then to execute, a configuration. This configuration will automatically be saved in the Configuration File under the name "current" when the configuration is executed. Once a configuration has been executed, the system may be reconfigured again only after the Master Initialization procedure has been repeated.

FN – Help: Displays @GENPART operating instructions.

In general, the order of executing these @GENPART options is as follows;

1. SF'08 – to load a configuration
2. SF'00 – to modify this configuration by adding or deleting partitions
3. SF'04 – to create the new partition parameters
4. SF'05 – to create the Master Device Table
5. SF'06 – to create the broadcast message
6. SF'09 – to save the configuration with a name other than "current"
7. SF'15 – to execute the configuration

These steps will create a permanent system configuration.

The following section outlines the screen loads given when in @GENPART

Load a Configuration (SF'08)

```
    LIST OF STORED CONFIGURATION (#PARTITIONS)
              current              (1)

CONFIGURATION 'current' LOADED. NAME OF CONFIGURATION TO LOAD? _____
```

The last configuration executed (called 'current') is automatically loaded. To load any other configuration, enter its name, then press RETURN.

Clear Partitions (SF'00)

```
        AVAILABLE USER MEMORY = xxK
        REMAINING USER MEMORY = xxK
        NO. OF TERMINALS?
        NO. OF PARTITIONS?
```

The program responds with a display that requests the total number of terminals that are to be configured into the system and the number of partitions that will be created. Available User Memory is automatically calculated and displayed. Remaining memory is updated and displayed as memory is allocated to the partitions. When all information has been entered, and RETURN is pressed, the program automatically invokes SF'04 (Edit Partition) to allow the editing of partition parameters.

Edit Partitions (SF'04)

```
PARTITION SIZE (K)        TERMINAL     PROGRAMMABLE PROGRAM
    1      _____            1           Y
    2      _____            2           Y
    3      _____            3           Y
    4      _____            4           Y


EDIT WHICH PARTITION (DEFAULT = 1)?
```

This option displays parameters for all partitions and initiates a cycle of prompts for the altering of these parameters. The cycle recurs until another option is selected. The user is thus allowed to modify parameters for each partition. The display is updated each time an item is entered.

For example to enter parameters for partition #2, enter 2 then key RETURN.
An asterisk appears beside the number of the partition whose parameters are
being edited, and the following series of prompts will be displayed in
succession at the bottom of the screen:

PARTITION SIZE (default = 0)

Any value greater than 1.25K and less than the amount of remaining User
Memory is a valid response. Note that the default value is not a valid
response unless all remaining user memory is to be divided evenly. After the
amount of user memory allocated to this partition has been entered, the screen
will appear;

TERMINAL (default = 2)?

Enter the terminal number which will be assigned to this partition. The
following screen will appear;

ENABLE PROGRAMMING (Y or N)?

By default, programming is allowed for all partitions; however, to prevent
inadvertant modification of certain programs, it may be desirable to disable
the programming mode in some partitions. After responding to this prompt, the
name of a program to be automatically loaded into this partition will now be
requested. The screen appears as follows;

NAME OF PROGRAM TO LOAD?

Enter the name of the program and key RETURN. When the configuration is
executed, the program will be automatically loaded from the system disk into
its' partition, and will then be run.

Other partitions which require modification may be serviced at this time
following the same procedure. Once all partitions have been edited (if
necessary), SF'05 is used to leave the "Edit Partition" cycle and invoke the
"Edit Master Device Table" option. With this option selected, the screen will
appear as follows;

DEVICE	PARTITION	DEVICE	PARTITION
1.	/215	all	17.
2.	/310	all	18.
3.	/320	all	19.
.			.
.			.
.			.
16.			32.

EDIT WHICH ENTRY (default = 1)?

Enter the device number of the item you wish to edit. An asterisk (*) will appear next to the device number selected. The screen appears as follows;

DEVICE ADDRESS (default = /000,/000 to delete entry)?

Enter the device address, then RETURN. The screen now appears;

ALLOCATE DEVICE TO WHICH PARTITION (default = all)?

Enter the partition number to allocate the peripheral and its controller. These screens will continue, in order to allow the user to edit all entries in the Master Device Table. When the parameters for all peripheral/partition allocations have been specified, the user can select another Special Function option to exit the "Edit Device Table" mode.

Broadcast Message (SF'06) When SF'06 is depressed, the following display appears at the bottom of the screen;

BROADCAST MESSAGE:

You may now enter a broadcast message. While in the broadcast message mode, all S.F. keys revert to their system defined EDIT functions. The S.F. keys cannot be used for any @GENPART function until the entry of the broadcast message is complete.

Save Configuration (SF'09) When SF'09 is depressed, the following display appears at the bottom of the screen;

CHECK CONFIGURATION TO SAVE. CONFIGURATION NAME? ----------------------

To save a configuration, ensure that the system diskette or hard disk is write-enabled, enter a unique name for the configuration, and key RETURN. The configuration currently in memory will automatically be saved under the name 'current'. However, each time a new configuration is executed, the new parameters replace the old parameters in the 'current' file.

Execute Configuration (SF'15) Once all parameters of a configuration have been defined, the system configuration can be executed. When SF'15 is depressed the configuration table will appear at the bottom of the screen, along with a prompt requesting the operator to verify the configuration parameters to be executed.

CHECK CONFIGURATION OK TO EXECUTE (Y or N)?

If Y (RETURN) is chosen, the configuration will be executed. If N (RETURN) is entered, the system returns to the beginning of the "Edit Partition" cycle. Once executed, a configuration can only be changed by first Master Initializing the system, and then, by specifying the new parameters.

Delete a Configuration (SF'10) When this is depressed, the following prompt will request which configuration to delete;

DELETE WHICH CONFIGURATION?

Enter the name of the configuration to be deleted, then RETURN. The configuration will be deleted from the system disk.

4.8 GENERATING EVENLY-DIVIDED PARTITIONS

To generate evenly-divided partitions, first load the BASIC-2 operating system by keying in the appropriate SF' key on terminal 1. Next, key SF'00 to initialize all terminals and clear the partitions. The prompt "NO. OF TERMINALS?" refers to the number in each bank of user memory. Answer this prompt with the number of terminals attached, then answer the "NO. OF PARTITIONS?" with the same number, then key EXECUTE. Now key SF'02 to divide memory evenly in each bank. Available memory will now be apportioned equally among the number of terminals entered earlier. Finally, key SF'15 to execute the configuration. A prompt will appear "CHECK CONFIGURATION. OK TO EXECUTE (Y or N)?". Enter Y and key EXECUTE if the configuration is correct. All terminals should now display "READY (BASIC-2)". Each terminal can now be used as an independent processor.

4.9 CUSTOMIZING PARTITION GENERATION

The user may write his own partition generation utility if he desires. Directions for this are given in the BASIC-2 Language Reference Manual.

4.10 SYSTEM TURNOVER TO CUSTOMER

When all diagnostics required for system installation have been successfully completed, and the software has been correctly completed, the system can be turned over to the customer. To turn over the system to the customer;

1. Demonstrate to the customer or to the responsible computer operator the disk initialization procedure.
2. Perform the Daily Power-Down procedure (ref. section 3.4), and explain each step to the applicable customer personnel.
3. Perform the Daily Power-Up procedure (ref. section 3.5), and explain each step to the applicable customer personnel.
4. Allow the customer to test the system using his programs. If the customer is satisfied with the operation of the system, officially turn the system over to the customer. This should be a verbal notification given by the CE performing the installation.

CHAPTER 5

PREVENTIVE MAINTENANCE

5.1 SCOPE

This chapter contains preventive maintenance, adjustment/alignment, and removal/replacement procedures for the Micro VP-1 and Micro VP-2 Computer Systems. This document only provides information for the maintenance of the CPU systems themselves. Maintenance for attached peripherals is documented in the appropriate product manual(s).

5.2 SPECIAL TOOLS AND EQUIPMENT

No special tools or equipment are required for maintaining the Micro VP Computer Systems.

5.3 MAINTENANCE PROCEDURES

To ensure proper operation, the Micro VP must have periodic preventive maintenance consisting of inspection, cleaning, and adjustments. The following preventive maintenance procedures should be performed in conjunction with the preventive maintenance done to the system disk drive. This assumes a clean operating environment and normal operating time of 40 hours per week. A dusty environment or a substantial increase in the operating time will require that these preventive maintenance procedures be carried out more frequently. In addition, these procedures should be performed during each unscheduled service call.

5.3.1 Central Processing Unit

The following procedure should be followed for the Preventive Maintenance of the Micro VP CPU;

1.   Check the cooling fan for proper operation.
2.   Clean the unit as outlined below.
     a. Remove the top cover from the system.
     b. Remove the I/O controllers and the CPU/Memory board.
     c. Remove all dust from the interior of the unit.
     d. Clean the finger connectors of each PCB.
     e. Reinstall all PC boards into the system.
     f. Using a mild detergent and a soft cloth or sponge, clean the
        CPU cabinetry. Do not use abrasive or corrosive chemicals.
3.   Check the operating voltages and ripple as defined in Section 5.4
     of this document.
4.   Replace the top cover on the system and run diagnostics as
     required to ensure proper operation of the equipment.

5.4 ALIGNMENTS AND ADJUSTMENTS

5.4.1 Voltage Adjustments

1. Remove the top cover from the system.
2. Ensure that the 120/240 AC line voltage select switch is set properly.
3. Depress the ac-power switch to the "1" position.
4. Using a Fluke Digital Voltmeter or equivalent, check -5vdc, +5vdc, +12vdc, and -12vdc at TP2 through TP5, on the motherboard. TP0 may be used as a ground reference. (Ref. Fig. 5-1). Refer to table 5-1 for the correct operating voltage levels.
5. +5vdc an +12vdc are the only adjustable voltages. Refer to Fig. 5-1 and adjust these voltages as required to achieve the correct operating voltage levels.

IF NO BRDS PLUGGED INTO MBRD WHEN CHECK V'S, WILL READ LOW. 12V MAY READ 8V.

WARNING

> Do not open the switching power supply under any circumstance. Extremely dangerous voltage and current(in excess of 300 volts DC and unlimited current are present within the power supply.
>
> Do not attempt to repair the switching power supply; it is field replaceable only.
>
> After powering the unit down and disconnecting the AC power connector from the power source receptacle, allow one minute before removing the power supply to provide adequate time for any residual voltage to drain through the bleeder resistors.

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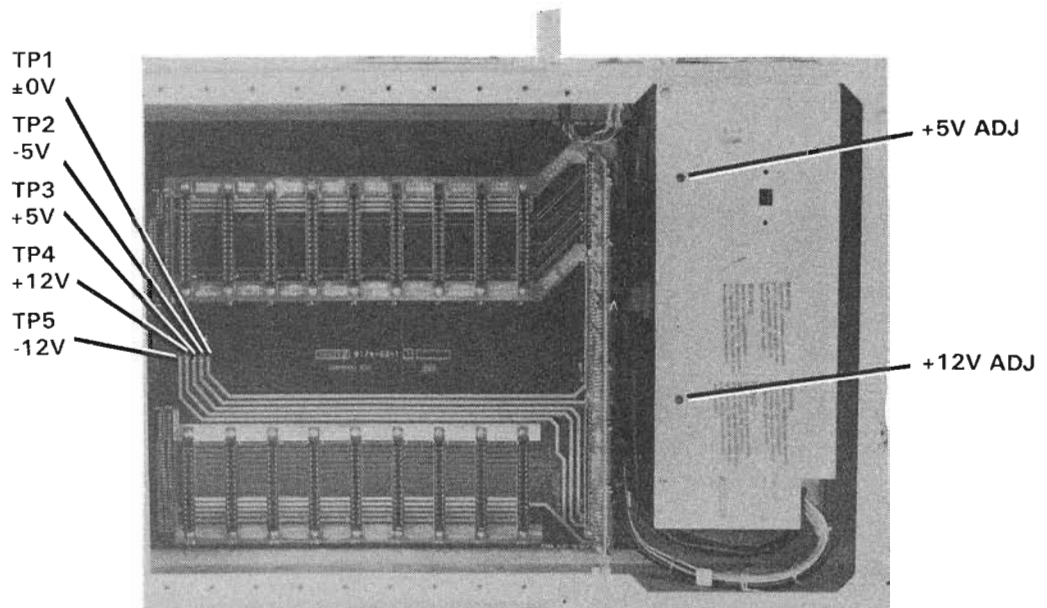
Fig. 5-1 Operating Voltage Testpoints

VOLTAGE	LIMITS	RIPPLE
+5vdc	+4.95vdc to +5.05vdc	15mv p-p
-5vdc	-4.95vdc to -5.05vdc	15mv p-p
+12vdc	+11.95vdc to +12.05vdc	15mv p-p
-12vdc	-11.95vdc to -12.05vdc	15mv p-p

Table 5-1 Operating Voltage Limits

If any voltage is missing or the +5 and/or +12 volts can not be adjusted, remove all PCB boards (ref. section 5.5 of this document) and perform the adjustment procedure again. If the voltage can be adjusted, one or more PCB is possibly causing the problem, however the power supply itself should not be ruled out. If a PCB is found to be at fault, replacement of the defective board is required.

If the voltage problem exists with no PCB boards installed, replacement of the Switching Power Supply is required. Refer to the Removal and Replacement procedure described in section 5.5.

5.5 REMOVAL AND REPLACEMENT PROCEDURES

5.5.1 Top Cover Removal

To remove the top cover of the Micro VP system;

1.   Remove 4 phillips-head screws on top cover (ref. Fig. 5-2).
2.   Carefully lift cover off the unit.

5.5.2 Top Cover Replacement

To replace the top cover of the Micro VP system;

1.   Place cover on unit.
2.   Insert 4 phillips-head screws and tighten.
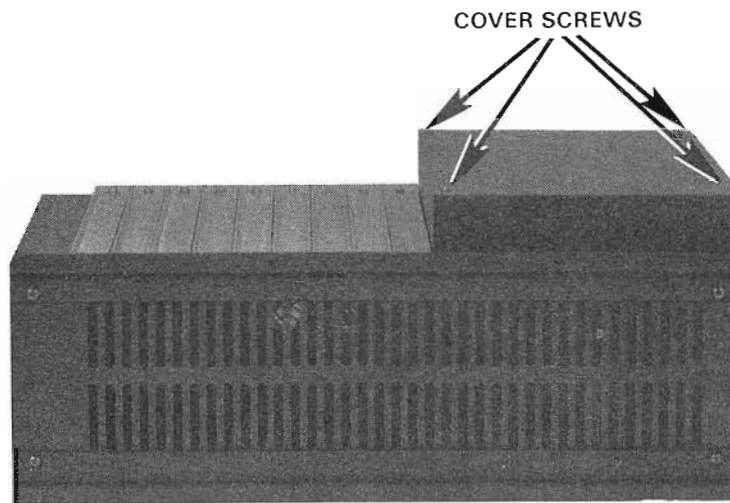
COVER SCREWS

B-02381-FY85-15

Figure 5-2   Top Cover Screws

5.5.3 Switching Power Supply Removal

To remove the Switching Power Supply from the Micro VP system;

1.   Depress the ac power on/off switch to the "0" position.
2.   Remove the ac plug from the power receptacle.
3.   Wait 1 minute for residual voltage to drain through the bleeder
     resisters. If top cover is installed on the system, remove it as
     described in Section 5.5.1.
4.   Remove the CPU/Memory Bd. from the system (Ref. section 5.5.5),
     and set it aside. Unplug connectors P22, P23, and P24 from the
     motherboard (Ref. Fig. 5-6).
5.   Remove the phillips head screw from the bottom of the system
     (Ref. Fig. 5-3).
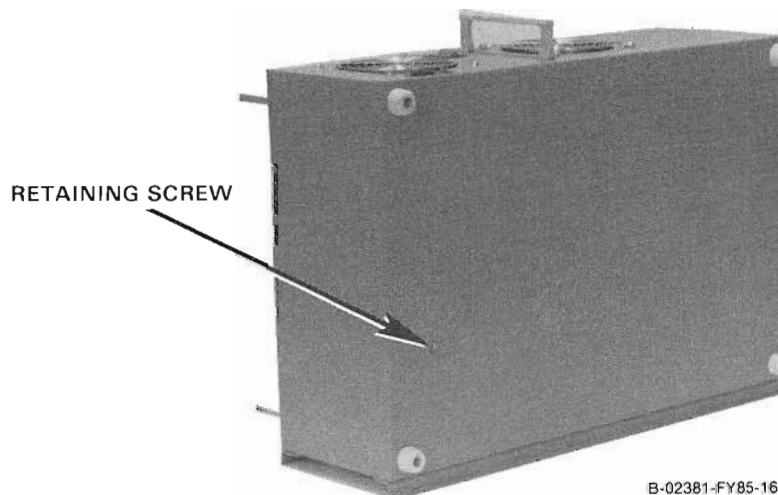
RETAINING SCREW

B-02381-FY85-16

Fig. 5-3   Bottom Retaining Screw

6. Remove the 2 hex head screws from the system as shown in Fig. 5-4.
7. Unplug the following connectors;
   The 4 lug connectors on the ac power on/off switch. (Ref. Fig. 5-6).
   The power connector to the system cooling fan.
8. Carefully lift the power supply out of the unit.

RETAINING
SCREWS
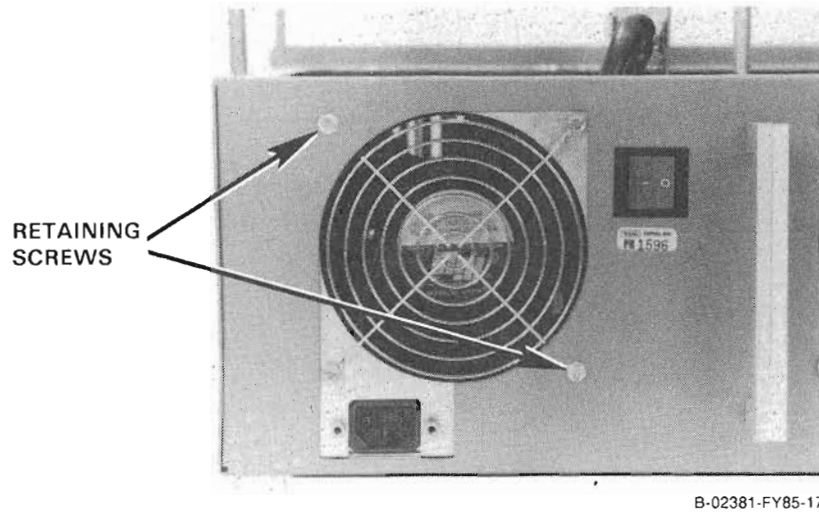
B-02381-FY85-17
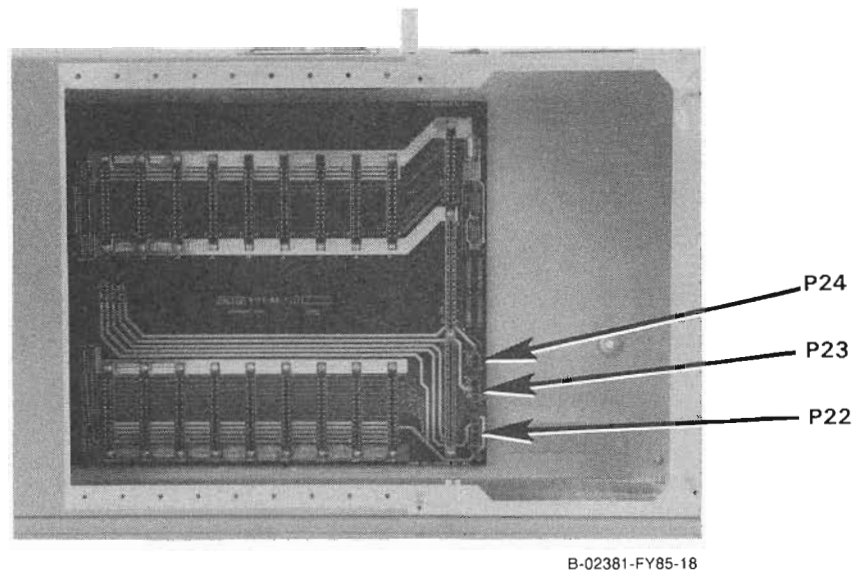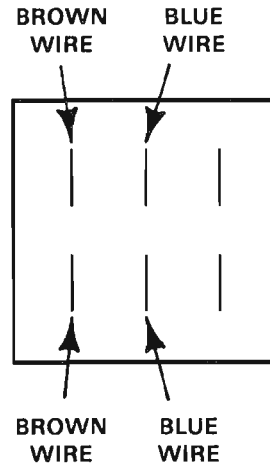
Fig. 5-4 Power Supply Retaining Screws

P24

P23

P22

B-02381-FY85-18

Fig. 5-5 Motherboard Connectors

BROWN   BLUE
WIRE   WIRE

BROWN   BLUE
WIRE   WIRE

B-02381-FY85-26

Fig. 5-6 AC Power On/Off Switch Wiring

5.5.4 Switching Power Supply Replacement

To replace the Switching Power Supply in the Micro VP system;

1. Insert the power supply into the unit.
2. Insert P22, P23, and P24 into their proper recepticles in the motherboard.
3. Reconnect the power connector to the system cooling fan.
4. Reconnect the 4 lug connectors on the ac power on/off switch. The correct wiring for these is shown in Fig. 5-6.
5. Insert the 2 hex head screws into the system and tighten. (Ref. Fig. 5-4.)
6. Insert the phillips head screw into the system and tighten. (Ref. Fig. 5-3.)
7. Re-install the CPU/Memory Bd (Ref. section 5.5.6).
8. Replace the top cover onto the unit.

5.5.5 CPU/Memory Board Removal

To remove the CPU/Memory board from the Micro VP system;

1. Ensure that ac power to the unit has been disconnected.
2. Remove the top cover from the system.
3. Carefully lift the CPU/Memory board from its motherboard slot and out of the unit.

5.5.6 CPU/Memory Board Replacement

To replace the CPU/Memory board in the Micro VP system;

1. Insert the CPU/Memory board into its slot in the Micro VP motherboard. (Ref. Fig. 5-7).
2. Install the top cover onto the system.
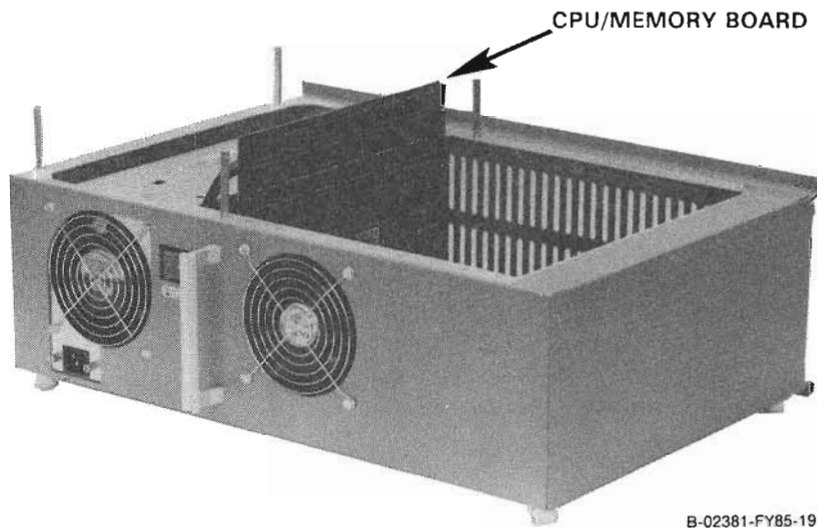
CPU/MEMORY BOARD

B-02381-FY85-19

Figure 5-7 CPU/Memory Board

5.5.7 I/O Controller Board Removal

To remove an I/O Controller board from the Micro VP system;

1. Ensure that ac power to both the unit and the connected peripheral has been disconnected.
2. Remove any external cabling to the I/O controller board.
3. Unscrew the two screws securing the I/O Controller Board to the unit.
4. Carefully lift the unit from its motherboard slots and out of the system.

5.5.8 I/O Controller Board Replacement

To replace an I/O Controller board in the Micro VP system;

1. Remove AC power from both the CPU and the peripheral to be connected.
2. Insert the I/O Controller board into a slot in the Micro VP motherboard.
3. Secure the board to the system with two screws.
4. Connect any external cabling to the I/O Controller.

5.5.9 Motherboard Removal

To remove the Motherboard from the Micro VP system;

1. Ensure that AC power has been removed from the system.
2. Remove top cover from the system.
3. Remove external cabling from the I/O boards.
4. Remove all I/O boards.
5. Remove CPU/Memory board.
6. Unplug connectors P22, P23, and P24 from the motherboard. Ref. Fig. 5-5.
7. Remove 42 phillips-head retaining screws and lift motherboard from the system.

5.5.10 Motherboard Replacement

To replace the motherboard in the Micro VP system;

1. Insert motherboard into the unit.
2. Insert 42 phillips-head retaining screws and tighten.
3. Plug connectors P22, P23, and P24 into the motherboard. Ref. Fig. 5-5.
4. Install CPU/Memory board.
5. Install all I/O boards and reconnect any associated cabling.
6. Install top cover on the system.
7. Apply ac power to the system and run diagnostics as necessary to ensure proper operation of the unit.

5.5.11 System Cooling Fan Removal

1. Remove ac power from unit and disconnect plug from power recepticle.
2. Remove I/O boards from slots shown in Fig. 5-8.
3. Unplug fan power cord from fan as shown in Fig. 5-9.
4. Loosen and remove 4 retaining screws, and lift fan from the unit.

REMOVE BOARDS FROM
THESE SLOTS
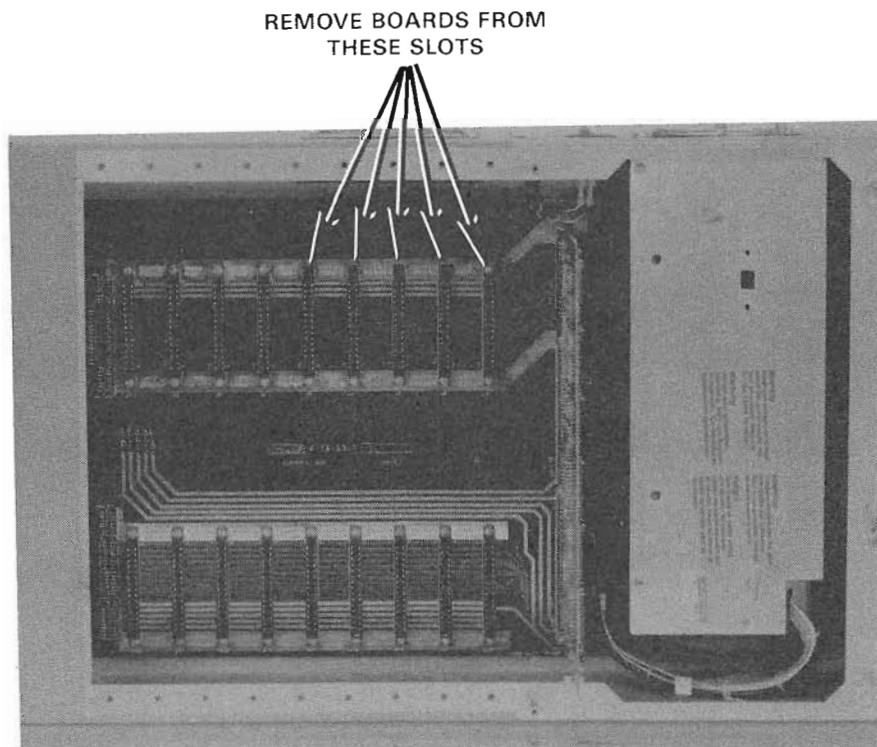
B-02381-FY85-21

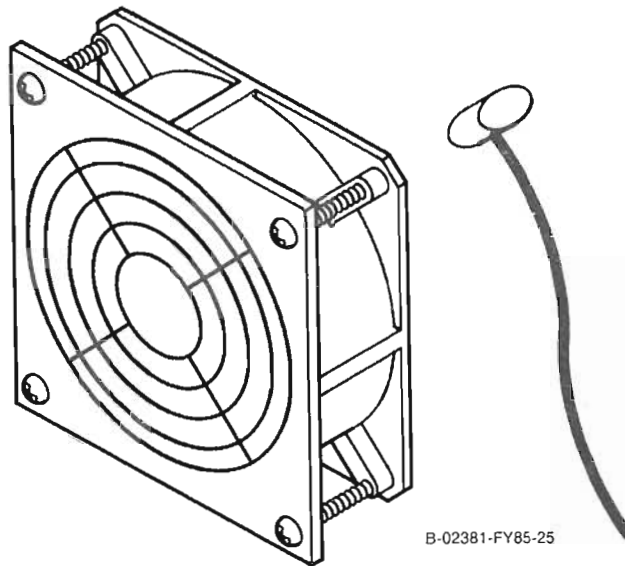Fig. 5-8 I/O Board Slots

B-02381-FY85-25

Fig. 5-9 Fan Power Connection

NOTE

Never remove the power supply cooling fan
individually from the system. It is not a field
replaceable item. It should be considered a
sub-assembly of the power supply and as such,
should only be replaced in conjunction with the
entire power supply.


5.5.12 System Cooling Fan Replacement

1. Insert cooling fan in system.
2. Insert 4 phillips-head screws and tighten.
3. Connect fan power cord.
4. Install I/O boards in motherboard slots.
5. Apply ac power to the unit and check fan for proper
   operation.

CHAPTER 6

ILLUSTRATED PARTS BREAKDOWN

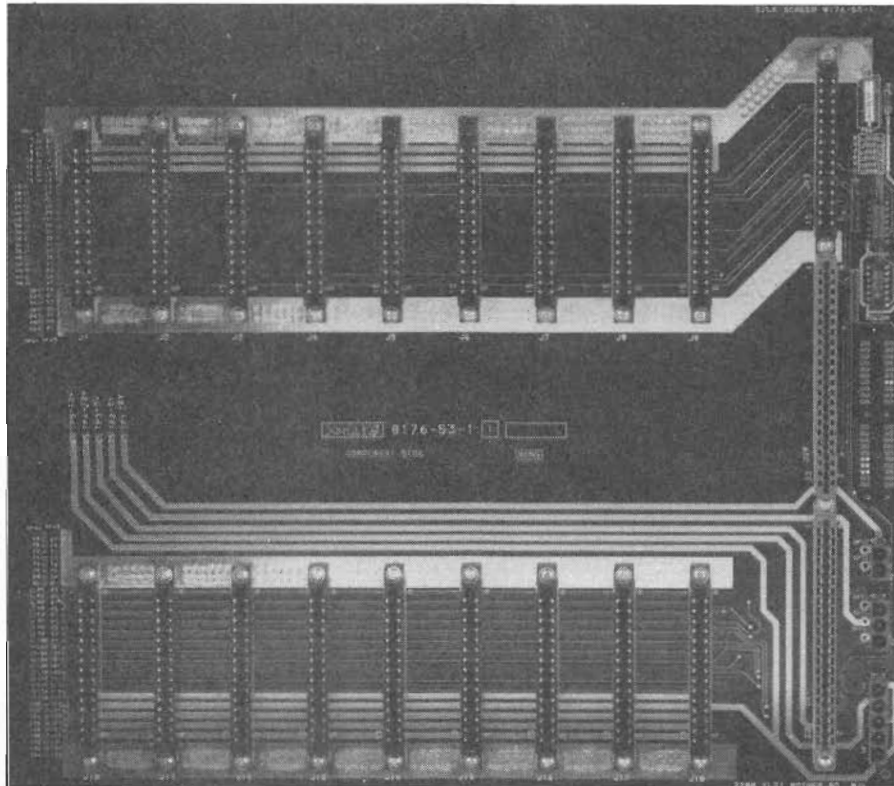### 6.1 SCOPE

This chapter contains the Illustrated Parts Breakdown for the Micro VP-1 and Micro VP-2 Computer Systems. Use this breakdown for part number identification when ordering field-replaceable components.
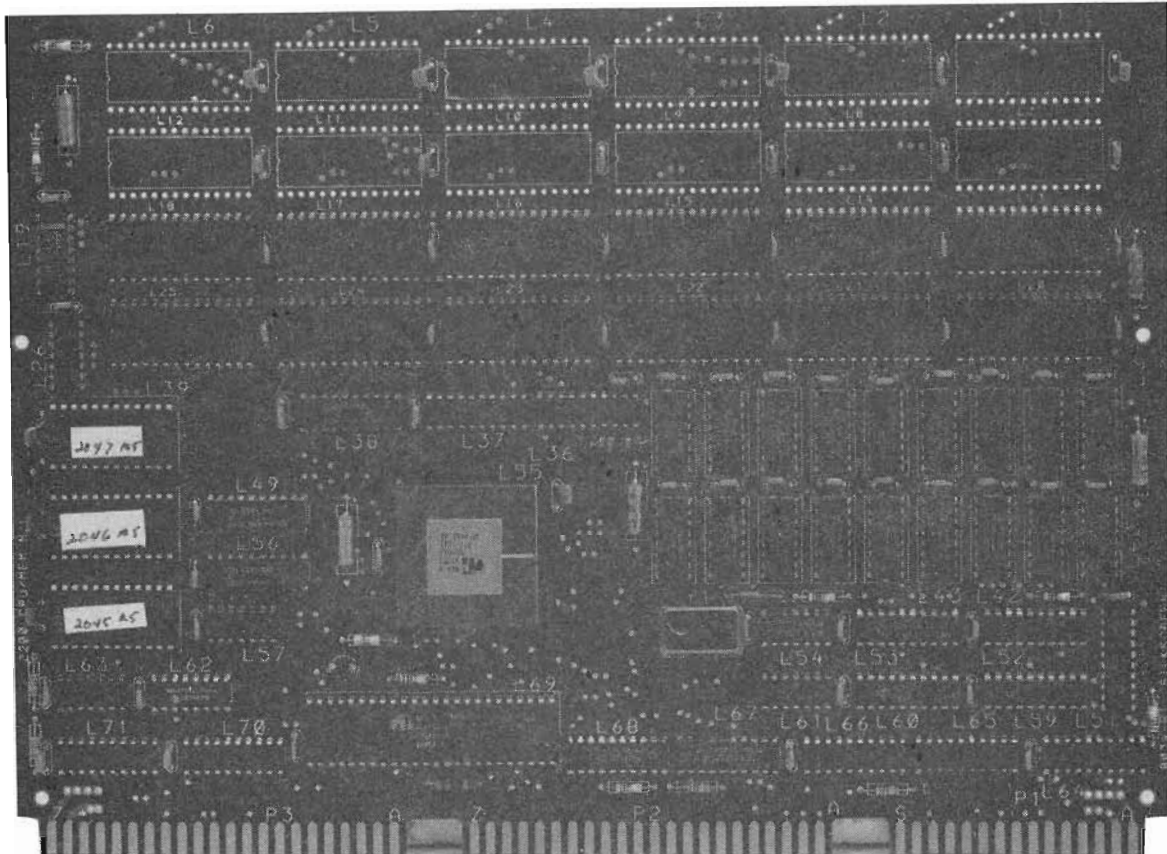
B-02381-FY85-4

Figure 6-1 CPU/Memory Board 210-8034
210-8034-1 (128K)
210-8034-2 (512K)

B-02381-FY85-6

Figure 6-2   Micro VP Motherboard
210-8176

B-02381-FY85-7

Figure 6-3   Switching Power Supply
270-0986

FIELD REPLACEABLE UNIT
PART NUMBERS

ITEM	DESCRIPTION	PART NUMBER
1.	CPU/Memory Bd.	210-8034-1 (128K)
		210-8034-2 (512K)
2.	Motherboard	210-8176
3.	Power Supply	270-0986
4.	Cooling Fan	400-1029
5.	Power Switch	325-0059

CHAPTER 7

TROUBLESHOOTING

7.1 SCOPE

This chapter describes the various diagnostic test programs available for the Micro VP, and gives guidelines for their use. It also provides a guide for isolating fault locations of field replaceable units.

There are three classes of diagnostic tests available for the Micro VP. The first, "Bootstrap" diagnostic, is a diagnostic program resident in the Micro VP CPU hardware. The next, the Microcode Diagnostics, test the hardware components of the system and attempt to pinpoint any malfunction. These are available from the Operating System Diskette. In the last class are the diagnostics available for Micro VP peripheral devices. A brief discussion of each follows in this section.

7.2 BOOTSTRAP DIAGNOSTICS

The Bootstrap Diagnostics are resident diagnostics loaded in three 1024 x 8 bit Intel 2708 PROMs. The purpose of the Bootstrap is to handle Master Initialization (Power-On), handle Reset (Initiated by depressing the RESET key on the keyboard), detect parity errors in Control and Data memory, and load the desired system software (i.e. diagnostics, or BASIC-2) from disk and initiating their execution. The Bootstrap diagnostics run automatically whenever the system is powered up, and verify basic system functions such as the CPU, Control Memory, Data Memory, and Registers. When these diagnostics have successfully completed the following message will appear on the screen;

```
MOUNT SYSTEM PLATTER
PRESS RESET
```

Three types of errors and five possible error messages can be reported by BOOTSTRAP. The three types of errors – initialization, reset, and system, are discussed below.

7.2.1 Initialization Errors

The first type of error is the initialization error. If, during BOOTSTRAP master initialization, the above message fails to display, a CPU related error or an I/O related error is indicated. The displaying of each letter in the above message corresponds to the successful completion of certain diagnostic tests. The following pages provide a breakdown of each letters' meaning and also gives guidelines for troubleshooting failures.

NOTE

It should be noted here that due to the small number of field-replaceable items in the Micro VP-1 and Micro VP-2 systems, and the complexity of the CPU/Memory Board, virtually all error codes encountered will require that the CPU/Memory Board be repaired/replaced.

CRT DISPLAY	SEQUENCE OF OPERATIONS	POSSIBLE FAILURES
Blank	Power on Trap to 8003	Hardware Trap Failure. Branch Instruction Failure.
Blank	Enable CRT, Clear Screen and Display "M".	CRT Address is wrong. I/O Register Failure. I/O Lines are Bad. CIO Instruction Failure.
"M"	Tests 24-Bit Parity Trap. Execute IC 800F which has Bad Parity.	Parity Checking Logic Failure. Hardware Trap Failure. TSP Instruction Failure (IC + 1 stored in stack) PC's may not hold IC retrieved from Stack. Compare Instruction Failure.
"MO"	Test Subroutine Branch and Subroutine Return Instructions.	Subroutine Branch Instruction Failure. Subroutine Return Instruction Failure. Stack Failure.
"MOU"	Clear CH, CL Parity Bits	Write/Read Data Memory Failure
"MOUN"	Check File Registers	Register Instruction Failure. Register Chip Failure. Compare Instruction Failure.
"MOUNT"	Check PC Incrementing on the A-BUS.	PC Chip Failure LPI Instruction Failure. Register Instruction Failure. A-Bus Increment Hardware Failure. Compare Instruction Failure.

CRT DISPLAY	SEQUENCE OF OPERATIONS	POSSIBLE FAILURES
"MOUNT S"	Test Auxiliary Registers	Auxiliary/Stack Chip Failure. PC Chip Failure Auxiliary Register Instruction Failure.
"MOUNT SY"	Test Binary ALU	Binary ALU Failure. AC, ACX, AI, SC, or SCX Instruction Failure.
"MOUNT SYS"	Test Stack	Auxiliary/Stack Chip Failure. PC Chip Failure. Stack Instruction Failure. Compare Instruction Failure.
"MOUNT SYST"	Test Decimal ALU	Decimal ALU Failure. DAC, DACI, DACX, DSC, DSCI, or DSCX Instruction Failure. Compare Instruction Failure.
"MOUNT SYSTE"	Test Binary Multiply	Multiply Hardware Logic Failure. M or MI Instruction Failure. Compare Instruction Failure.
"MOUNT SYSTEM"	Test Shift	Shift Logic Error. Compare Instruction Failure.
"MOUNT SYSTEM "	Verify PROM	PROM Chip Failure.
"MOUNT SYSTEM P"	Zero 8-Bit Data Memory	SR Failure Bad IC's.
"MOUNT SYSTEM PLATTER" "PRESS RESET"	System Loops, diagnosing data and control memory. All Diagnostics have passed. Press RESET to start system operation.	

7.2.2 Reset Errors

Reset Errors are errors which occur while attempting to respond to the prompt "Key SF'". Possible causes of this type of error are;

- The Special Function Key was not depressed sufficiently.
- The 2236DE/DW, 3336DE/DW, 2236MXD, or 2236MXE may be defective.
- The Special Function Key which was depressed was undefined.

7.2.3 System Errors

System Errors are error conditions which are reported to the operator via a SYSTEM ERROR message on the CRT. Memory errors and Disk errors are common examples of system errors. A breakdown of each of these follows:

7.2.3.1 Memory Errors

Should a memory error be detected, the following screen will appear;

```
    *** SYSTEM ERROR MMMM XXXX ***
PRESS RESET
```

In these cases:
          MMMM - PECM = Parity Error Control Memory
                 PEDM = Parity Error Data Memory
                 VECM = Verify Error Control Memory
                 VEDM = Verify Error Data Memory
          XXXX - Various error information pertenent to the
                 type of error.

In both Data Memory and Control Memory, one bit has been set aside for parity error detection. In Control Memory, when a parity error has been detected during an instruction fetch, a branch is made to Control Memory address 8000 (Hex), located in the bootstrap proms. The Bootstrap then performs its designated error routine and displays an PECM error on the screen as follows;

```
*** SYSTEM ERROR (PECM aaaa dddddd) ***
```

Bad parity may be the result of:

- the dropping of bits by Control/Bootstrap Memory
- the picking up of bits by Control/Bootstrap Memory
- writing bad parity to Control Memory
- defective parity checking logic

It may be possible, after encountering this error, to resume execution of the currently loaded system program. However, if the error occurs again a Control Memory diagnostic should be run. If a failure occurs, the CPU/Memory board should be replaced.

In Data Memory, when a parity error has been detected, a branch is made to Control Memory address 8002 (Hex), located in the bootstrap proms. The Bootstrap then performs another error routine and displays a PEDM error as follows:

```
*** SYSTEM ERROR (PEDM ss.aaaa) ***
```

This error implies that bad parity was detected during a read of Data Memory. The same causes listed above for Control Memory may applied to Data Memory as well. Again, it may be possible to resume execution of the currently loaded system program, unless the error is reported again. In this case, a Data Memory diagnostic should be run. Again, if a failure occurs, the CPU/Memory board should be replaced.

VECM and VEDM are verify errors which imply that attempts to load either Data or Control memory were unsuccessful. If these errors occur, the operator should attempt to reload BASIC-2. However, should successive failures be reported, appropriate memory diagnostics should be run to determine if there are any defective memory chips.

7.2.3.2 Disk Errors

There are several possible disk errors that may occur while Bootstrap is trying to load a particular system program. In most cases, the recovery procedure that should be taken is to attempt to reload the system program. Below is a listing of possible disk errors, their cause, and recovery procedures.

ERROR	POSSIBLE CAUSE	POSSIBLE RECOVERY
0082	The file to be loaded does not reside on the platter specified.	Ensure that the proper platter is properly mounted, that the proper disk drive was specified, and that the proper special function key was pressed. Press RESET as prompted, and select the appropriate special function.
0088	Wrong Record Type Error which occurs during a load when the format of the record read does not conform to the bootstrap format.	Ensure that the proper platter is properly mounted, the proper disk drive was specified, and that the proper special function key was pressed. Press RESET, as prompted, and select the appropriate special function.
0090 0091 0092	A disk hardware error occured. The disk did not recognize or respond to the system at the beginning of a read or write operation, or the disk is not in a file-ready position.	Ensure that the disk is turned on and properly set up for operation. Set the disk into LOAD mode and then back into RUN mode, with the RUN/ LOAD selection switch.
0093	A disk format error was detected during a disk read or write. Specifically the system was unable to read a sector address.	Verify correct drive head alignment. If correct, reformating the disk is. required. Be aware that this action will result in the loss of all data on the disk.

ERROR	POSSIBLE CAUSE	POSSIBLE RECOVERY
0094	The disk format key is engaged (the key should be engaged only when formatting a disk.	Turn off the format key.
0095	A disk-seek error occurred; the specified sector could not be found on the disk.	Run the program again. If the error persists, reinitialize the disk. Could also be hardware related.
0096	System was unable to read the data field of a sector.	If the disk has been formatted, rewrite the bad sector or reformat the disk. Reformatting the disk will result in the loss of data from the disk, however.
0097	A longitudinal redundancy check occurred when reading a sector.	Ensure that the system platter is properly mounted in the operator specified disk unit. Key RESET, as prompted, and try to reload. If the error persists, try a backup platter.
0098	The disk sector being addressed is not on the disk.	Ensure that the disk is ready and the system platter is properly mounted in the operator specified disk unit. Key RESET, as prompted, and try to reload. If the problem persists, then bootstrap may be bad or the disk may be defective.

7.3 MICROCODE DIAGNOSTICS

The Microcode Diagnostics are diagnostics which perform in depth testing of the hardware components of the system. These diagnostics reside on the system disk and are accessed in the following manner:

1. Apply power to the system and verify that the screen on terminal 1 appears as below:

```
MOUNT SYSTEM PLATTER
PRESS RESET
```

2. Place the system platter disk/diskette into the system drive and press the RESET key on the keyboard. (Press RESET if the terminal is model #2336DE and SHIFT RESET if the terminal is model #2336DW.) Observe the screen shown.

KEY SF'?

3. Depress the special function key which corresponds to the drive which contains the system disk. The screen will now display:

****SYSTEM 2200****

Select item with SPACE & BACKSPACE   MEMORY xxxxK
Key RUN to execute, CLEAR or PREV SCRN for previous screen   Terminal X

■ MVP BASIC-2
_ Diagnostics

4. Space down to Diagnostics, and key RUN. The screen now appears:

****CUSTOMER DIAGNOSTIC MENU****

Select item with SPACE & BACKSPACE   MEMORY xxxxK
Key RUN to execute, CLEAR or PREV SCRN for previous screen   Terminal X

■ CPU Instructions
_ Control Memory
_ Data Memory
_ CPU Registers

_ All of the above

5. Below are descriptions of each of these diagnostics.

7.3.1 CPU Instructions Diagnostic

This diagnostic is designed to test the instruction set of the Central Processor. The test sequence is as follows:

a) Test Immediate Register instructions
b) Test Register instructions
c) Test Extended Register instructions
d) Test Branch instructions
e) Test Immediate Register instructions with Read/Write
f) Test Register instructions with Read/Write
g) Test Mini Instructions with Read/Write
h) Return to step a

If RESET is keyed during this program, the KEY SF'? message shall be displayed.

A normal display is as follows:


```
                ***CPU INSTRUCTIONS DIAGNOSTIC***   REV XXXX

  (PASS XXXX)
  IMMED REG LL
  REG INSTR LL              where:   XXXX = Number of completed loops
  X-REG INSTR LL                     LL = Microinstruction currently
  MASK BR LL                              being tested (in Hex).
  REG BR LL
  IMMED R/W LL
  REG R/W LL
  AUX/STACK R/W LL
```


Should the system be unable to execute a particular instruction, the CRT cursor will stop at XX of the failing instruction. Should the title fail to appear, any of the following could be at fault: ORI, AC, SB, SR, B, BT, BF, BNE, BLER, or BNR.

7.3.2 Control Memory Diagnostic

The control memory diagnostic tests control memory from end-of-program to end-of-memory for addressing, and a modified Row Pattern test.

A normal display is as follows:


```
                ***CONTROL MEMORY DIAGNOSTIC***   REV XXXX

  Memory Size = xxxxK                             No Err's
```


The following tests are cycled through, each time incrementing the pass count:

7.3.2 Cont.

DATA BUS STUCK TEST (PASS XXXX)

DATA BUS SHORTS TEST (PASS XXXX)

BANK/PAGE ADDRESSING (PASS XXXX)

ADDRESS LINE SHORT TEST (PASS XXXX)

ADDRESS LINE/PIN TEST (PASS XXXX)

ADDRESS MULTIPLEXER (PASS XXXX)

SIMPLE MARCHING 1's/0's (PASS XXXX)

24 BIT, MOVING INVERSIONS (PASS XXXX)

When RESET is keyed during this program, the KEY SF'? message will be displayed.

7.3.3 Data Memory Diagnostic

The data memory diagnostic tests data memory from end-of-program to end-of-memory for addressing, and a modified Row Pattern test.

A normal display is as follows:

```
            ***DATA MEMORY DIAGNOSTIC***   REV XXXX

Memory Size = xxxxK                              No Err's
```

The following tests are cycled through, each time incrementing the pass count:

DATA BUS STUCK TEST (PASS XXXX)

DATA BUS SHORTS TEST (PASS XXXX)

BANK/PAGE ADDRESSING (PASS XXXX)

PARITY GENERATION TEST (PASS XXXX)

ADDRESS LINE SHORT TEST (PASS XXXX)

ADDRESS LINE/PIN TEST (PASS XXXX)

ADDRESS MULTIPLEXER (PASS XXXX)

SIMPLE MARCHING 1's/0's (PASS XXXX)

9 BIT MOVING INVERSIONS (PASS XXXX)

When RESET is keyed during this program, the KEY SF'? message will be displayed.

7.3.4 CPU Registers Diagnostic

This diagnostic tests registers F0-F7, CH, CL, PH, PL, SL, K, AUX 0-32, and STACK 0-96 (the SH register is not tested due to the ability of the hardware to change bit status).

A normal display is as follows:

```
                          ***CPU REGISTER DIAGNOSTIC***

No Err's           Press 'P' to Print Errors at /215 ('T' For /204)
```

The following tests are cycled through, each time incrementing the pass count:

8 Bit Registers Test (PASS XXXX)

Aux Memory Test (PASS XXXX)

Stack Memory Test (PASS XXXX)

If ALL OF THE ABOVE is chosen from the User Diagnostic Menu, each of the diagnostics mentioned previously will be run. All screens will remain the same with the exception of the Chain Mode Pass Count. This count is the number of passes all of the tests have successfully completed.

7.4 PERIPHERAL DEVICE DIAGNOSTICS

Because of the wide range of peripherals available to the Micro VP systems, it would be impractical to present here a full list of the diagnostics supported for each. All available peripherals are fully documented in their own maintenance publications.

7.5 DIAGNOSTIC ERROR MESSAGES

The following section further outlines various error messages which may be encountered during the aforementioned diagnostics. Due to the small number of field-replaceable items in the Micro VP-1 and Micro VP-2 systems, and the complexity of the CPU/Memory Board, virtually all error codes encountered will require that the CPU/Memory Board be repaired/replaced.

1. **AECM** Errors (**A**ddressing **E**rror in **C**ontrol **M**emory)

This error is displayed as;

AECM aaaa bbbb xxxxxx

Where: aaaa = the address of th instruction in error
            bbbb = the conflicting address
            xxxxxx = An XOR of the expected and actually read instruction

This error indicates that writing to Control Memory location bbbb seems to modify location aaaa. The "1" bits in the xxxxxx field of the display indicate which bit(s) have been modified. The error could also occur if a chip at location aaaa had a marginal failure.

2. **BECM** Errors (**B**it **E**rror in **C**ontrol **M**emory)

This error is displayed as:

BECM aaaa xxxxxx

Where: aaaa = the address of the instruction in error
            xxxxxx = An XOR of the instruction actually read from memory
                     with the instruction that was expected to be there.

This error implies that a bit error was detected while reading Control Memory. The "1" bits in the xxxxxx field of the display indicate which bit(s) are incorrect.

3. **PECM** Errors (**P**arity **E**rror in **C**ontrol **M**emory)

This error is displayed as:

PECM aaaa dddddd

Where: aaaa = the address of the instruction with bad parity
             dddddd = the instruction located at aaaa. The instruction
                       is reread when displayed and thus may not be the
                       same as when the error occurred.

   This error implies that bad parity was detected during execution of the
diagnostic.

4. **VECM** Errors (Verify Error in Control Memory)

   This error is displayed as:

   VECM aaaa

   Where: aaaa = an address in the section of Control Memory that
                          does not verify correctly.

5. **AEDM** Errors (Addressing Error in Data Memory)

   This error is displayed as:

   AEDM ss.aaaa ss.bbbb xx

   Where: ss =   Memory bank containing the error
                aaaa =   Address of the data in error
                bbbb =   Conflicting Address
                  xx =   XOR of the expected and actually read data.

   This error indicates that writing to location bbbb seems to modify
location aaaa. The "1" bits in the xx field of the display indicate which bits
have been modified. The error could also occur if a chip at location aaaa had
a marginal failure.

6. **BEDM** Errors (Bit Error in Data Memory)

   This error is displayed as:

```
BEDM ss.aaaa xxyy
```

Where: ss =   Memory bank containing the error
          aaaa =   Address of the data in error
          xxyy =   XOR of the data <u>actually read</u> from data memory
                     with the data that was <u>expected</u> to be there.

This error implies that a memory error was detected while reading data memory. The "l" bits in the xxyy field of the display indicate which bit(s) are not correct. If all the bits are zero, one of the two parity bits associated with the pair of bytes is incorrect.

7. **PEDM** Errors (<u>P</u>arity <u>E</u>rror in <u>D</u>ata <u>M</u>emory)

This error is displayed as:

```
PEDM ss.aaaa
```

Where: ss =   Memory bank containing the error
          aaaa =   Data Memory address at the time of the error. This
                     is probably, but not necessarily, the address of
                     the memory location with bad parity.

This error implies that bad parity was detected during a read of a 8-bit User/Data Memory.

8. **REDM** Errors (<u>R</u>ead <u>E</u>rror in <u>D</u>ata <u>M</u>emory)

This error is displayed as:

```
REDM ss.aaaa xx
```

Where: ss =   Memory bank contining the error
          aaaa =   Address of the data in error
            xx =   XOR of the data in memory with the data that was
                     expected to be there.

This error implies that a memory error was detected while reading User/Data memory. The "l" bits on the xx field of the display indicate which bits are not correct. If all the bits are zero, a bit in the other byte of th pair of bytes is incorrect.

9. **VEDM** Errors (Verify Error in Data Memory)

This error is displayed as:

        VEDM ss.aaaa

Where: ss =   Memory bank containing the error
         aaaa =   Address of the data in error

This error is reported to a system program being given control after loading, or when memory is verified in response to RESET or CLEAR being executed. The area of User/Data Memory used for storing constants (BASIC verb tables, math constants, messages) does not verify correctly.

10.**General Registers Error Displays**

This error is displayed as either of the below:

Error 1)

REGISTER TEST
FFFF
REGISTER TT AND CC ERROR (XX)
#LL

                        Where: FFFF =   Number of completed loops at time
                                          of error
                                  TT =   Name of register under test
                                  CC =   Name of conflict register
                                  XX =   Contents of register CC

This error is caused when testing register TT, register CC was found not to contain the expected.

Error 2)

REGISTER TEST
FFFF
REGISTER TT ERROR (XX)
LLLL

This error is caused when the register under test fails to hold the test pattern.

11.Auxiliary/Stack Error Displays

This error is displayed as either of the below:

Error 1)

```
AUXILIARY TEST
# FFFF
AUX TT FAILURE (XXXX)
# LLLL
```

Where: FFFF = Number of completed loops at time
               of error.
          TT = Auxiliary register under test.
        XXXX = XOR of expected and actual.

This error occurs when the Auxiliary register under test is found not to contain the expected test pattern.

Error 2)

```
AUXILIARY TEST
# FFFF
AUX TT AND AUX CC FAILURE (XXXX)
# LLLL
```

Where: CC = Conflict register

This error is caused when Auxiliary register CC was found not to contain the expected test pattern.

Error 3)

```
AUXILIARY TEST
# FFFF
STACK AND AUX TT FAILURE (XXXX)
# LLLL
```

This error is caused when a Stack level was found not to contain the expected test pattern.

12.Stack/Auxiliary Error Displays

This error is displayed as either of the below:

```
STACK TEST
# FFFF
STACK FAILURE (XXXX)
# LLLL
```

Where: FFFF =   Number of completed loops at
                time of error
       XXXX =   XOR of expected and actual

This error is caused when a Stack level fails to maintain the expected pattern.
        Error 2)

```
STACK TEST
# FFFF
AUX YY FAILURE (XXXX)
# LLLL
```

Where: YY = Auxiliary register

This error is caused when a particular Auxiliary register fails to maintain the expected pattern.

Other Error Codes which may be encountered are listed below by catagory:

Syntax Errors:

S10	Missing left parenthesis
S11	Missing right parenthesis
S12	Missing equal sign
S13	Missing comma
S14	Missing asterisk
S15	Missing angle brackets
S16	Missing letter
S17	Missing hex digit
S18	Missing relation operator
S19	Missing required word
S20	Expected end of statement
S21	Missing line number
S22	Illegal PLOT argument
S23	Missing literal string
S24	Illegal expression or missing variable
S25	Missing numeric scalar variable
S26	Missing array variable
S27	Missing numeric array
S28	Missing alpha array
S29	Missing alpha variable

NONRECOVERABLE ERRORS

Misc. Errors:

A01	Memory exceeded (overlap: text & symbol table)
A02	Memory exceeded (overlap: text & value stack)
A03	Not enough memory (LISTDC, MOVE, COPY)
A04	Stack overflow (operator stack)
A05	Line too long
A06	Program protected
A07	Illegal immediate mode statement
A08	Statement not legal here
A09	Program not resolved

Program Errors:

P32	Starting address greater than ending address
P33	Line number conflict
P34	Illegal value
P35	No program
P36	Undefined line number or CONTINUE illegal
P37	Undefined special function subroutine
P38	Undefined FN function
P39	FN nested too deep
P40	NEXT without FOR
P41	RETURN without GOSUB
P42	Illegal image
P43	Illegal matrix operand
P44	Matrix not square
P45	Operand dimensions not compatible
P46	Illegal microcommand
P47	Missing buffer variable
P48	Illegal device specification
P49	Interrupt table full
P50	Illegal dimensions or variable length
P51	Variable or value too short
P52	Variable or value too long
P53	Noncommon variables already defined
P54	Common variable required
P55	Undefined array
P56	Illegal subscripts
P57	Illegal STR () arguments
P58	Illegal field/delimiter specification
P59	Illegal redimension

RECOVERABLE ERRORS

Computation Errors:

C60	Underflow
C61	Overflow
C62	Division by zero

C63	Zero divided by zero, or zero raised to zero power
C64	Zero raised to negative power
C65	Negative number raisee to noninteger power
C66	SQR of negative power
C67	LOG of zero
C68	LOG of negative power
C69	Argument too large

`Execution Errors:

X70	Insufficient data
X71	Value exceeds format
X72	Singular matrix
X73	Illegal INPUT data
X74	Wrong variable type
X75	Illegal number
X77	Invalid partition reference

Disk Errors:

D80	File not open
D81	File full
D82	File not in catalog
D83	File already catalogued
D84	File not scratched
D85	Index full
D86	Catalog end error
D87	No end file
D88	Wrong record type
D89	Sector address beyond EOF

I/O Errors:

I90	Disk hardware error (X'CO' not received)
I91	Disk hardware error
I92	Disk hardware error (timeout)
I93	Disk format error
I94	Format key engaged
I95	Seek error
I96	CRC error
I97	LRC error
I98	Illegal sector address
I99	Read-after-write error

CHAPTER 8

SCHEMATICS

Please refer to the Microfiche version of this document for the Micro VP Computer System schematics.

APPENDIX A

2275 MULTIPLEXER/MULTIPLEXER EXTENDER OPTION

The 2275 Multiplexer and 2275 Multiplexer Extender (2275MUX/2275MUXE) boards will enable a single 2275 Disk Drive or 2280 Phoenix Drive (or future DPU-type disk systems) to serve multiple CPUs. The multiplexer enables up to four CPUs to share a disk drive; a multiplexer extender, used in conjunction with the multiplexer, enables up to four additional CPUs to share the same disk. A single multiplexer can support a maximum of three multiplexer extenders and can thus serve a maximum of 16 CPUs.

The multiplexer and any associated multiplexer extenders plug into adjacent slots on the system bus. The multiplexer provides a disk interface for the Micro VP in which it resides, eliminating need for the resident 22C80 board. The extender boards connect to the multiplexer via a ribbon cable and draw power from the system bus.
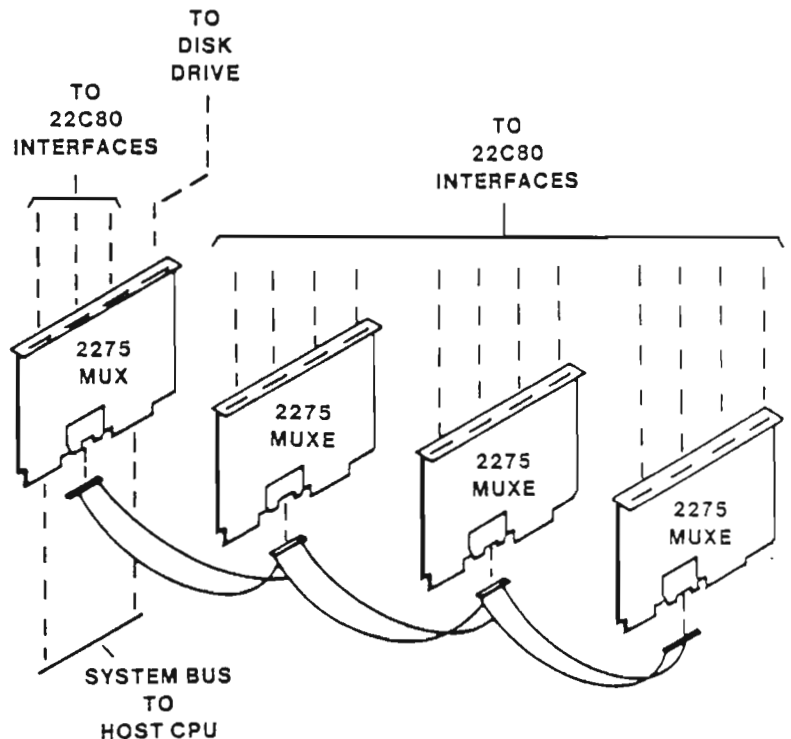
8-03521-FY87-13

The multiplexer, in conjunction with the multiplexer extender(s), divides functionally into five general areas:

- Ring counter and port-select logic

- Port Buffers

- 2200 Interface

- Extender input/output

- Disk Buffer

8-03521-FY87-11
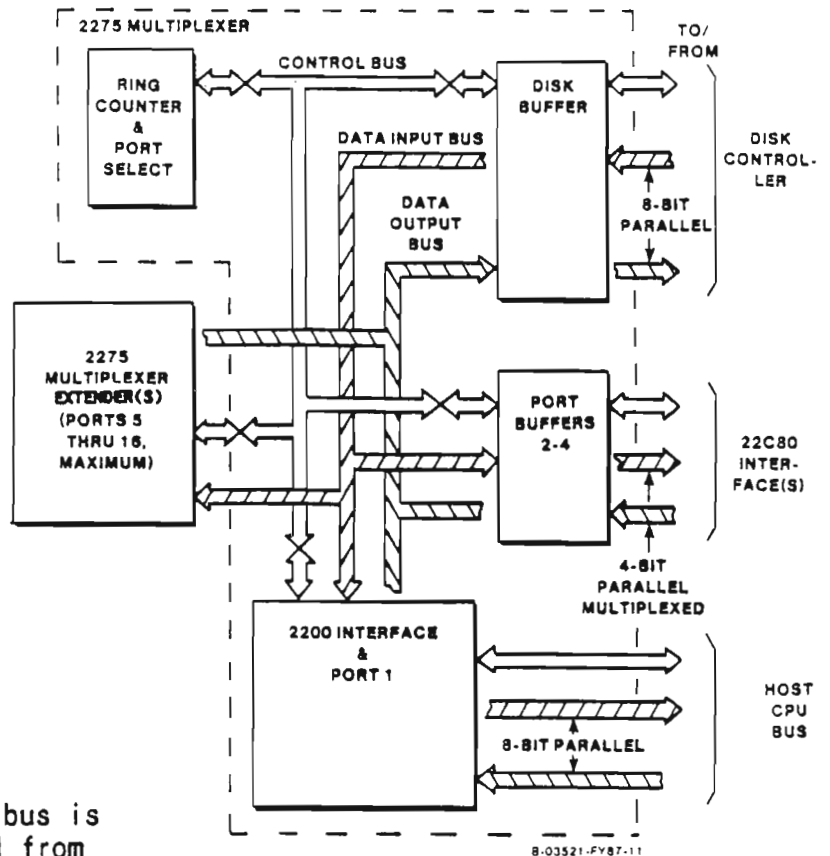
Data on the multiplexer I/O bus is four-bit parallel, converted from eight-bit parallel from either the disk drive (input) or from the respective CPUs (output). The disk buffer converts between the eight-bit disk bus and and the four-bit multiplexed bus for each I/O operation; the 22C80, of the requesting CPU, converts between the eight-bit CPU bus and the four-bit multiplexed bus. The 2200 Interface (Port 1) portion of the multiplexer board performs the same conversion for each transmission between the host CPU and the multiplexer.

The port-select logic comprises a binary counter and a four-bit bistable latch. A 2-Mhz clock drives the counter to generate 16 sequential scan addresses, one for each port. The port-select logic scans each port in sequence until a request is detected.

Any CPU, to access the disk drive, raises a request signal by addressing its 22C80 interface. The port-select logic, upon detecting the request, disables the counter clock and returns an acknowledge signal to the 22C80 interface. With the ring counter disabled, and the requesting port selected, the requesting CPU can access the disk drive.

The input and output data busses connecting the CPU to the drive are four-bit parallel busses. The port buffers interface the multiplexed busses and control signals to the multiplexer when enabled. The decoding of the associated scan address for the given port enables the appropriate port buffer.

B-03521-FY87-7
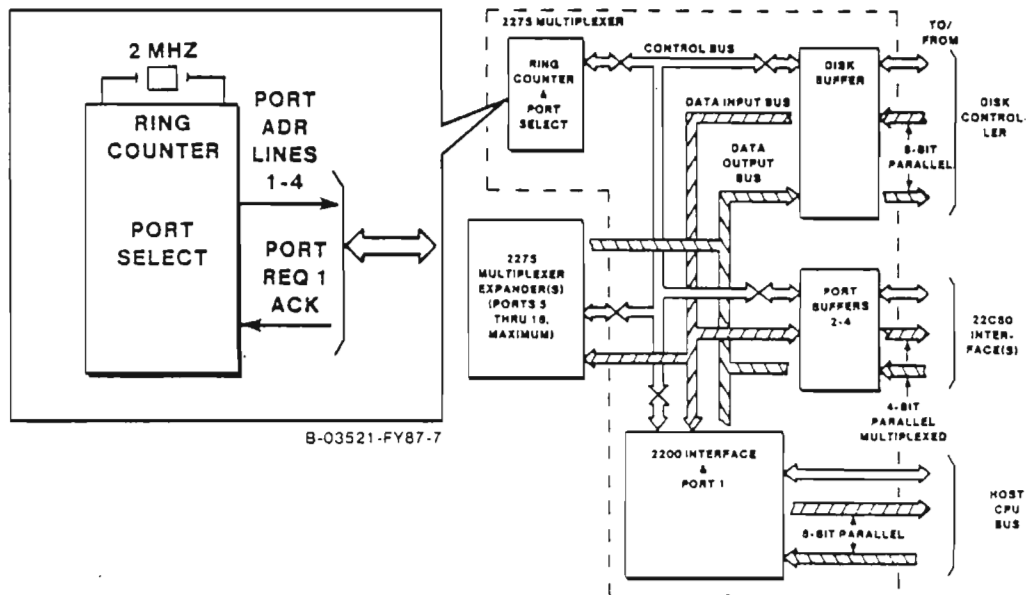
When a port buffer decodes its associated scan address interfacing is
enabled between the respective 22C80 board and the multiplexer. Once
the link has been made, the multiplexer is transparent to both the
disk drive and the requesting CPU. When the disk access is complete,
the 22C80 request clears, the clock counter resumes counting, and port
request scanning resumes.
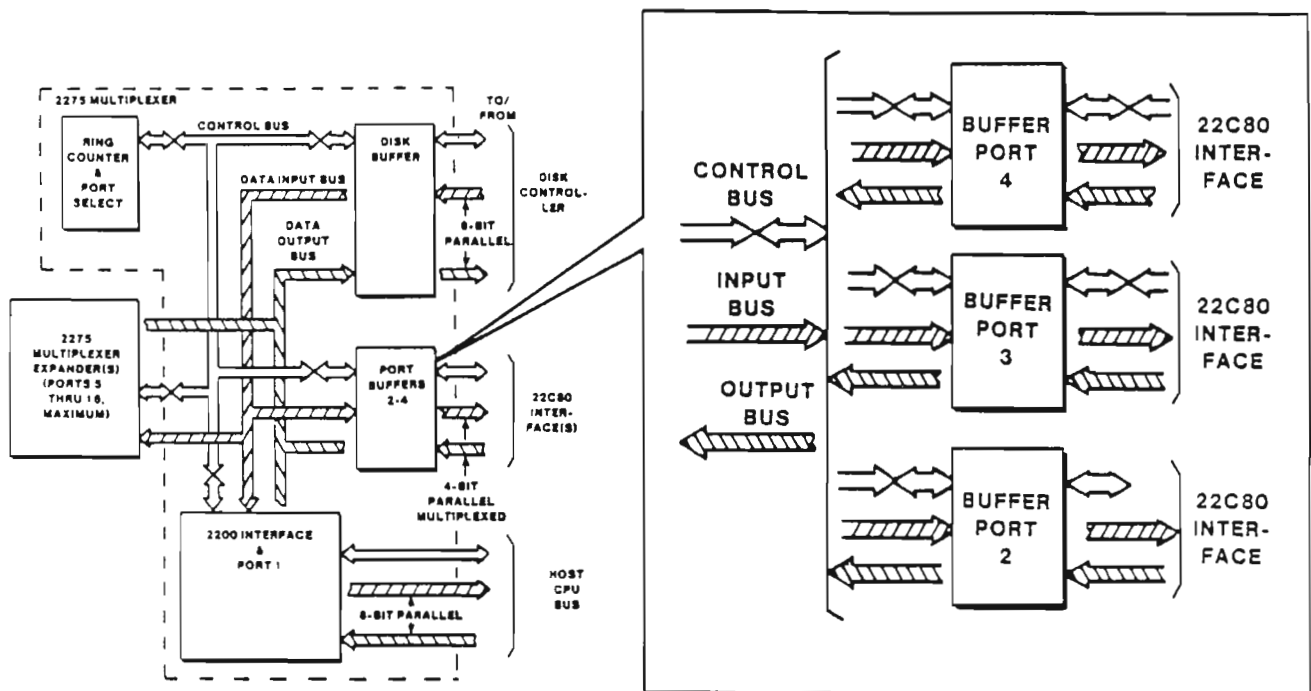
B-03521-FY87-5

The 2200 Interface of the multi-
plexer board combines the
functions of port buffer and 22C80
Interface. The 2200 Interface both
decodes the scan address (in the
same manner as the other port
buffers) and performs the 22C80
functions for the CPU in which
it resides.
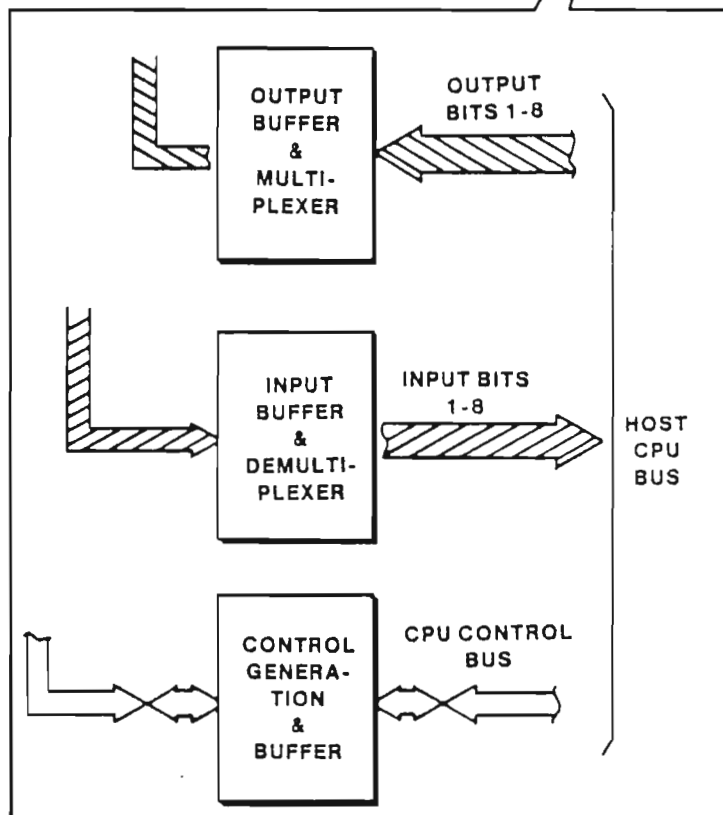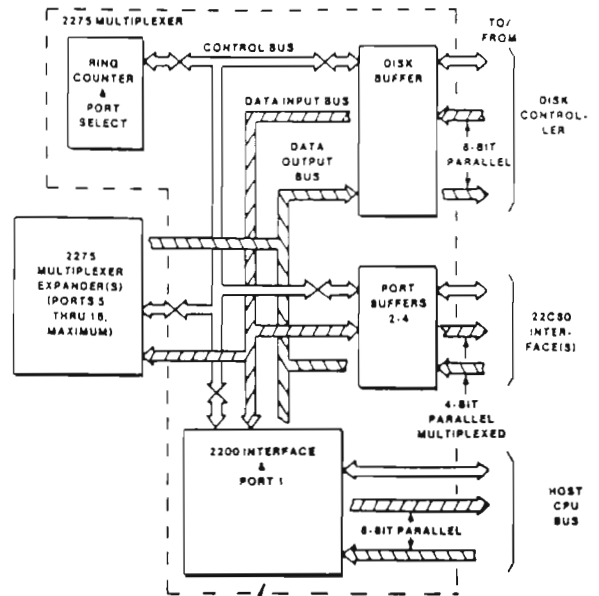
B-03521-FY87-4

The extender boards interface the same control and data busses as the port buffers resident on the multiplexer board. Each extender board contains four port buffers. The port-select logic has an addressing capability of 16 addresses (maximum); therefore, the system can accommodate but 12 extension port buffers (plus the four port buffers resident on the multiplexer board).
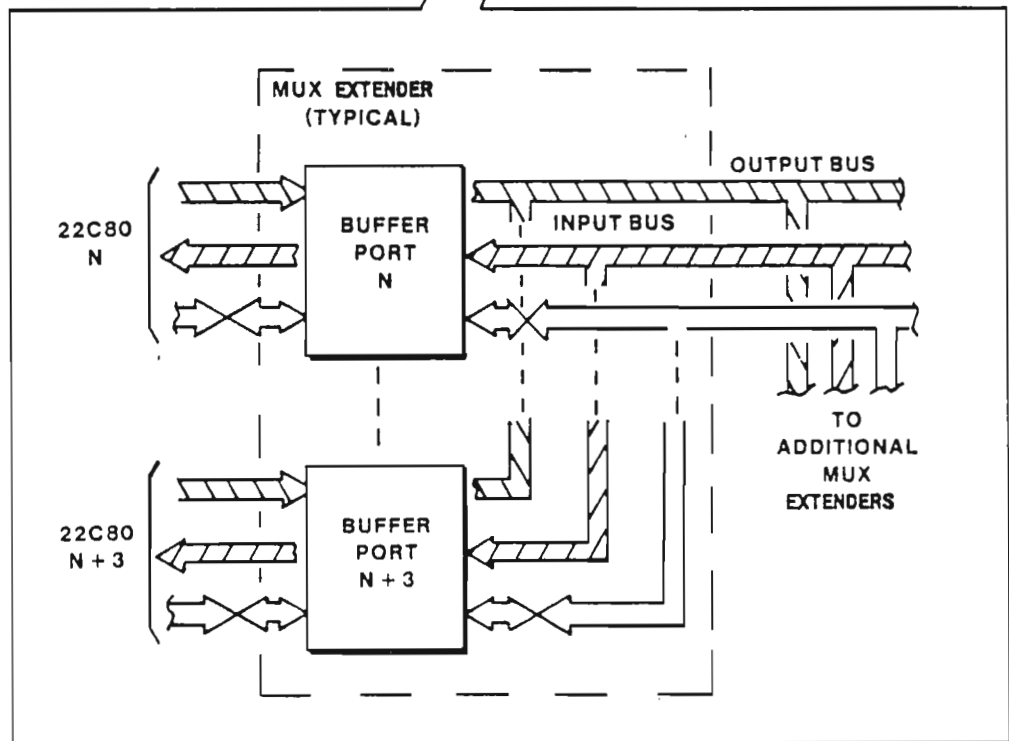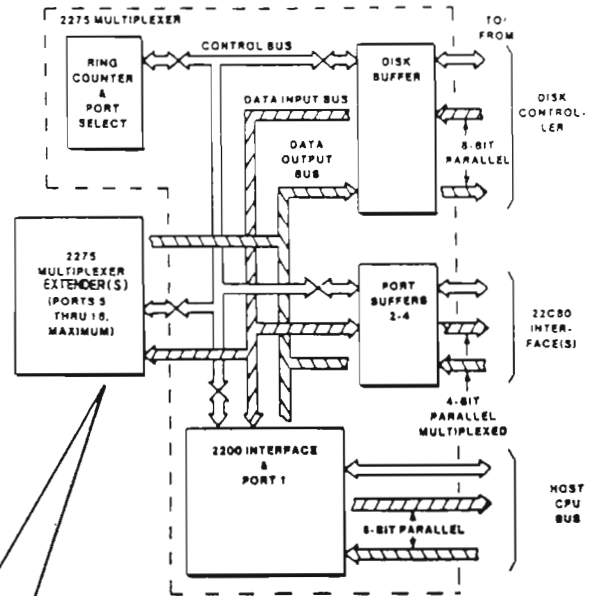
B-03521-FY87-2

The disk buffer consists of I/O buffer multiplexer/demultiplexers which interface between the disk I/O busses and the multiplexed I/O busses internal to the multiplexer hardware. The input buffer receives eight-bit-parallel disk data, and loads the data on the internal bus as four-bit transmissions. Conversely, the output buffer assembles four-bit-parallel output data into eight-bit bytes for transmission to the disk controller.
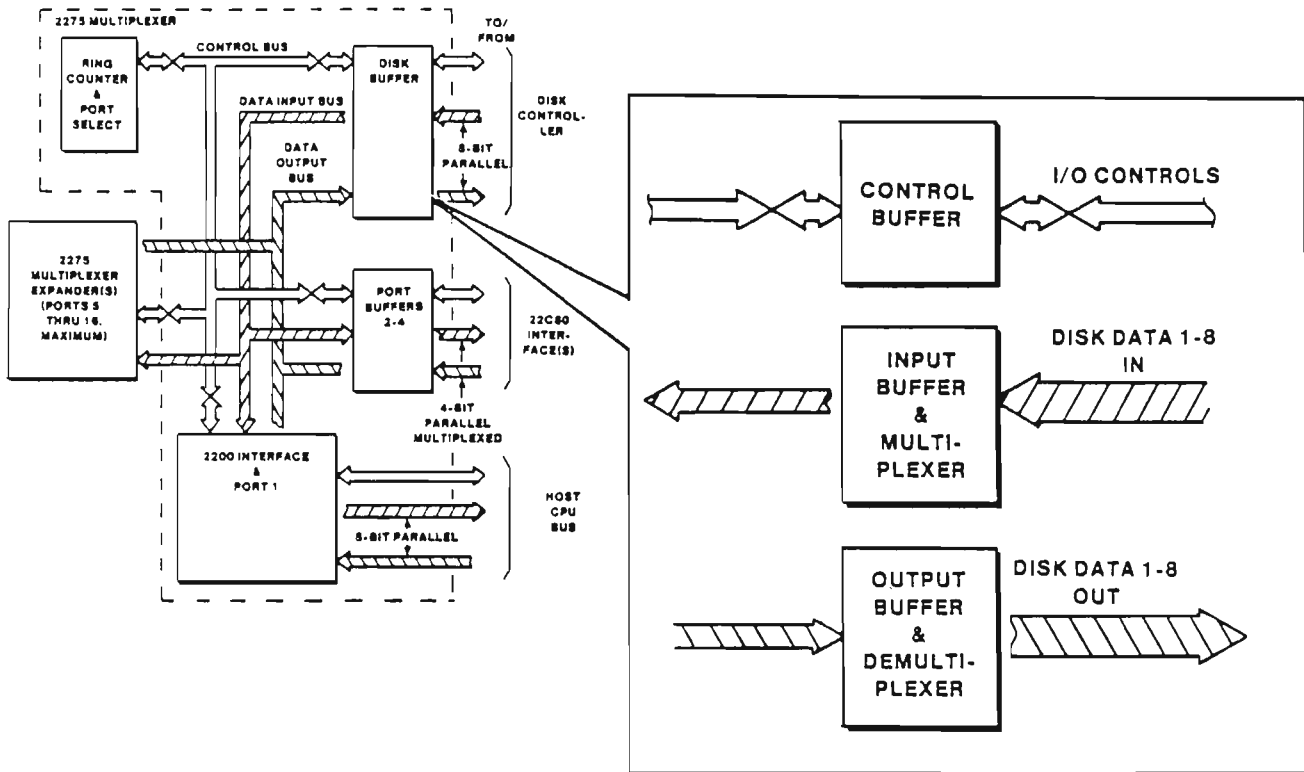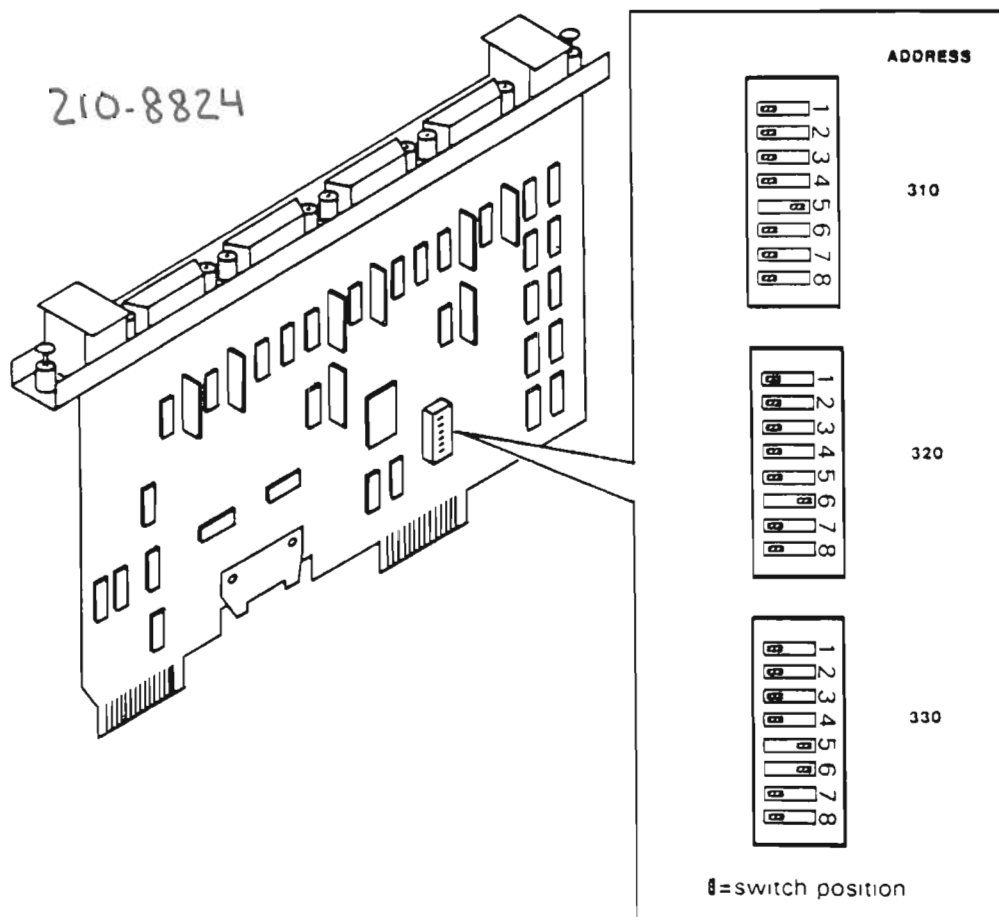

B-03521-FY87-1

A.1   INSTALLATION

Installation of the multiplexer board and extender board(s) comprise the ensuring of address switch settings, and the completion of (multiplexer) system hookup. Both the multiplexer and extension boards plug into the Micro VP system bus in the same manner as any other option boards.

A.1.1   Switch Settings

The setting of Switch 1 on the multiplexer board determines the disk address of the system in which the multiplexer resides. Additional systems establish disk address on their associated 22C80 Disk Interface switch settings (the disk address does not have to be the same for different systems using the same disk drive). Set desired disk address for host system as shown here.

210-8824

ADDRESS

310

320

330

ä=switch position

B-03521-FY87-14

A.1.1   Switch Settings (cont)

Switch 1 on each extender board identifies the extender so that its ports may be addressed by the multiplexer (the address selected via Switch 1 should not be confused with the disk address; there is no connection between the two addresses). A single extender board in a system may be set to an address of either 1, 2, or 3. The setting of additional boards requires only that no two addresses be the same.
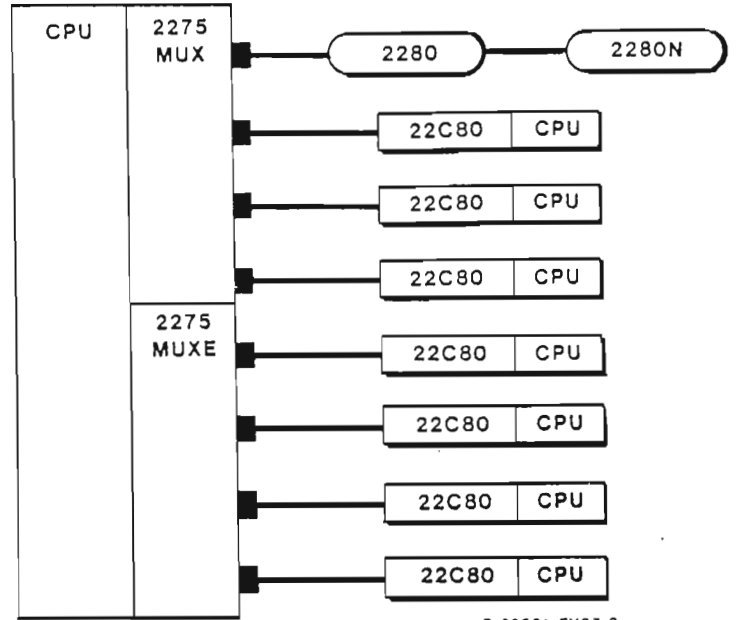

210·8825
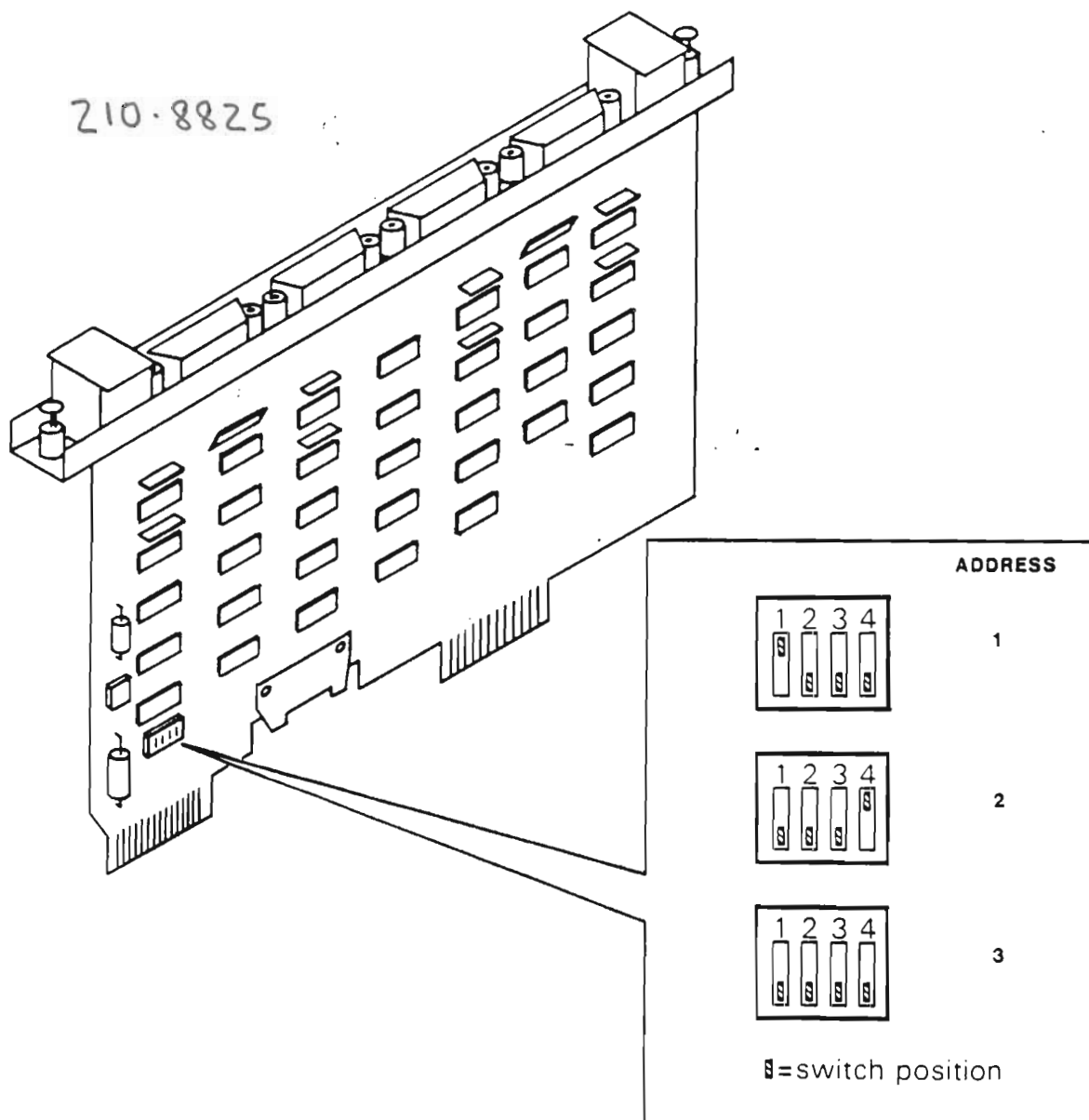
8-03521-FY87-16
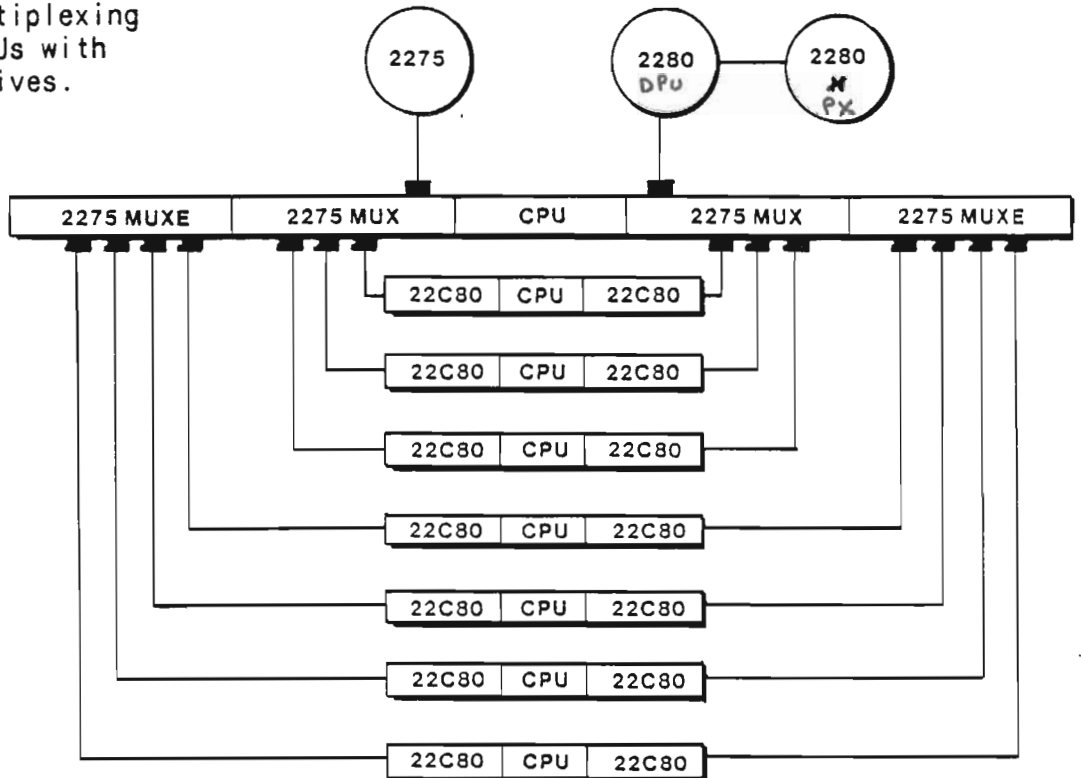
A.1.2 System Hookup

For cabling connections to associated CPUs and disk drive, <u>refer to appropriate installation instructions</u>. The following sketches show examples of hookups, including:

a typical hookup multiplexing eight CPUs with one disk drive

B-03521-FY87-8

and the multiplexing of eight CPUs with two disk drives.

B-03521-FY87-10

A.1.2   System Hookup (cont)
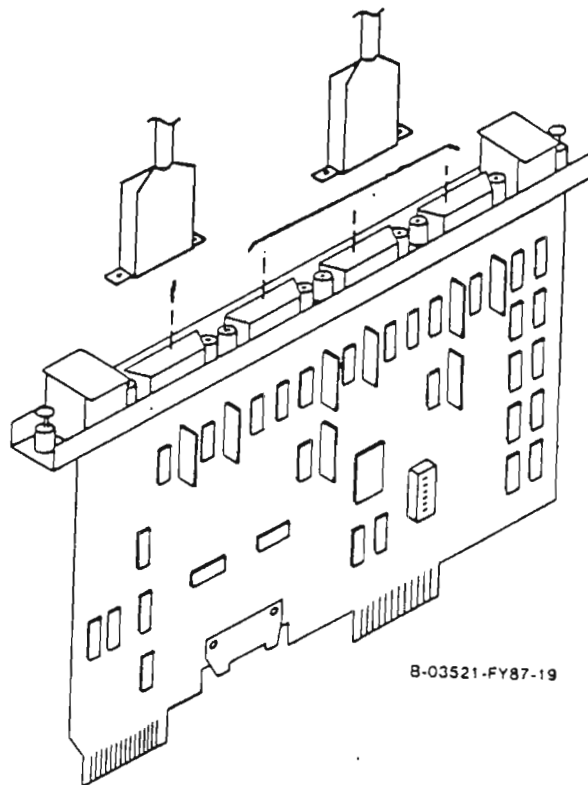
1. Insert multiplexer board into
   available CPU option slot.

   MULTPLEXER BRD PART # 210·8824

2. Connect cable from disk drive
   to connector marked
   DISK DRIVE.

3. Connect cable(s) from associ-
   ated CPU(s) to available
   connectors.
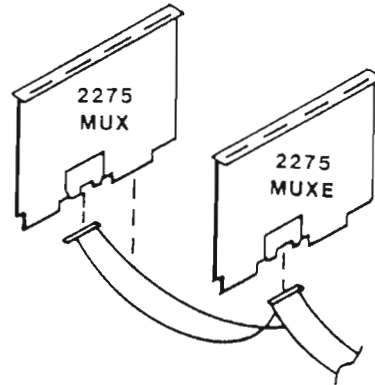
   PART # OF CABLES.
   AVAILABLE LENGTHS

B-03521-FY87-19

A.1.2 System Hookup (cont)
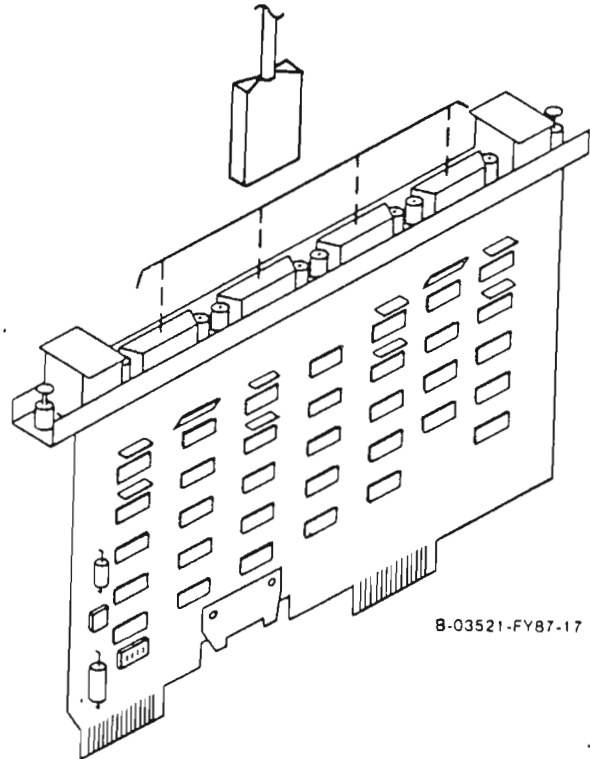
4. Insert extension board(s) into
    adjacent slots.

    EXPANDER BRD PART # 210·8825

5. Connect multiplexer to exten-
    sion board(s) via supplied
    ribbon cable.

    RIBBON CABLE PART # 220·3588

6. Connect cable(s) from associ-
    ated CPU(s) to available
    connector(s).

    CABLE PART #'s & LENGTHS.

2275
MUX

2275
MUXE

8-03521-FY87-17
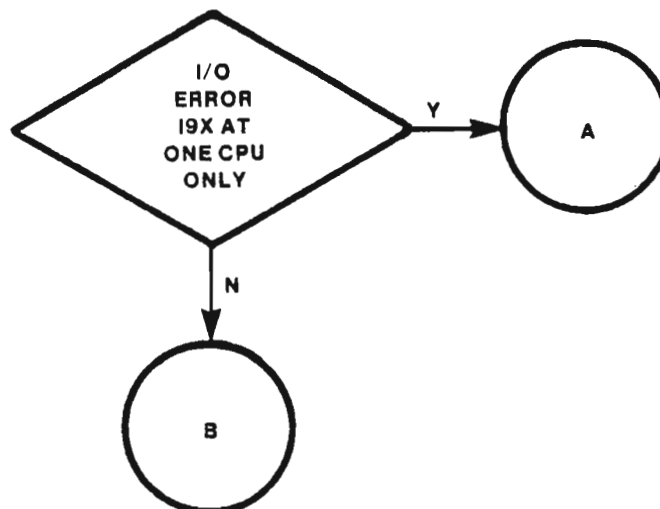
A.2   CHECKOUT

System checkout may be simplified by verification of one unit at a
time prior to a whole-system check.

1. Select diskette containing the
    2200 Multiple Disk Exerciser
    from 2200 Diagnostic Package
    (195-2956-0). Load diagnostic.

2. Run diagnostic simultaneously
    on two or more CPUs, each CPU
    addressing a different disk
    surface/platter. Repeat check
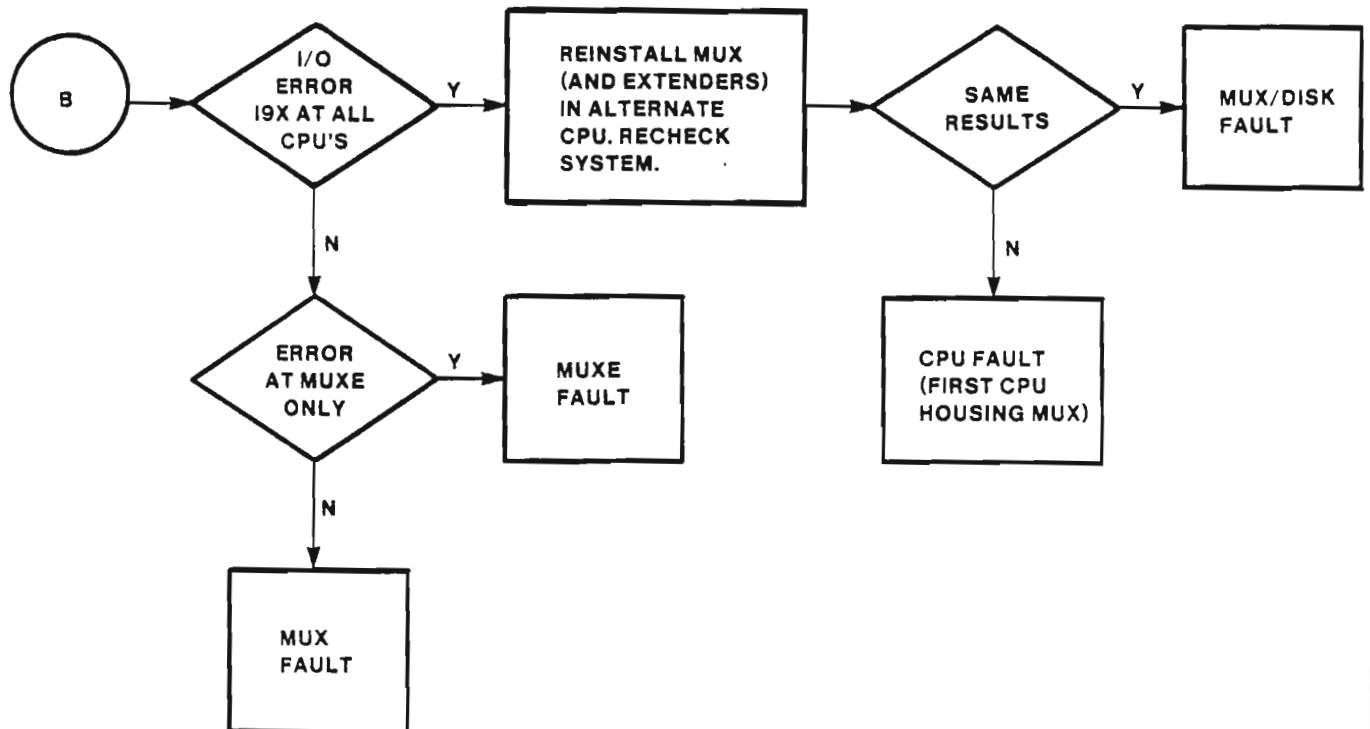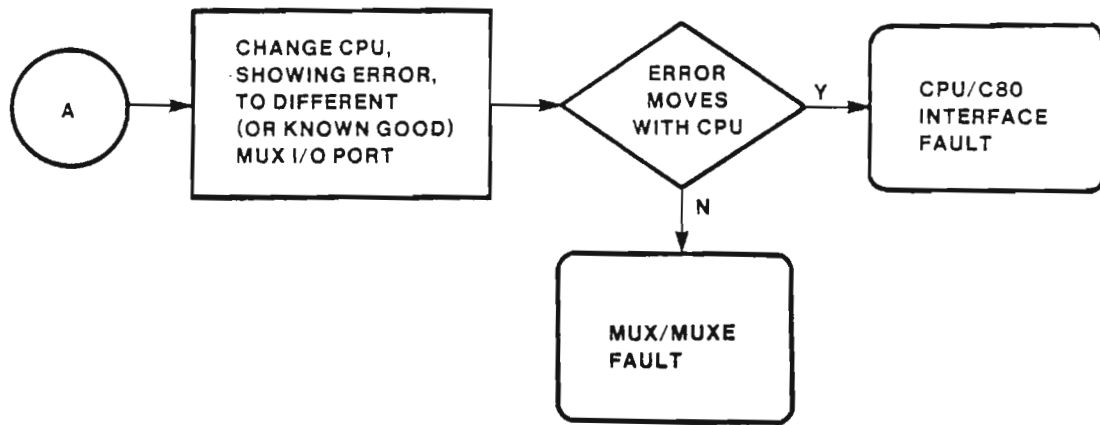   to include all CPUs.

    Should CPU display I/O Error-
    I9X, go to Troubleshooting.

A.3   TROUBLESHOOTING

Should a fault indication occur during initial installation check,
analysis may be aided by a retracing of steps - disconnecting units to
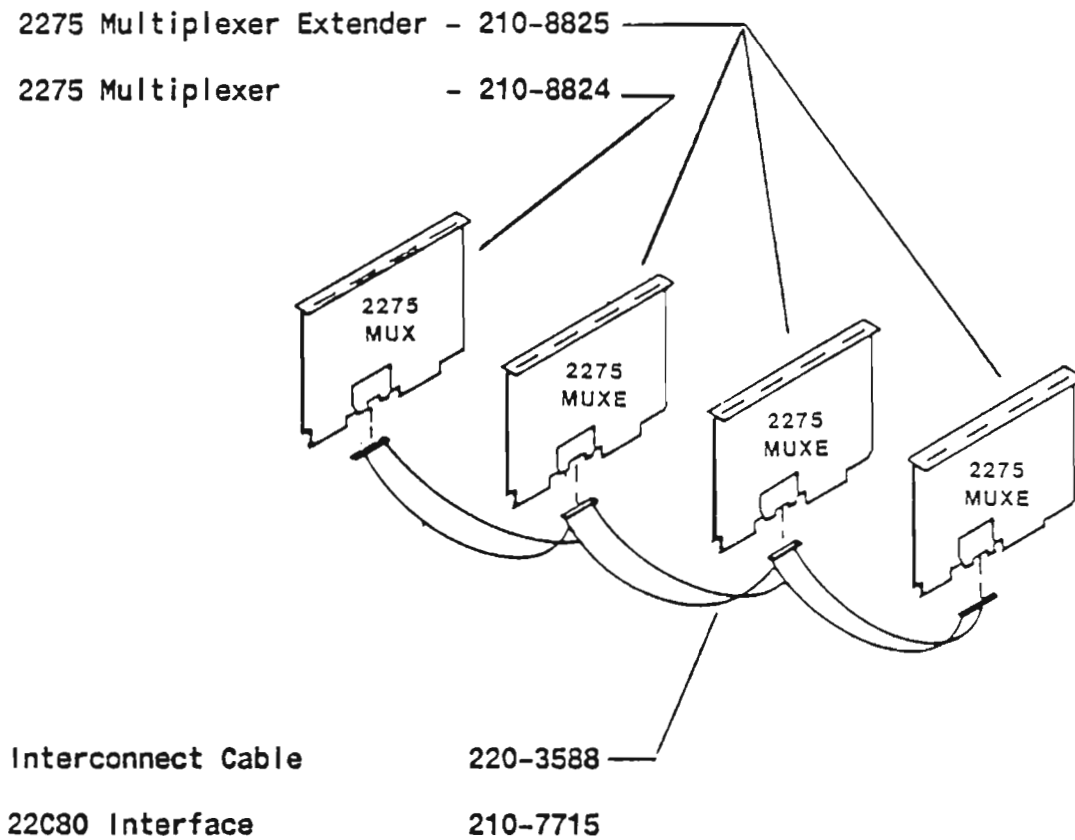point at which fault occurs.

A.3   TROUBLESHOOTING (cont)

```
( A ) ──► [ CHANGE CPU,       ──► < ERROR        ── Y ──► [ CPU/C80
            SHOWING ERROR,         MOVES                    INTERFACE
            TO DIFFERENT           WITH CPU >               FAULT ]
            (OR KNOWN GOOD)             │
            MUX I/O PORT ]              N
                                        │
                                        ▼
                                  [ MUX/MUXE
                                    FAULT ]
```

```
( B ) ──► < I/O        ── Y ──► [ REINSTALL MUX    ──► < SAME      ── Y ──► [ MUX/DISK
            ERROR               (AND EXTENDERS)         RESULTS >             FAULT ]
            I9X AT ALL          IN ALTERNATE               │
            CPU'S >             CPU. RECHECK               N
              │                 SYSTEM. ]                  │
              N                                            ▼
              │                                      [ CPU FAULT
              ▼                                        (FIRST CPU
        < ERROR      ── Y ──► [ MUXE                    HOUSING MUX) ]
          AT MUXE              FAULT ]
          ONLY >
            │
            N
            │
            ▼
      [ MUX
        FAULT ]
```

A.4 PARTS REPLACEMENT

Part numbers of MUX/MUXE components
and associated equipment are as
follows:

2275 Multiplexer Extender - 210-8825

2275 Multiplexer   - 210-8824

Interconnect Cable   220-3588

22C80 Interface   210-7715

NEED PART #'s FOR CABLES BETWEEN MUX BRDS + CPU's
WITH AVAILABLE LENGTHS.

NEW PRODUCT STATUS

2275MUX & 2275MUXE

Current Status: 2275MUX PEP # H0146A
                2275MUXE PEP # H0146B

First Customer Ship: Q4 FY87

Logistics:
    There will be three FRU's associated with this product:
        210-8824 Multiplexer (MUX)   MTBF:104,436 hrs
        210-8825 Multiplexer Extender (MUXE)   MTBF:163,577 hrs
        220-3588 Interconnection Cable   MTBF:TBD

Technical Documentation:
    Documentation class code is TBD.
    This product will be used in the MicroVP, LVP and MVP systems.
    Final revisions are being made to the PUB.

TEE/FSC:
    Repair Plan will be required for the MUX and MUXE. Hardware Specifications
    and Schematics have been provided.

Diagnostic Support:
    Existing 2200 Disk Diagnostics will support this product. The 2275MUX/MUXE
    has been tested using the 2200 Multiple Disk Exerciser (Rev. 64A5). The
    diagnostic was obtained from Wang Direct by ordering diagnostic package
    number 195-2956-0.

Technical Training Center:
    This product should to be included in the 2200 System Class. The Product
    Maintenance Manual and TSB will provide necessary information for Customer
    Engineers previously trained on the 2200 system.

CPU/MEMORY PCB UPGRADE OPTIONS

1.1 INTRODUCTION

1.1.1   Scope and Purpose

The scope and purpose of this manual is to provide the Wang Customer Engineer with the information necessary to install, troubleshoot, and repair the Wang Micro VP in the field. Familiarity with the Wang Micro VP product line is recommended for effective use of this manual.

The Micro VP Computer System is an interactive, multi-user, multi-task, disk-based computer system, utilizing VLSI [Very Large Scale Integration] technology. The Micro VP supports up to 16 terminals and 16 jobs [partitions] concurrently as well as a wide range of peripheral devices, such as printers, plotters, disk drives, tape drives, and TC devices. Disk drive sharing for up to 15 additional CPUs is also available as an option.

By utilizing VLSI, the Micro VP processor design is incorporated into a single chip. This allows the Micro VP CPU, control memory, and user memory to reside on a single PC board. The two models of the Micro VP Computer System offered are the Micro VP-1 that contains 128KB of Data Memory and the Micro VP-2 which contains 512KB of Data Memory. Both systems, however, contain 32K of Control Memory. In addition, these two existing 128KB or 512KB CPU PCBs may be upgraded to Enhanced CPU/Memory configurations via upgrade kits.

2.1   DIAGNOSTIC ERROR MESSAGES

2.1.1   AEDM Errors (Addressing Error in Data Memory)

NOTE

When memory exceeds 512KB, the address information that is displayed for memory error at boot time is invalid.

This error is displayed as:

AEDM ss.aaaa ss.bbbb xx

Where:
  ss=Memory bank containing the error.
aaaa=Address of the data in error.
bbbb=Conflicting Address
  xx=XOR of the "expected" and
     "actually read" data.

This error indicates that writing to location "bbbb" seems to modify location "aaaa". The "1" bits in the "xx" field of the display indicate which bits have been modified. The error could also occur if a chip at location "aaaa" had a marginal failure.

2.1.2 BEDM Errors (Bit Error in Data Memory)

NOTE

When memory exceeds 512KB, the address
information that is displayed for
memory error at boot time is invalid.

This error is displayed as:

BEDM ss.aaaa xxyy

Where:
  ss=Memory bank containing the error.
aaaa=Address of the data in error.
xxyy=XOR of the data "actually read"
     from data memory with the data
     that was "expected" to be there.

This error implies that a memory error was detected while reading data
memory. The "1" bits in the "xxyy" field of the display indicate which bit[s]
are not correct. If all the bits are zero, one of the two parity bits
associated with the pair of bytes is incorrect.

2.1.3 PEDM Errors (Parity Error in Data Memory)

NOTE

When memory exceeds 512KB, the address
information that is displayed for
memory error at boot time is invalid.

This error is displayed as:

PEDM ss.aaaa

Where:
  ss=Memory bank containing the error.
aaaa=Data Memory Address at the time of
     the error. This is probably, but
     not necessarily, the address of the
     memory location with bad parity.

This error implies that bad parity was detected during a read of an 8-bit
User/Data Memory.

2.1.4   REDM Errors (Read Error in Data Memory)

NOTE

When memory exceeds 512KB, the address information that is displayed for memory error at boot time is invalid.

This error is displayed as:

REDM ss.aaaa xx

Where:
  ss=Memory bank containing the error.
aaaa=Address of the data in error.
  xx=XOR of the data in memory with the
      data that was expected to be there.

   This error implies that a memory error was detected while reading User/Data memory. The "1" bits on the "xx" field of the display indicate which bits are not correct. If all the bits are zero, a bit in the other byte of the pair of bytes is incorrect.

2.1.5   VEDM Errors (Verify Error in Data Memory)

NOTE

When memory exceeds 512KB, the address information that is displayed for memory error at boot time is invalid.

This error is displayed as:

VEDM ss.aaaa

Where:
  ss=Memory bank containing the error.
aaaa=Address of the data in error.

   This error is reported to a system program being given control after loading, or when memory is verified in response to RESET or CLEAR being executed. The area of User/Data Memory used for storing constants [BASIC verb tables, math constants, messages] does not verify correctly.

3.1 INSTALLING OPTIONS

3.1.1 Existing Micro VP CPU/Memory PCB Upgrades

Existing 128KB or 512KB CPU PCB users have the option of direct swap-out replacement of current 128KB or 512KB CPU PCBs for the Enhanced CPU PCBs, by ordering Upgrade kits as follows:

Kit Name	Kit P/N	Kit Description	Enhanced CPU PCB P/N
UJ 5057	289-0969	128KB PCB to 512KB PCB	210-8937-B
UJ 5065	289-0968	128KB PCB to 1MB PCB	210-8937-C
UJ 5066	289-0967	128KB PCB to 2MB PCB	210-8937-D
UJ 5067	289-0966	128KB PCB to 4MB PCB	210-8937-E
UJ 5068	289-0965	128KB PCB to 8MB PCB	210-8937-F
UJ 5069	289-0964	512KB PCB to 1MB PCB	210-8937-C
UJ 5070	289-0963	512KB PCB to 2MB PCB	210-8937-D
UJ 5071	289-0962	512KB PCB to 4MB PCB	210-8937-E
UJ 5072	289-0961	512KB PCB to 8MB PCB	210-8937-F

CPU/Memory PCB Replacement Instructions:

1) Power-down system (Ref. sections 3.2.1 and 3.5).

2) Remove the existing 128KB or 512KB CPU PCB (Ref. section 5.5.5).

3) Install the Enhanced CPU PCB replacement (Ref. section 5.5.6).

4) Power-up system (Ref. sections 3.2.1 and 3.4).

5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

3.1.2 Enhanced Micro VP CPU/Memory PCB Upgrades

NOTE

When the accessed memory exceeds 512KB, Operating System Version 3.1 minimum is required.

NOTE

The Micro Diagnostic for Enhanced Memory Test is incorporated in the Operating System Release 3.1.

3.1.2 Enhanced Micro VP CPU/Memory PCB Upgrades (Cont'd)

Micro VP CPU/Memory PCB Upgrade Kits:

MODEL NUMBER	DESCRIPTION
UJ-5057	128KB to 512KB Memory Upgrade
UJ-5059	1MB to 2MB Memory Upgrade
UJ-5060	1MB to 4MB Memory Upgrade
UJ-5061	1MB to 8MB Memory Upgrade
UJ-5062	2MB to 4MB Memory Upgrade
UJ-5063	2MB to 8MB Memory Upgrade
UJ-5064	4MB to 8MB Memory Upgrade
UJ-5065	128KB to 1MB Memory Upgrade
UJ-5066	128KB to 2MB Memory Upgrade
UJ-5067	128KB to 4MB Memory Upgrade
UJ-5068	128KB to 8MB Memory Upgrade
UJ-5069	512KB to 1MB Memory Upgrade
UJ-5070	512KB to 2MB Memory Upgrade
UJ-5071	512KB to 4MB Memory Upgrade
UJ-5072	512KB to 8MB Memory Upgrade

Micro VP CPU/Memory PCB Upgrade Kit Contents:

Each Upgrade Kit includes the following items:

- PAL chip specifically tailored to desired Upgrade Memory size

- Necessary quantity of additional SIMMs Memory Modules to accomplish the upgrade

- Operating System installed on diskette only

Enhanced CPU/Memory PCB Upgrade Installation Instructions:

Presently installed CPU/Memory PCBs may be upgraded to Enhanced CPU/Memory by ordering upgrade kits as follows:

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
128KB	512KB	UJ5057	289-0969	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 5.5.5).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-B (Ref. section 5.5.6).
4) Power-up system (Ref. sections 3.2.1 and 3.4).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
128KB	1MB	UJ5065	289-0968	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 5.5.5).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-C (Ref. section 5.5.6).
4) Power-up system (Ref. sections 3.2.1 and 3.4).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
128KB	2MB	UJ5066	289-0967	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 5.5.5).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-D (Ref. section 5.5.6).
4) Power-up system (Ref. sections 3.2.1 and 3.4).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
128KB	4MB	UJ5067	289-0966	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 5.5.5).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-E (Ref. section 5.5.6).
4) Power-up system (Ref. sections 3.2.1 and 3.4).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
128KB	8MB	UJ5068	289-0965	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 5.5.5).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-F (Ref. section 5.5.6).
4) Power-up system (Ref. sections 3.2.1 and 3.4).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
512KB	1MB	UJ5069	289-0964	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 5.5.5).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-C (Ref. section 5.5.6).
4) Power-up system (Ref. sections 3.2.1 and 3.4).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
512KB	2MB	UJ5070	289-0963	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 5.5.5).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-D (Ref. section 5.5.6).
4) Power-up system (Ref. sections 3.2.1 and 3.4).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
512KB	4MB	UJ5071	289-0962	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 5.5.5).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-E (Ref. section 5.5.6).
4) Power-up system (Ref. sections 3.2.1 and 3.4).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
512KB	8MB	UJ5072	289-0961	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 5.5.5).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-F (Ref. section 5.5.6).
4) Power-up system (Ref. sections 3.2.1 and 3.4).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
1MB	2MB	UJ5059	289-0960	Kit includes one (1) new PAL chip for memory addressing (P/N 377-3486) and two (2) 1MB x 9 SIMMs Modules (P/N 377-4513).

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 5.5.5).
3) Replace the PAL chip at PCB location L2 with the PAL chip supplied in kit (Ref. Figure B-1).
4) Remove the four (4) 256KB SIMMs Modules (Ref. Figures B-1 and B-2).
5) Insert two (2) 1MB SIMMs Modules from the kit into the first two (2) empty SIMMs sockets starting at the bottom of the SIMMs connectors (Ref. Figures B-1 and B-3).
6) Position jumper J2 correctly to reflect the 1MB SIMMs Module installation (Ref. Figure B-4).
7) Install the CPU/Memory PCB (Ref. section 5.5.6).
8) Power-up system (Ref. sections 3.2.1 and 3.4).
9) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
1MB	4MB	UJ5060	289-0959	Kit includes one (1) new PAL chip for memory addressing (P/N 377-3487) and four (4) 1MB x 9 SIMMs Modules (P/N 377-4513).

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 5.5.5).
3) Replace the PAL chip at PCB location L2 with the PAL chip supplied in kit (Ref. Figure B-1).
4) Remove the four (4) 256KB SIMMs Modules (Ref. Figures B-1 and B-2).
5) Insert four (4) 1MB SIMMs Modules from the kit into the first four (4) empty SIMMs sockets starting at the bottom of the SIMMs connectors (Ref. Figures B-1 and B-3).
6) Position jumper J2 correctly to reflect the 1MB SIMMs Module installation (Ref. Figure B-4).
7) Install the CPU/Memory PCB (Ref. section 5.5.6).
8) Power-up system (Ref. sections 3.2.1 and 3.4).
9) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
1MB	8MB	UJ5061	289-0958	Kit includes one (1) new PAL chip for memory addressing (P/N 377-3488) and eight (8) 1MB x 9 SIMMs Modules (P/N 377-4513).

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 5.5.5).
3) Replace the PAL chip at PCB location L2 with the PAL chip supplied in kit (Ref. Figure B-1).
4) Remove the four (4) 256KB SIMMs Modules (Ref. Figure B-1 and B-2).
5) Insert eight (8) 1MB SIMMs Modules from the kit into the eight (8) empty SIMMs sockets at the bottom of the SIMMs PCB connectors (Ref. Figures B-1 and B-3).
6) Position jumper J2 correctly to reflect the 1MB SIMMs Module installation (Ref. Figure B-4).
7) Install the CPU/Memory PCB (Ref. section 5.5.6).
8) Power-up system (Ref. sections 3.2.1 and 3.4).
9) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
2MB	4MB	UJ5062	289-0957	Kit includes one (1) new PAL chip for memory addressing (P/N 377-3487) and two (2) 1MB x 9 SIMMs Modules (P/N 377-4513).

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 5.5.5).
3) Replace the PAL chip at PCB location L2 with the PAL chip supplied in kit (Ref. Figure B-1).
4) Insert the two (2) additional 1MB x 9 SIMMs Modules from the kit into the first two (2) empty SIMMs sockets at the bottom of the SIMMs connectors (Ref. Figures B-1 and B-3).
5) Install the CPU/Memory PCB (Ref. section 5.5.6).
6) Power-up system (Ref. sections 3.2.1 and 3.4).
7) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
2MB	8MB	UJ5063	289-0956	Kit includes one (1) new PAL chip for memory addressing (P/N 377-3488) and six (6) 1MB x 9 SIMMs Modules (P/N 377-4513).

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 5.5.5).
3) Replace the PAL chip at PCB location L2 with the PAL chip supplied in kit (Ref. Figure B-1).
4) Insert the six (6) additional 1MB x 9 SIMMs Modules from the kit into the first six (6) empty SIMMs sockets at the bottom of the SIMMs connectors (Ref. Figures B-1 and B-3).
5) Install the CPU/Memory PCB (Ref. section 5.5.6).
6) Power-up system (Ref. sections 3.2.1 and 3.4).
7) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
4MB	8MB	UJ5064	289-0955	Kit includes one (1) new PAL chip for memory addressing (P/N 377-3488) and four (4) 1MB x 9 SIMMs Modules (P/N 377-4513).

To accomplish upgrade, perform following:
1) Power-down system (Ref. sections 3.2.1 and 3.5).
2) Remove presently installed CPU/Memory PCB from system (Ref section 5.5.5).
3) Replace the PAL chip at PCB location L2 with the PAL chip supplied in kit (Ref. Figure B-1).
4) Insert the four (4) additional 1MB x 9 SIMMs Modules from the kit into the first four (4) empty SIMMs sockets at the bottom of the SIMMs connectors (Ref. Figures B-1 and B-3).
5) Install the CPU/Memory PCB (Ref. section 5.5.6).
6) Power-up system (Ref. sections 3.2.1 and 3.4).
7) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

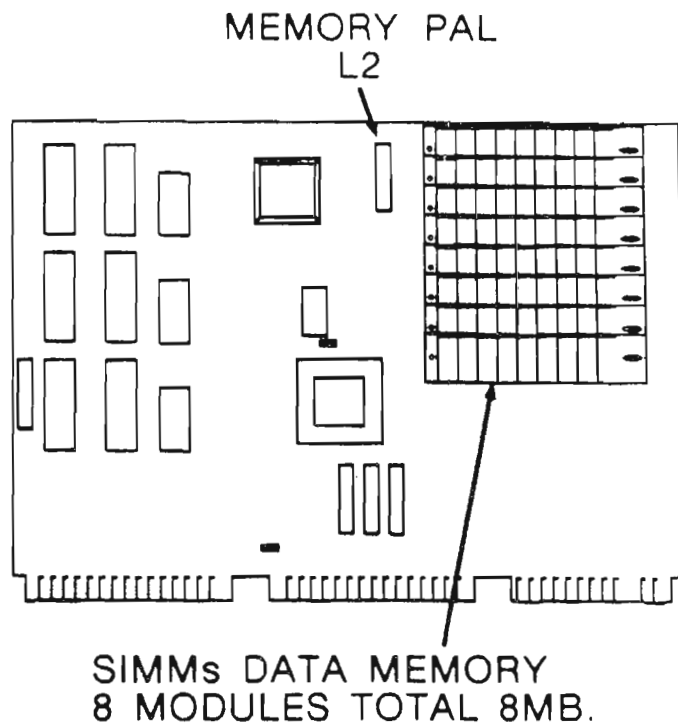## 3.1.2   Enhanced Micro VP CPU/Memory PCB Upgrades (Cont'd)

MEMORY PAL
L2

SIMMs DATA MEMORY
8 MODULES TOTAL 8MB.

Figure B-1.   Enhanced Micro VP CPU/Memory PCB Components Layout

1 Locate SIMMs Memory section of CPU board

2 Remove SIMMs Module by spreading both locking connector posts.

3 Grasp both SIMMs Module corners and pull SIMMs Module forward.

4 Lift SIMMs Module straight up and out of SIMM connector.
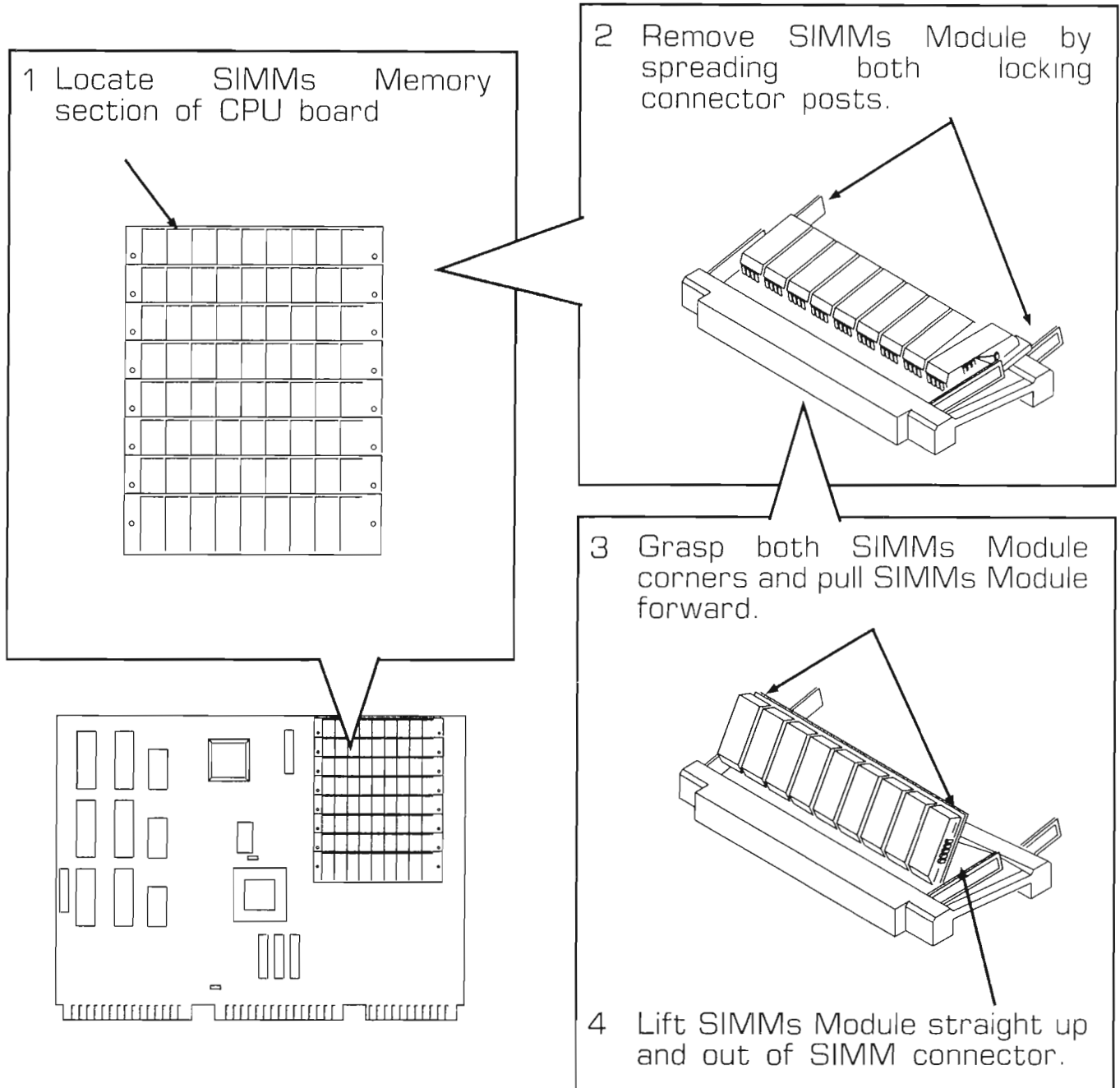
Figure B-2. Enhanced Micro VP CPU/Memory PCB SIMMs Module Removal

1 Locate   SIMMs   Memory
section of CPU Board.

2 Insert   SIMMs   Module   into
SIMMs connector at 30° angle.

3 Place thumbs on both SIMMs
Module corners.

4 Push SIMMs Module down
toward board until locking posts
snap into place.
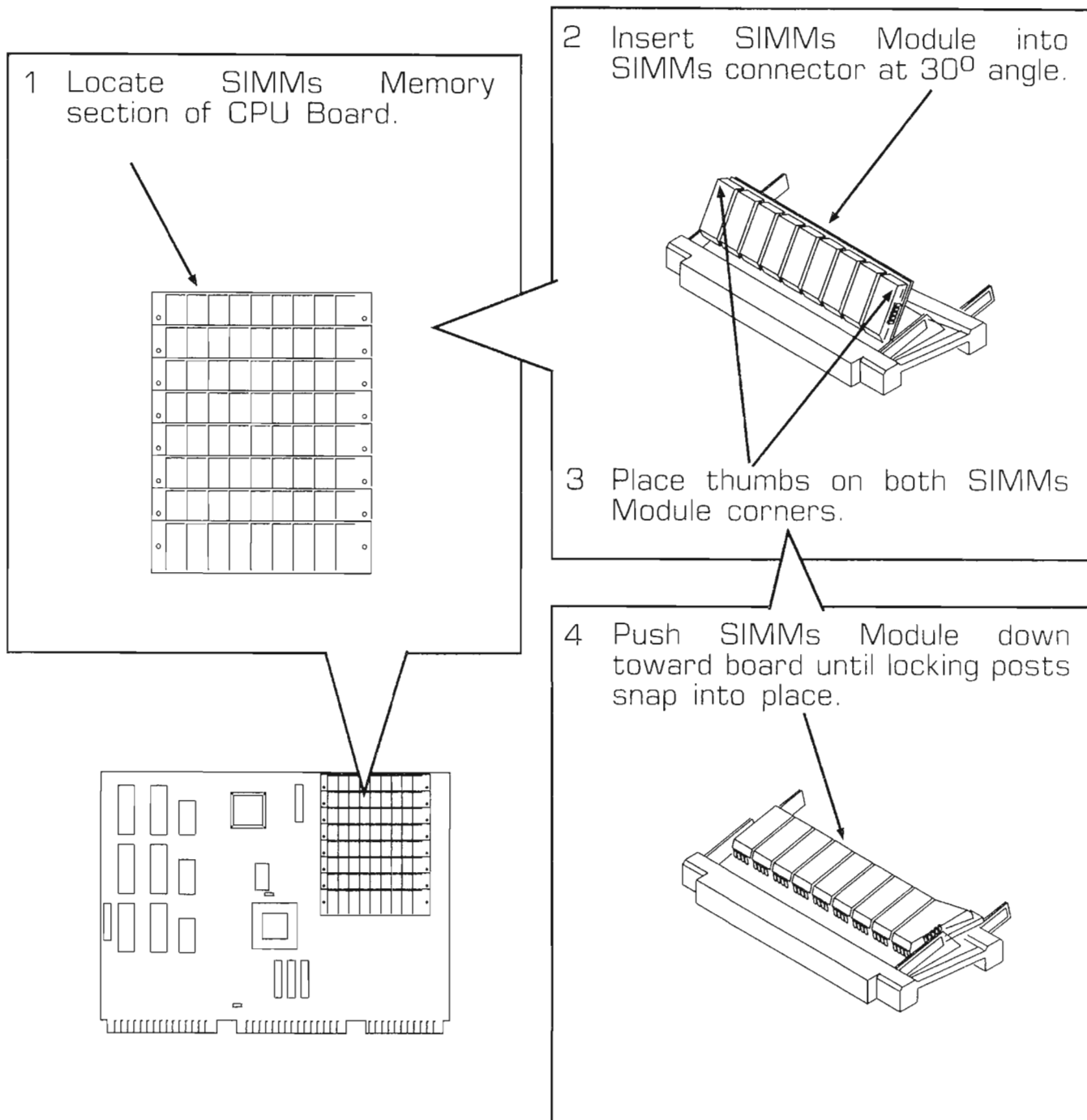
Figure B-3.   Enhanced Micro VP CPU/Memory PCB SIMMs Module Insertion

SIMMs Memory Selection Jumper (J2):

• If 256KB SIMM size (memory size of 1MB or less) is used:

1   Mount jumper on right side (shorting pins 2 and 3 together).

• If 1MB SIMM size is used:

1   Mount jumper on left side (shorting pins 1 and 2 together).

CPU Clock Jumper (J1):

Mount J2 Memory selection jumper as follows:

2   J1 jumper must be connected for proper operation of CPU and CPU Clock functions.
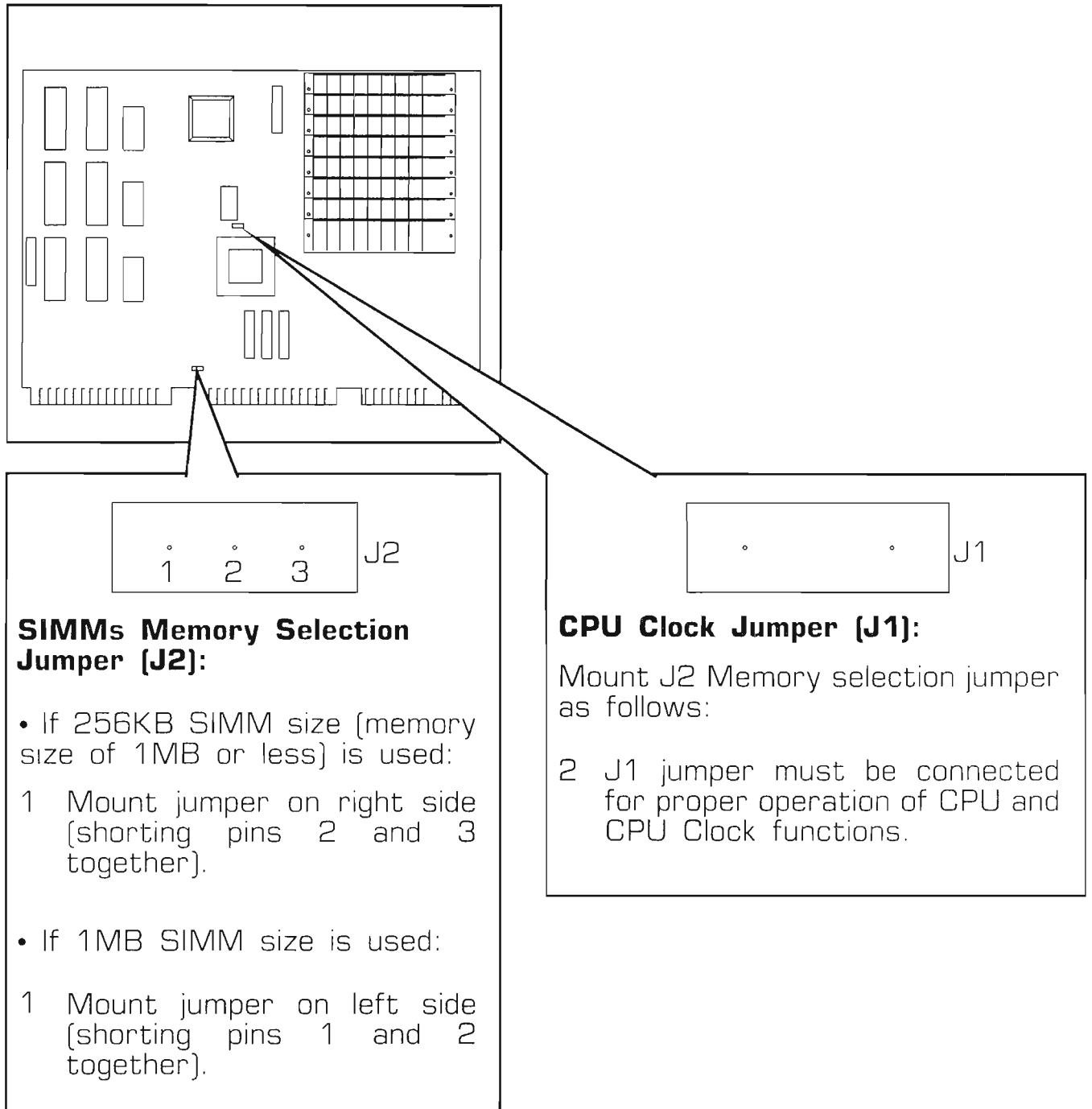
Figure B-4.   Enhanced Micro VP SIMMs CPU/Memory PCB Jumpers

4.1 FUNCTIONAL DESCRIPTION

4.1.1 Introduction

The overall operation of the Micro VP-1 and VP-2 is controlled by the CPU/Memory Board (P/N 210-8034-1, 210-8034-2 or 210-8937-A thru F). This new Enhanced CPU/Memory PCB increases the maximum system memory to 8MB. This increased memory allows the user to allocate up to 1MB for user partitions. Memory not allocated to user partitions will be reserved for RAMDISK. This section provides a brief description of this CPU.

4.2 CPU FUNCTIONAL THEORY

4.2.1   128KB Data Memory (Micro VP - Original CPU PCB)

With a 128K Data Memory configuration there are two banks, with 9 chips in each bank, for a total of 18 chips. Each chip contains 64K x 1 bit which produces 64K x 9 bits [8 data bits plus 1 parity bit] in each bank. Together the two banks produce 128K 8 bit bytes plus parity. Operation of the data memory is controlled by the Data Memory Controller chip.
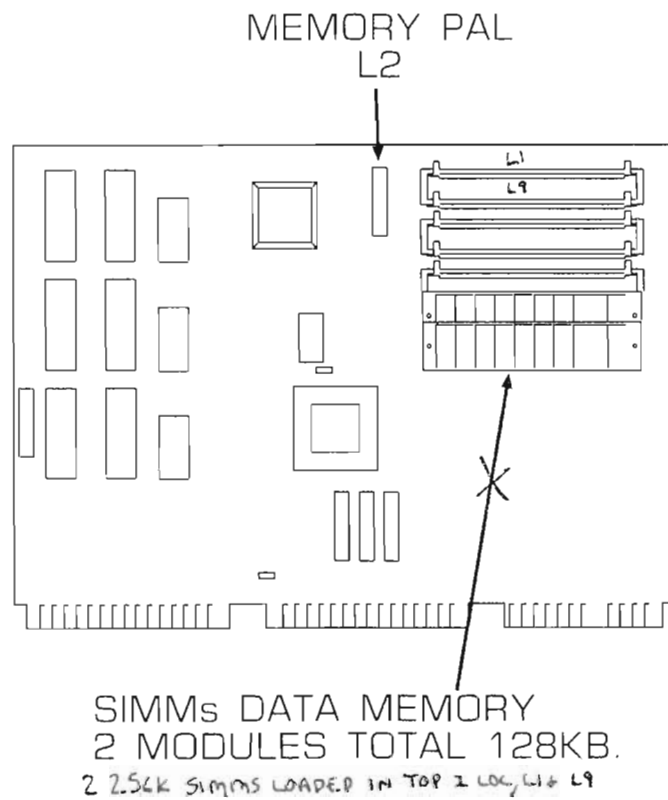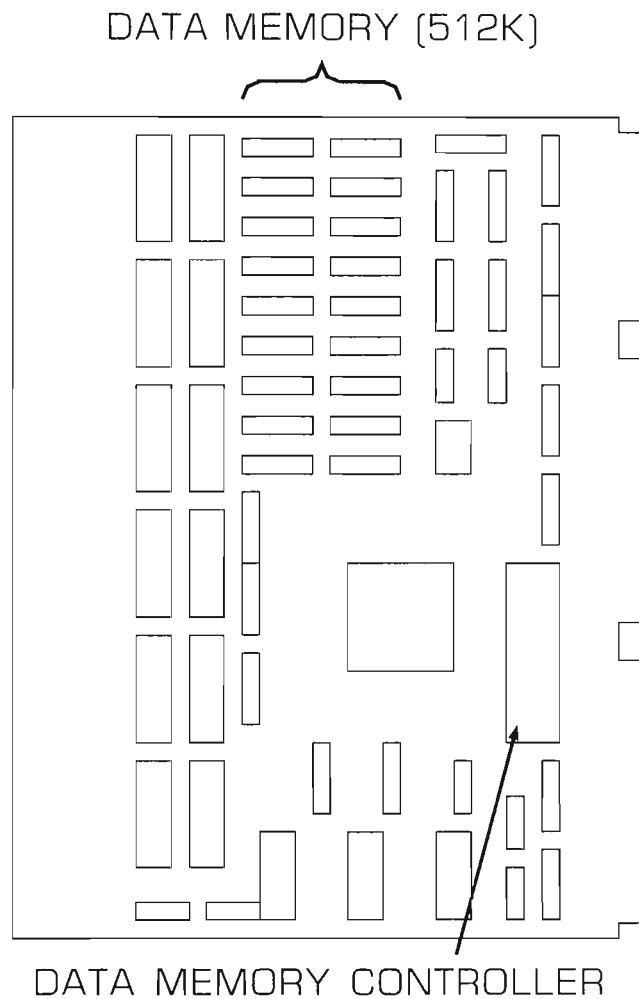
DATA MEMORY [128K]

DATA MEMORY CONTROLLER
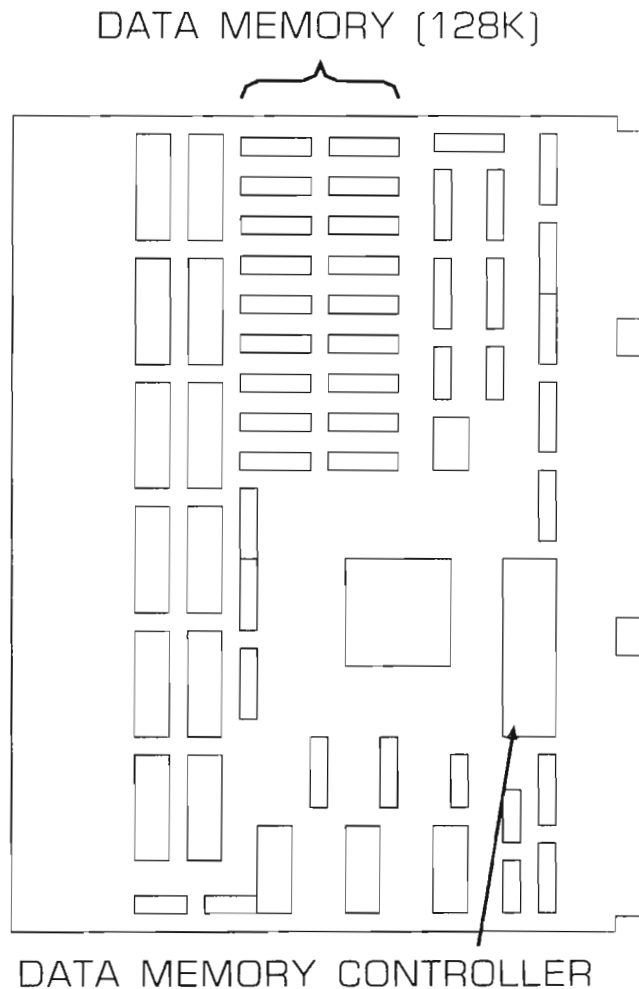
Figure B-5. Micro VP Original CPU/Data Memory PCB (128KB)

4.2.2 128KB Data Memory (Micro VP – Enhanced CPU PCB)

   With a 128K Data Memory configuration there are two 256KB SIMMs Modules,
with 9 SIMMs chips on each module. Each SIMMs chip contains 256K x 1 bit
which produces 256K x 9 bits [8 data bits plus 1 parity bit] on each module.
Together the two SIMMs modules produce ~~512~~ ~~128~~K 8 bit bytes plus parity, *BUT* Data   *BUT ONLY 128K IS ADDRESSABLE BECAUSE OF THE PAL CHIP.*
Memory addressing is accomplished by the PAL chip at CPU board location L2.

MEMORY PAL
L2

SIMMs DATA MEMORY
2 MODULES TOTAL 128KB.
2 256K SIMMS LOADED IN TOP 2 LOC, L4 & L9

Figure B-6. Micro VP Enhanced CPU/Data Memory PCB (128KB)

4.2.3 512KB Data Memory (Micro VP – Original CPU PCB)

With a 512K Data Memory configuration there are two banks, with 9 chips in each bank, for a total of 18 chips. Each chip contains 256K x 1 bit which produces 256K x 9 bits [8 data bits plus 1 parity bit] in each bank. Together the two banks produce 512K 8 bit bytes plus parity. Operation of the data memory is controlled by the Data Memory Controller chip.

DATA MEMORY (512K)

DATA MEMORY CONTROLLER

Figure B-7. Micro VP Original CPU/Data Memory PCB (512KB)

4.2.4 512KB Data Memory (Micro VP - Enhanced CPU PCB)

With a 512K Data Memory configuration there are two 256K SIMMs Modules, with 9 SIMMs chips on each module. Each SIMMs chip contains 256K x 1 bit which produces 256K x 9 bits [8 data bits plus 1 parity bit] on each module. Together the two SIMMs modules produce 512K 8 bit bytes plus parity. Data Memory addressing is accomplished by the PAL chip at CPU board location L2.
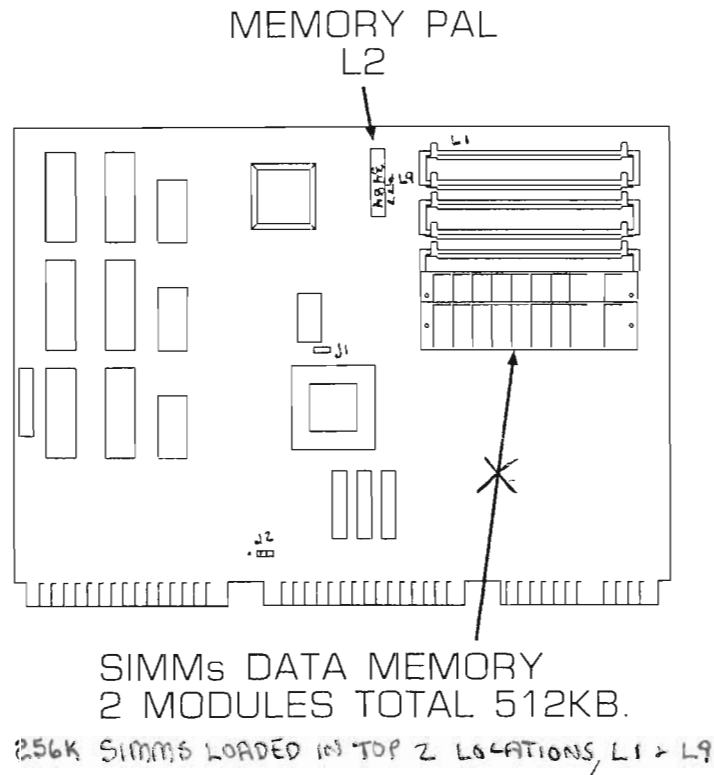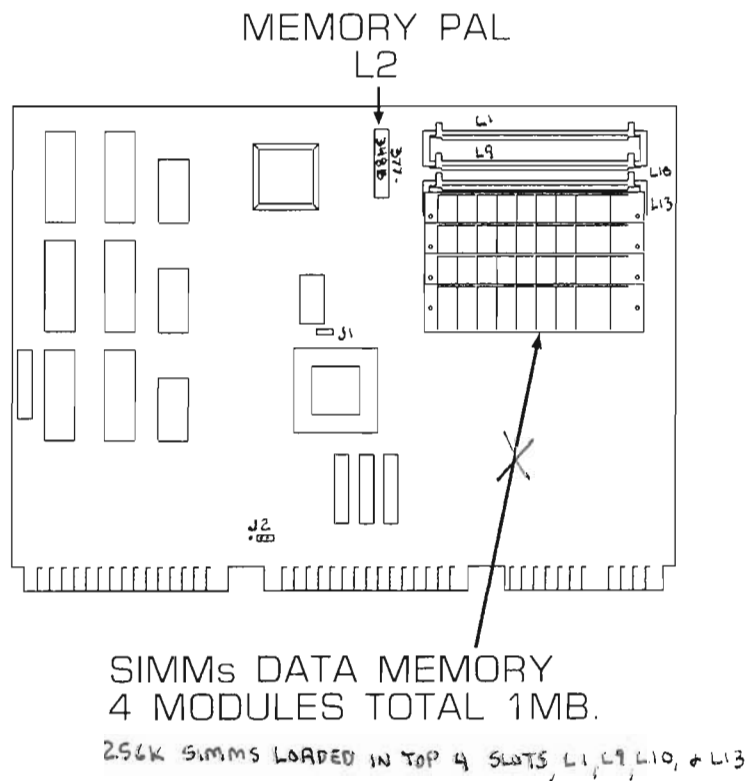
MEMORY PAL
L2

SIMMs DATA MEMORY
2 MODULES TOTAL 512KB.
256K SIMMS LOADED IN TOP 2 LOCATIONS, L1 + L9

Figure B-8. Micro VP Enhanced CPU/Data Memory PCB (512KB)

4.2.5 1MB Data Memory (Micro VP - Enhanced CPU PCB)

With a 1MB Data Memory configuration there are four 256K SIMMs Modules, with 9 SIMMs chips on each module. Each SIMMs chip contains 256K x 1 bit which produces 256K x 9 bits [8 data bits plus 1 parity bit] on each module. Together the four SIMMs modules produce 1MB 8 bit bytes plus parity. Data Memory addressing is accomplished by the PAL chip at CPU board location L2.
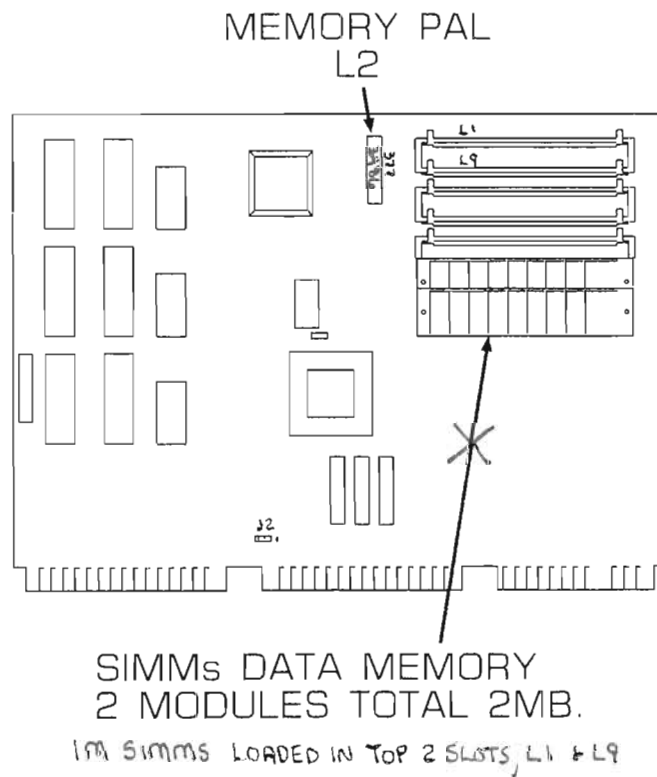
MEMORY PAL
L2

SIMMs DATA MEMORY
4 MODULES TOTAL 1MB.

256K SIMMS LOADED IN TOP 4 SLOTS L1,L9,L10, & L13

Figure B-9. Micro VP Enhanced CPU/Data Memory PCB (1MB)

4.2.6   2MB Data Memory (Micro VP – Enhanced CPU PCB)

   With a 2MB Data Memory configuration there are two 1MB SIMMs Modules, with 9 SIMMs chips on each module. Each SIMMs chip contains 1MB x 1 bit which produces 1MB x 9 bits [8 data bits plus 1 parity bit] on each module. Together the two SIMMs modules produce 2MB 8 bit bytes plus parity.   Data Memory addressing is accomplished by the PAL chip at CPU board location L2.
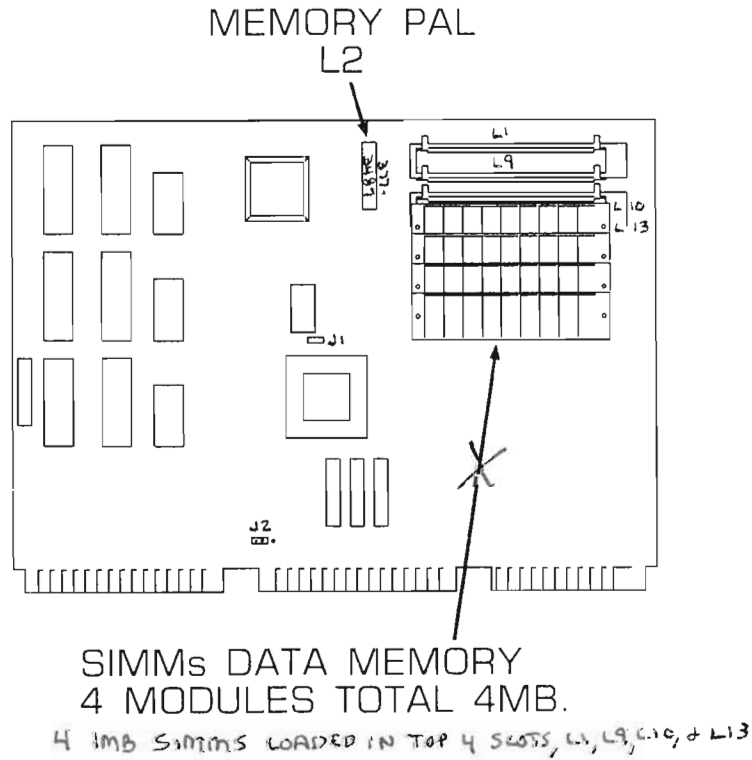
MEMORY PAL
L2

SIMMs DATA MEMORY
2 MODULES TOTAL 2MB.

Im SIMMS LOADED IN TOP 2 SLOTS, LI & L9

Figure B–10.   Micro VP Enhanced CPU/Data Memory PCB (2MB)

4.2.7 4MB Data Memory (Micro VP - Enhanced CPU PCB)

With a 4MB Data Memory configuration there are four 1MB SIMMs Modules, with 9 SIMMs chips on each module. Each SIMMs chip contains 1MB x 1 bit which produces 1MB x 9 bits [8 data bits plus 1 parity bit] on each module. Together the four SIMMs modules produce 4MB 8 bit bytes plus parity. Data Memory addressing is accomplished by the PAL chip at CPU board location L2.

Figure B-11. Micro VP Enhanced CPU/Data Memory PCB (4MB)

4.2.8 8MB Data Memory (Micro VP - Enhanced CPU PCB)

With a 8MB Data Memory configuration there are eight 1MB SIMMs Modules, with 9 SIMMs chips on each module. Each SIMMs chip contains 1MB x 1 bit which produces 1MB x 9 bits [8 data bits plus 1 parity bit] on each module. Together the eight SIMMs modules produce 8MB 8 bit bytes plus parity. Data Memory addressing is accomplished by the PAL chip at CPU board location L2.
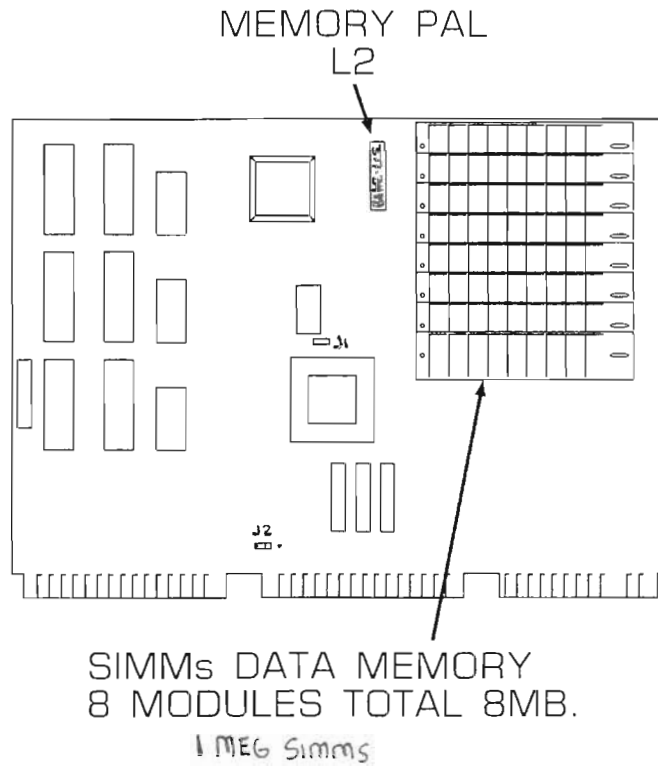
MEMORY PAL
L2

SIMMs DATA MEMORY
8 MODULES TOTAL 8MB.
1 MEG Simms

Figure B-12. Micro VP Enhanced CPU/Data Memory PCB (8MB)

4.3   Memory Partitioning

When using the 512KB Memory, the maximum memory partition size is 28KB if all 16 partitions are used. When Main Memory is increased to 1MB, the maximum memory partition size will increase to 56KB.

4.4   Enhanced CPU/Memory Board Block Diagram

The Enhanced CPU/Memory Board Block Diagram is not included in this edition of the Micro VP Computer System Manual. This information will be provided in a subsequent edition.

Programmable Array Logic (PAL):

Data Memory Addressing is accomplished on the Enhanced CPU Board via PAL circuitry at CPU Board location L2. PAL logic chips are programmable 20 pin DIP packaged AND array that provides inputs to a fixed OR array. Based on proven fuseable-link technology, PALs solve three problem areas which are:

- Decreasing board space due to increasing board density

- Inventory reduction due to less need for logic chips

- PALs accept fast internal design changes limited to fuseable links

Programmable Array Logic (PAL) chips greatly enhance 32 bit design, performance and unique operation of 16 bit processors.

5.1   ILLUSTRATED PARTS

5.1.1   System Components (Sheet 1 of 3)

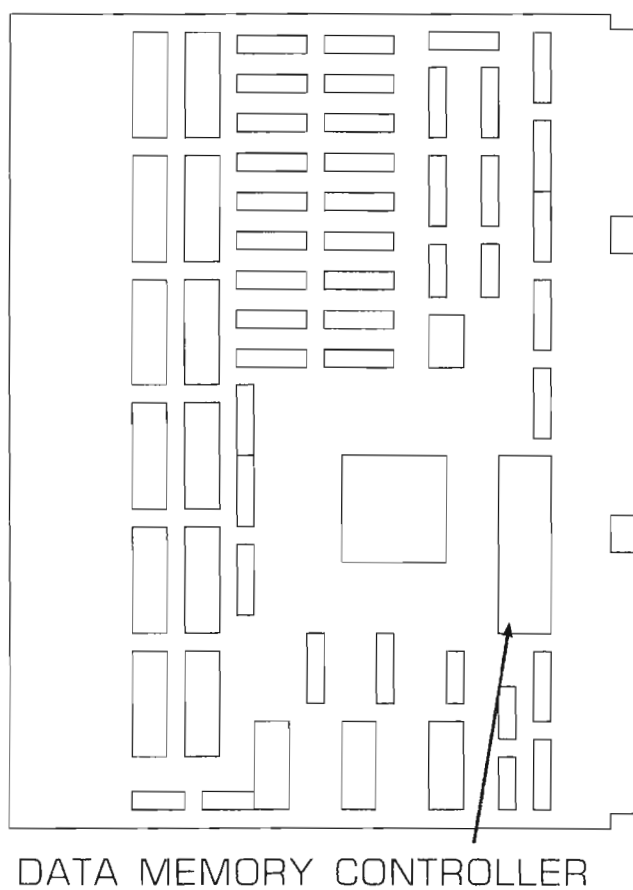| Item	Part Number	Description
1	210-8034-1	128KB CPU Board (Original CPU)
2	210-8034-2	512KB CPU Board (Original CPU)

DATA MEMORY CONTROLLER

Figure B-13.   Micro VP Computer System Components

5.1   ILLUSTRATED PARTS

5.1.1   System Components (Sheet 2 of 3)

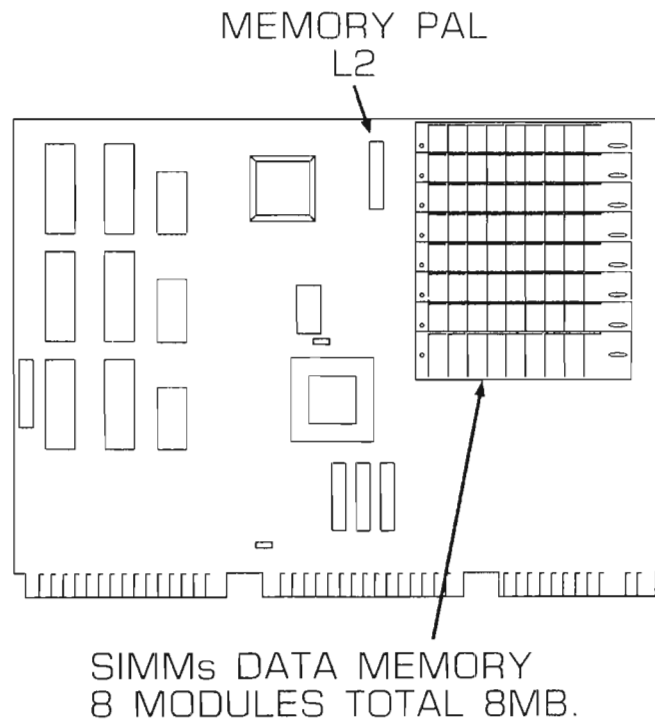| Item	Part Number	Description
3	210-8937-A	128KB CPU Board (Enhanced CPU Model)
4	210-8937-B	512KB CPU Board (Enhanced CPU Model)
5	210-8937-C	1MB CPU Board (Enhanced CPU Model)
6	210-8937-D	2MB CPU Board (Enhanced CPU Model)
7	210-8937-E	4MB CPU Board (Enhanced CPU Model)
8	210-8937-F	8MB CPU Board (Enhanced CPU Model)

MEMORY PAL
L2

SIMMs DATA MEMORY
8 MODULES TOTAL 8MB.

Figure B-14.   Micro VP Computer System Components

5.1.1 System Components (Sheet 3 of 3)

| Item	Part Number	Description
9	377-4508	256KB SIMMs CPU Memory Module
10	377-4513	1MB SIMMs CPU Memory Module
11	377-3483	Memory PAL (L2) (128KB CPU Memory Board)
12	377-3484	Memory PAL (L2) (512KB CPU Memory Board)
13	377-3485	Memory PAL (L2) (1MB CPU Memory Board)
14	377-3486	Memory PAL (L2) (2MB CPU Memory Board)
15	377-3487	Memory PAL (L2) (4MB CPU Memory Board)
16	377-3488	Memory PAL (L2) (8MB CPU Memory Board)

MEMORY PAL
L2

SIMMs DATA MEMORY
8 MODULES TOTAL 8MB.
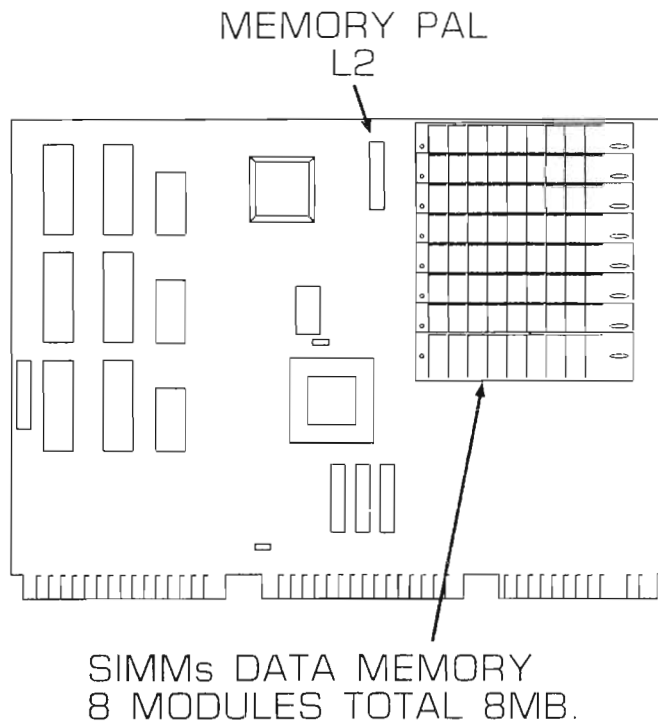
Figure B-15. Micro VP Computer System Components