

2200 COMPUTER

Model: SVP



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PREFACE

This documentation package for the 2200SVP Computer is comprised of five separate publications which include a Product Maintenance Manual (PMM), three Product Service Notices (PSN's), and a Publication Update Bulletin (PUB). The three PSN's and the PUB are inserted at the end of the PMM. A listing of all these documents is as follows:

- 1. PMM 729-0935: 2200SVP Computer
- 2. PSN 729-0935-1: 2200SVP Option W Board Installation
- 3. PSN 729-0936: 2200 SVP WL# 210-7890-A Dual Diskette Drive Controller
 --Setting Device Address Switch SW1
 --PROM Part Numbers
- 4. PSN 729-0945: 2200SVP: WL# 210-7890-A VCO Adjustment
- 5. PUB: 2200LVP/SVP: WP# 210-8694/8794 PLL Adjustment

The scope of this documentation package reflects the type of maintenance philosophy selected for this product (swap unit, printed circuit assembly, chip level or any combination thereof). It's purpose is to provide the Wang-trained Customer Engineer (CE) with instructions to operate, troubleshoot and repair the 2200SVP Computer.

Second Edition (March 1984)

This edition of the 2200SVP Computer PMM obsoletes document numbers 729-0935, 729-0935-1, 729-0936, and 729-0945. The material in this document may only be used for the purpose stated in the Preface. Updates and/or changes to this document will be published as PSN's or subsequent editions.

This document is the property of Wang Laboratories, Inc. All information contained herein is considered company proprietary, and its use is restricted solely for the purpose of assisting the Wang-trained CE in servicing this Wang product. Reproduction of all or any part of this document is prohibited without the prior consent of Wang Laboratories, Inc.

This manual provides field personnel with information needed to unpack, install, operate, and maintain the 2200SVP Computer.

Following is a list of documentation categories referenced by this manual. Documentation from these other categories is required for the performance of certain maintenance tasks related to the 2200SVP Computer. Be sure to check for other required documentation at the beginning of each section.

Model 2200LVP Product Maintenance Manual -- IV.A.3 Site Planning & Preparation -- I.A.7 2227B, 2228B/C/D Telecommunications Controllers -- IV.B.2 I/O Controllers: Setting Device Address Switches -- IV.B.1 I/O Cable Connector Installation -- I.B.O 2236DE Interactive Terminal -- III.D.1 DSDD Diskette Drive (SA850) -- III.A.11 Winchester Disk Drive (SA1002) -- III.A.12 2211M, 2221M Printer Multiplexers -- III.C.0 2221W Matrix Printer -- III.C.3 2231W, -1, -2, -3, -6 Matrix Printers -- III.C.4 2251 Matrix Printer -- III.C.11 2261W Matrix Printer -- III.C.2 2263W-1, -2, -3 Chain Printers -- III.C.1 2271 Bi-Directional Writer -- III.C.8 2271P Bi-Directional Writer/Plotter -- III.C.8 2272-2 Drum Plotter -- III.C.15 2273-1, -2 Band Printers III.C.10 2281 Diablo Daisy Printer -- III.C.7 2281P Diablo Daisy Printer/Plotter -- III.C.7 2281W/WC Wang Daisy Printers -- III.C.6 2282 Graphic CRT Plotter -- III.D.1 IP41L Image Printer III.C.13 System Diagnostics -- IV.C.1 System Conversions/Upgrades -- I.B.2 2200SVP Operating System -- IV.C.4 Programming the 2200SVP -- IV.C.2 System Utility Programs -- IV.C.3 Telecommunications Software -- IV.C.3

2200SVP COMPUTERS

MODEL 2200SVP-8X (WL NO. 177-3238 FOR 60 Hz; WL NO. 157-3238 FOR 50 Hz) MODEL 2200SVP-16X (WL NO. 177-3239 FOR 60 Hz; WL NO. 157-3239 FOR 50 Hz) MODEL 2200SVP-8A (WL NO. 177-3240 FOR 60 Hz; WL NO. 157-3240 FOR 50 Hz) MODEL 2200SVP-16A (WL NO. 177-3241 FOR 60 Hz; WL NO. 157-3241 FOR 50 Hz) MODEL 2200SVP-8B (WL NO. 177-3242 FOR 60 Hz; WL NO. 157-3242 FOR 50 Hz) MODEL 2200SVP-16B (WL NO. 177-3243 FOR 60 Hz; WL NO. 157-3243 FOR 50 Hz) MODEL 2200SVP-8C (WL NO. 177-3244 FOR 60 Hz; WL NO. 157-3244 FOR 50 Hz) MODEL 2200SVP-16C (WL NO. 177-3245 FOR 60 Hz; WL NO. 157-3245 FOR 50 Hz)

TABLE OF CONTENTS

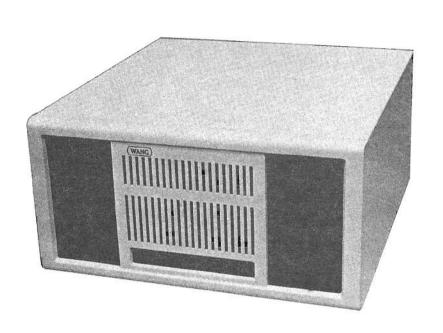
	PAGE
SECTION 1 GENERAL DESCRIPTION	1-1
1.1 SYSTEM OVERVIEW	1-1
1.2 COMPONENTS OF THE 2200SVP SYSTEM	1-1
1.2.1 CENTRAL PROCESSING UNIT	1-2
1.2.2 DSDD DISKETTE DRIVE (Shugart SA850)	1-3
· · · · · · · · · · · · · · · · · · ·	1-3
1.2.3 WINCHESTER DISK DRIVE (Shugart SA1002)	1-4
1.2.4 DISK/DISKETTE DRIVE PROCESSING UNITS	
1.2.5 2236DE INTERACTIVE TERMINAL	1-5
1.2.6 PRINTERS/PLOTTERS	1-5
1.2.7 INPUT/OUTPUT CONTROLLERS	1-6
1.2.8 TELECOMMUNICATIONS CONTROLLERS	1-6
1.3 2200SVP FEATURES	1-8
1.3.1 BASIC-2 LANGUAGE	1-8
1.3.2 GENERAL INPUT/OUTPUT INSTRUCTIONS	1-8
1.3.3 EDITING	1-8
1.3.4 PROGRAM DEBUGGING	1-9
1.3.5 ERROR CONTROL	1-10
1.3.6 PROGRAMMABLE INTERRUPT	1-10
1.3.7 SYSTEM UTILITIES	1-10
1.4 MODEL CONFIGURATION	1-12
1.5 SPECIFICATIONS	1-1
1.5.1 2200SVP CPU	1-1
1.5.2 DISK DRIVES	1-1
1.5.2 DIDE DELVES	1-1
SECTION 2 SYSTEM PROGRAMMING AND OPERATION	2-1
SECTION 3 BOOTSTRAP OPERATION	3–1
3.1 BOOTSTRAP	3-1
	3-1
3.1.1 MASTER INITIALIZATION	_
3.1.2 RESET	3-2
3.1.3 CONTROL AND DATA MEMORY PARITY ERRORS	3-3
3.1.4 LOADING SYSTEM FILES	3-3
3.2 BOOTSTRAP ERROR MESSAGES AND RECOVERY	3-4
3.2.1 INITIALIZATION ERRORS	3-4
3.2.2 RESET ERRORS	3-7
3.2.3 SYSTEM ERRORS	3-1
3.2.3.1 CONTROL MEMORY ERRORS	3-1
3.2.3.2 DATA MEMORY ERRORS	3-1
3.2.3.3 DISK ERRORS	3-1
SECTION 4 OPERATION AND PROGRAMMING CONSIDERATIONS	4-1
4.1 POWER-ON	4-1
4.2 LOADING THE OPERATING SYSTEM	4-1
4.3 COPYING THE SYSTEM DISK	4-3
	4-4
4.4 PROGRAMMING CONSIDERATIONS	
SECTION 5 HARDWARE THEORY OF OPERATION	5-1
5.1 CENTRAL PROCESSING UNIT	5-1

5.2 DISK/DISKETTE PROCESSING UNIT	5-1
5.3 DUAL DISKETTE PROCESSING UNIT	
5.3.1 Z80A INPUT/OUTPUT PORT ADDRESSES	
5.3.2 2200SVP CPU/DPU COMMUNICATION	5-2
5.3.2.1 CPU-TO-DPU	
5.3.2.2 DPU-TO-CPU	5-6
SECTION 6 SITE PREPARATION	6-1
SECTION 7 UNPACKING AND RECEIVING INSPECTION	7-1
7.1 TOOLS REQUIRED	7-1
7.2 PRE-UNPACKING INSPECTION	7-1
7.3 UNPACKING INSTRUCTIONS	
SECTION 8 INSTALLATION	8-1
0 4 DDD THOMAS ARTON THADDOMION	8-1
8.1 PRE-INSTALLATION INSPECTION	8-2
8.2 INITIAL SETUP	
8.2.1 2200SVP CIRCUIT BOARDS (LOADING)	8-9
8.2.2 2200SVP CABLE CONNECTIONS	8-17
8.2.3 2200SVP POWER SUPPLY AC INPUT VOLTAGE SELECTION	8-17
8.2.4 TELECOMMUNICATIONS CONTROLLERS	8-25
8.2.5 DISK DRIVES	8-25
8.2.6 2236DE INTERACTIVE TERMINAL	8-25
8.2.7 PERIPHERALS	8-25
8.3 INSTALLATION AND POWER-ON PROCEDURES	8-25
SECTION 9 DIAGNOSTICS	9-1
SECTION 10 PREVENTIVE MAINTENANCE	10-1
SECTION 11 REMOVAL/REPLACEMENT AND ADJUSTMENT PROCEDURES	11-1
11.1 RECOMMENDED TEST EQUIPMENT/TOOL LIST	11-1
11.2 CPU VOLTAGE ADJUSTMENT PROCEDURE	
11.3 DISK/DISKETTE PROCESSING UNIT PLO ADJUSTMENT	
11.4 DUAL DISKETTE PROCESSING UNIT PLO ADJUSTMENT	11-5
11.5 DSDD DISKETTE DRIVE ADJUSTMENTS/ALIGNMENTS	11-5
11.6 REMOVAL/REPLACEMENT PROCEDURES	11-5
11.6.1 TOP COVER	11-5
11.6.2 CIRCUIT BOARD RETAINER	11-5
11.6.3 DISKETTE DRIVE	11-6
11.6.4 WINCHESTER DRIVE	11–6
11.6.5 HEATSINK ASSEMBLY	11-7
SECTION 12 TROUBLESHOOTING	12/13-1
SECTION 13 CONVERSIONS	12/13-1
SECTION 14 PARTS LIST	14-1
SECTION 15 BILL OF MATERIALS	15-1
APPENDIX A 2200SVP ERROR CODES	A-1

APPENDIX B	MECHANICAL DR.	AWINGS	B/C-1
APPENDIX C	SCHEMATICS	• • • • • • • • • • • • • • • • • • • •	B/C-1

LIST OF FIGURES

FIGURE		PAGE
1-1	TYPICAL 2200SVP SYSTEM CONFIGURATION	1-7
5-1	DUAL-DISKETTE PROCESSING UNIT BLOCK DIAGRAM	5-8
8-1	2200SVP (FRONT VIEW)	
8-2	2200SVP (REAR VIEW)	8-4
8-3	2200SVP WITH 3-BOARD DPU (INTERNAL FRONT VIEW)	8-5
8-4	2200SVP WITH 1-BOARD DPU (INTERNAL FRONT VIEW)	8-6
8-5	2200SVP (INTERNAL LEFT VIEW)	8-7
8-6	2200SVP (INTERNAL RIGHT VIEW)	8-8
8-7	CIRCUIT BOARD LOADING (3-BOARD DPU)	8-9
8-7A	CIRCUIT BOARD LOADING (1-BOARD DPU)	8-10
8-8	WL NO. 210-7694 2200/DISK INTERFACE (DPU)	8-12
8-9	WL NO. 210-7696-X MICROCOMPUTER/MEMORY (DPU)	8-13
8-10	WL NO. 210-7789-A TERMINAL/PRINTER CONTROLLER	8-15
8-11	WL NO. 210-7890-A DUAL DSDD DISKETTE DRIVE CONTROLLER	8-16
8-12	DISK/DISKETTE DRIVE I/O CABLE CONNECTIONS	8-18
8-13	DSDD DISKETTE DRIVE CABLE CONNECTIONS	8-19
8-14	WINCHESTER DISK DRIVE I/O CABLE CONNECTIONS	8-20
8-15	WINCHESTER DISK DRIVE POWER CABLE CONNECTIONS	8-21
8-16	DISK/DISKETTE DRIVE DC POWER HARNESS CONNECTION	8-22
8-17	TELECOMMUNICATIONS JUMPER CABLE	8-23
8-18	AC VOLTAGE SELECTION SWITCH	8-24
11-1	DC VOLTAGE TESTPOINTS	11-3
11-2	WL NO. 210-7887 REGULATOR DC VOLTAGE POTS	11-4
11-3	COVER REMOVAL	11-8
11-4	CIRCUIT BOARD RETAINER REMOVAL; WINCHESTER DISK DRIVE REMOVAL	11-9
11-5	DSDD DISKETTE DRIVE REMOVAL: HEATSINK REMOVAL	11-10



SECTION 1

GENERAL DESCRIPTION

1.1 SYSTEM OVERVIEW

The 2200SVP is a compact, high-performance, single-user, multi-purpose, disk-based computer, programmable in Wang BASIC-2.

State-of-the-art disk technology enhances the speed and versatility of the 2200SVP. Two types of disk drives are available with the 2200SVP--a dual-sided, double-density (DSDD) diskette drive (standard), which is IBM 3741-compatible, and a fixed Winchester-style drive (optional). Both storage devices represent the latest developments in cost-effective, high-speed, mass storage peripherals.

At the customer's option, the 2200SVP may be equipped with a telecommunications controller, which allows a remote device to be connected to the Central Processing Unit. The 2200SVP processor supports both asynchronous and bisynchronous transmission.

The 2200SVP also supports a wide range of peripheral devices, such as printers with varying speeds and features, plotters, and printer/plotter multiplexers.

The 2200SVP has been designed to preserve compatibility with Wang's older, single-user systems. Because the BASIC-2 language supported on the 2200SVP is identical to BASIC-2 on the 2200VP, there is 100% software compatibility between these systems (software storage media excepted). However, differences in the number of peripherals which can be attached to the system may affect some user programs. The 2200SVP also supports earlier Wang BASIC syntax, providing a significant degree of compatibility with non-VP systems.

1.2 COMPONENTS OF THE 2200SVP SYSTEM

FIGURE 1-1, following the text in this section, illustrates a typical 2200SVP system configuration.

1.2.1 CENTRAL PROCESSING UNIT (Memory and power supply included)

The <u>Central Processing Unit</u> (CPU) controls the operation of the 2200SVP computer system, and its primary objective or function is to fetch, decode, and execute instructions that reside in memory. The CPU is basically composed of work registers, an Arithmetic/Logic Unit (ALU), and control circuitry. The work registers are normally used as temporary storage areas during program execution. The ALU contains the circuitry necessary for performing all arithmetic and logical operations required for program execution. The control circuitry allows the CPU to execute a program automatically, by reading an instruction from memory, decoding that instruction, and generating the proper control signals to execute that instruction.

The 2200SVP does not store its system programs (the BASIC-2 interpreter, Operating System, and system diagnostics) in the same memory area used to store the application software. System programs are stored in a separate memory area called <u>Control Memory</u>. The 2200SVP contains approximately 16K 24-bit words of Control Memory. When the system is powered on, the system programs are loaded into Control Memory from the system platter and remain resident in memory until the system is powered off or reinitialized. Control Memory is a separate, protected memory area which cannot be accessed by the user or the user's programs. The system programs are, therefore, always protected against accidental interference or destruction by a user program.

Data memory is the area of memory available to the user's programs and data, and therefore is sometimes called User Memory. Data memory may be 32K bytes or 64K bytes. Because the system programs are stored separately, all User Memory except for a small portion used for overhead, is available for programs and data.

The <u>power supply</u> contained in the 2200SVP chassis/cabinet not only provides the necessary voltages for the CPU and memory, but also for the I/O controllers, the disk(ette) drive(s), and the Disk/Diskette Processing Unit, all of which are contained in the 2200SVP cabinet.

The 2200SVP CPU/memory/power supply consists of the following logic boards.

MLAP	<u>DESCRIPTION</u>
210-6789-A	Memory Control
210-6790	Instruction Counter
210-6791	Stack
210-6792	ALU
210-6793-1	Registers
210-7587-1B	Data Memory32K
210-7587-1A	Data Memory64K
210-7588-A	Control Memory16K
210-7788	Motherboard
210-7887	Regulator

DESCRIPTION

NOTE:

All the boards listed above, with the exception of the motherboard and power supply regulator, are the same as those used in the 2200VP/MVP/LVP CPU's.

1.2.2 DSDD DISKETTE DRIVE (Shugart SA850)

WI#

One Shugart SA850 dual-sided, double-density (DSDD) Diskette Drive, with a storage capacity of 1 MB, comes standard with the 2200SVP (a second DSDD Drive is optional). The expanded capacity diskette drive can be used to obtain faster backup with fewer platters. In addition to its backup capabilities, the DSDD diskette also serves as the medium for transferring system software and application packages. The DSDD Diskette Drive (through the DPU) automatically recognizes single-sided, single-density, soft-sector diskettes, and single or dual-sided, double-density, soft-sector diskettes. The DSDD Diskette Drive is mounted in the compact 2200SVP cabinet, thus saving space which separate drives customarily require. The part numbers for the DSDD Drive are:

WL# 278-4015 (60 Hz version) WL# 278-4015-1 (50 Hz version)

Refer to Section 1.5.2 for disk drive capacity specifications, and sector addressing scheme. Refer to documentation category III.A.11 for more detailed information concerning the DSDD Drive.

1.2.3 WINCHESTER DISK DRIVE (Shugart SA1002)

One Shugart SA1002 Winchester Disk Drive (also referred to as the fixed-disk drive) is available as a customer selected option on the 2200SVP. Because the Winchester Drive is contained in the 2200SVP cabinet, it provides fast data access in a compact space without the mechanical or environmental problems associated with removable media-type drives. The Winchester Drive comes in one model; however, there are two capacities that may be selected: 2-MB, or 4-MB. The desired capacity, as shown on the customer's purchase order, is selected by a switch on one of the DPU boards as well as a PROM change in the DPU (ref: Section 8 for details). The part numbers for the Winchester Disk Drive are:

WL# 278-4013 (60 Hz version) WL# 278-4013-1 (50 Hz version)

Refer to Section 1.5.2 for disk drive capacity specifications, and sector addressing scheme. Refer to documentation category III.A.12 for more detailed information concerning the Winchester Drive.

1.2.4 DISK/DISKETTE PROCESSING UNITS

The 2200SVP utilizes a Disk Processing Unit (DPU), which is physically located inside the 2200SVP chassis/cabinet, to control all disk drive operations such as reading, writing, head actuator positioning, and CPU-to-disk interfacing.

There are two types of DPU's available with the 2200SVP--one that controls two DSDD Diskette Drives, and one that controls either two DSDD Diskette Drives or a DSDD Diskette Drive and a Winchester Disk Drive. (The customer has the choice of drive options.)

The dual Diskette Drives controller is composed of the WL# 210-7890-A logic board.

The dual Diskette Drives or Diskette/Winchester Drives controller is a 3-board processing unit with built-in diagnostic capability. It is composed of the following boards. (These boards are the same as those used in the 2200LVP.)

<u>WL#</u>	DESCRIPTION
210-7694 210-7695-A 210-7696-A	2200/Disk Interface Disk Controller Microcomputer/Memory (4 MB Winchester Disk Drive) Microcomputer/Memory (2 MB Winchester Disk Drive)
210-7696-B 210-7696-C	Microcomputer/Memory (2 Mb windrester bisk brive) Microcomputer/Memory (dual Diskette Drives)

1.2.5 2236DE INTERACTIVE TERMINAL

User communication with the 2200SVP is through a 2236DE Interactive Terminal with business graphics capabilities. The terminal consists of a large, easy-to-read 80 X 24-character, 12-inch CRT-screen display and a typewriter-style keyboard. Since the terminal has a provision for connection of a local printer or plotter on the back of the unit, screen dumps may be output, and all standard printing operations may be performed. The 2236DE terminal also generates extensive bar and line graphics by standard program statements. Refer to documentation category III.D.1 for more detailed information concerning the 2236DE Terminal.

1.2.6 PRINTERS/PLOTTERS

A variety of printers, offering various speeds and print types, may be used with the 2200SVP. The printers range in speed from 15 characters per second to 600 lines per minute, and include matrix, chain, band, and daisy-wheel impact types. A selection of plotters, including drum, CRT, and daisy-wheel type, and printer/plotter multiplexers are also available for use on the 2200SVP. Refer to the appropriate sections in documentation category III.C for detailed information concerning the available printers, plotters, and multiplexers listed on the following page.

NOTE:

Due to the physical structure of the SVP, only one printer or plotter is supported. An additional printer or plotter may be connected to the 2236DE Terminal if desired.

PRINTERS

2221W Matrix (120 cps)
2231W, -1, -2, -3, -6 Matrix (120 cps)
2251 Matrix (110 cps)
2261W Matrix (240 lpm)
2263W-1, -2, -3 Chain (400/600 lpm)
2271 Bi-Directional (15 cps)
2273-1, -2 Band (250/600 lpm)
2281 Diablo Daisy (30 cps)
2281W/WC Wang Daisy (40 cps)
IP41L Image (900 cps)

PLOTTERS

2271P Bi-Directional 2272-2 Drum 2281P Diablo Daisy 2282 Graphic CRT

PRINTER MULTIPLEXERS

2211M 2221M

1.2.7 INPUT/OUTPUT CONTROLLERS

The 2200SVP utilizes two I/O controllers: a WL# 210-7789 Terminal/Printer Dual Controller, and an optional telecommunications controller (see next section for TC information). The Dual Controller provides the RS-232-C compatible interface between the CPU and the 2236DE Interactive Terminal, and also between the CPU and the printer/plotter. The local terminal communicates with the controller at a baud rate of 19.2K.

1.2.8 TELECOMMUNICATIONS CONTROLLERS

The 2200SVP has four telecommunications options available: the 2227B asynchronous controller (WL# 177-2227B), the 2228B synchronous controller (WL# 177-2228B), the 2228C synchronous controller (WL# 177-2228C), and the 2228D synchronous controller (WL# 177-2228D). The TC controllers communicate with host computers, compatible terminals, or other Wang systems at speeds ranging from 1200 to 4800 baud. Emulation software packages are available for 2741, 2780, 3270, 3275, 3741, 3780, Teletype, Burroughs, and HASP protocols.

NOTE:

Due to the physical structure of the SVP, only one telecommunications controller is supported.

Refer to documentation category IV.B.2 for detailed information concerning the TC controllers.

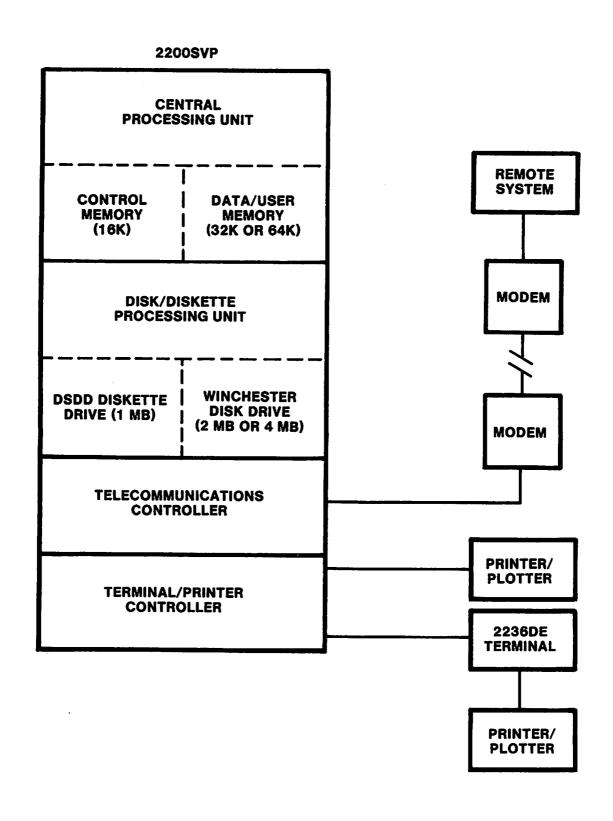


FIGURE 1-1 TYPICAL 2200SVP SYSTEM CONFIGURATION

1.3 2200SVP FEATURES

Refer to Wang BASIC-2 Language Reference Manual, WL# 700-4080 -- IV.C.2, for more detailed information concerning the topics mentioned in this Section.

1.3.1 BASIC-2 LANGUAGE

Wang BASIC-2 is a general-purpose, high-level programming language developed by Wang Laboratories. BASIC-2 is a modified version of the original Dartmouth BASIC language, offering all of the important features of the original BASIC, as well as numerous new features and enhancements. The result is a language which is both powerful and extremely versatile, well suited for both technical and commercial applications.

The BASIC-2 language consists of a large group of instructions of various types, including statements, commands, and operator-defined and system-defined functions. Of these, the two most important are statements and commands. Statements are programmable instructions used to write programs in BASIC-2. Commands are used by the operator to control CPU operations directly from the keyboard, and generally are not programmable.

1.3.2 GENERAL INPUT/OUTPUT INSTRUCTIONS

A general I/O statement (\$GIO), included in the BASIC-2 language, is provided to perform data input, data output, and I/O control operations with a programmable signal sequence. This statement supports I/O operations for the 2227B, and 2228B/C/D telecommunications controllers.

1.3.3 EDITING

The editing capabilities of the 2200SVP enable the operator to edit program lines, Immediate Mode lines, and input data values, both during and after entry. In Text Entry Mode (prior to EXECUTION of the data that was entered), the 2200SVP provides the following limited capabilities for editing the entered data.

- -- Character deletion
- -- Line erasure
- -- Program line deletion
- -- Program line replacement

The most powerful editing capabilities of the 2200SVP are accessible to the operator in Edit Mode (entered by depressing the EDIT key). Edit Mode supports the following types of editing operations.

- -- Editing a numbered program line during entry.
- -- Recalling a program line from memory and editing it.
- -- Editing an Immediate Mode line or system command during entry.
- -- Recalling from memory and editing the last executed Immediate Mode line or system command.
- -- Editing a text line consisting of data values entered in response to an INPUT request.
- -- Recalling and editing the last entered data text line.

While the CPU is in Edit Mode, Special Function keys 4-15 perform cursor positioning, data insertion, and data deletion functions.

1.3.4 PROGRAM DEBUGGING

The process of locating and identifying errors in a BASIC-2 program often involves careful analysis of the program's performance at critical stages in program execution. To aid the programmer in this task, the 2200SVP provides a variety of debugging tools that include:

- -- The STOP statement to stop program execution.
- -- The CONTINUE command to continue program execution.
- -- The HALT/STEP key to step through a program one statement at a time.
- -- The TRACE statement to show the values of variables as they change.
- -- Special forms of the LIST command to list program text, cross-references for program line numbers, variables, and marked subroutines, and the contents of the Device and Interrupt Tables.
- -- The RENUMBER command to renumber program lines.

1.3.5 ERROR CONTROL

The BASIC-2 language provides an extensive set of diagnostics designed to automatically detect and report a wide range of error conditions. The 2200SVP initially checks each text line for various types of errors as the line is entered by the programmer. Further error checking is carried out during program resolution, when the program in memory is resolved prior to execution. During program execution, the diagnostics automatically detect and report any errors that arise.

1.3.6 PROGRAMMABLE INTERRUPT

BASIC-2 also provides limited I/O interrupt handling capabilities. The programmable interrupt automatically transfers program control to an interrupt processing subroutine when an interrupt condition occurs, and subsequently returns control to the interruption point in the main program after the interrupt processing is finished. Because different devices can be assigned different priorities in the interrupt scheme, this type of interrupt is often called a "priority interrupt"; it is extremely useful in applications where temporary interruption of program processing is required for operator inquiry or maximum printer throughput.

1.3.7 SYSTEM UTILITIES

Integrated Support System (ISS) Release 5 provides support software for 2200VP/LVP/MVP/SVP systems. The major software components of ISS Release 5 are the following:

ISS Utilities

-- Operator-controlled programs which provide several standard functions necessary for a disk-based Data Processing environment. Categories of the functions available with the ISS Utilities include Copy Functions (copy/verify), Programming Functions (e.g., compression, decompression), Catalog Index Functions (e.g., sort catalog, reconstruct index), and Special Purpose Functions (e.g., disk dump, file status report).

Screen/Disk Subroutines

-- Program-controlled subroutines designed to eliminate the repetitious, detailed programming tasks otherwise required of an application programmer. These subroutines provide a simple interface between application programs and a wide range of potentially complex disk-related and operator-related tasks. There are three groups of Screen/Disk subroutines: Disk (e.g., allocate data file space, free unused sectors), Screen (e.g., data entry, postion cursor), and Translation Tables (ASCII-to-EBCDIC, EBCDIC-to-ASCII).

SORT-4 Subsystem

-- Sorts records contained within a disk data file. A user-written setup program provides the parameters for the sort and loads SORT-4 software. SORT-4 eliminates the lengthy operator/screen dialog otherwise required for the entry of the sort parameters, although the user's setup program may request operator-keyed input of appropriate parameters. When sorting is complete, SORT-4 can load a specified application program module and can be used as a subsystem to an application program.

Key File Access Method (KFAM)

-- An indexed disk-file access method which supports multistation access to data file records according to ascending, descending, or random key sequence. KFAM enables records within a disk file to be rapidly located by certain conventions associated with the particular access method used.

1.4 MODEL CONFIGURATION

The 2200SVP is identified by a model number of the format:

2200SVP-xxy

where: 2200SVP represents the CPU/DPU, a 1 MB DSDD Diskette Drive, and the cabinet.

xx is a one or two digit number representing the actual CPU user-memory size when multiplied by 4K.

- 8 32K of user-memory
- 16 64K of user-memory

y is a capital letter representing the model of the second (optional) disk drive.

- A 1 MB DSDD Diskette Drive
- B 2 MB Winchester Disk Drive
- C 4 MB Winchester Disk Drive
- X No second disk drive

A summary of all model descriptions and numbers is given in TABLE 1-1.

TABLE 1-1 SUMMARY OF 2200SVP MODEL NUMBERS

MODEL	DESCRIPTION	WL# 60 HERTZ	WL# 50 HERTZ
2200SVP-8X	32K Memory, 1 MB Diskette	177-3238	157-3238
2200SVP-16X	64K Memory, 1 MB Diskette	177-3239	157-3239
2200SVP-8A	32K Memory, dual 1 MB Diskettes	177-3240	157-3240
2200SVP-16A	64K Memory, dual 1 MB Diskettes	177-3241	157-3241
2200SVP-8B	32K Memory, 1 MB Diskette, 2 MB Winchester	177-3242	157-3242
2200SVP-16B	64K Memory, 1 MB Diskette, 2 MB Winchester	177-3243	157-3243
2200SVP-8C	32K Memory, 1 MB Diskette, 4 MB Winchester	177-3244	157-3244
2200SVP-16C	64K Memory, 1 MB Diskette, 4 MB Winchester	177-3245	157-3245

1.5 SPECIFICATIONS

1.5.1 2200SVP CPU

Size

```
Height - 12.0 in. (30.4 cm)
Width - 21.0 in. (53.5 cm)
Depth - 26.0 in. (66.0 cm)
```

Memory Cycle Time

600 nanoseconds

User Memory Size

32K bytes (standard) Expandable to 64K bytes

Control Memory Size

16K 24-bit words

Numeric Range

10⁻¹⁰⁰ to 10¹⁰⁰, floating point with 13 significant digits

Power Requirements

```
115 or 230 VAC <u>+</u> 10%
50 or 60 Hz <u>+</u> 1.0 Hz
307 Watts
```

Fuses

```
4.0 amp (SB) for 115 VAC 2.0 amp (SB) for 230 VAC
```

Operating Environment

```
Temperature - 60° to 80°F (15° to 27°C)
Relative Humdity - 35% to 65% (noncondensing--recommended)
20% to 80% (noncondensing--allowable)
```

Heat Output

1,050 Btu/hr

1.5.2 DISK DRIVES

	1 MB <u>Diskette</u>	2 MB <u>Winchester</u>	4 MB <u>Winchester</u>
Disk Surfaces	2	1	2
Sectors/Track	26	32	32
Tracks/Surface	75	##254	*** 255
Bytes/Sector	374	320	320
Bytes/Data Field	256	256	256
Sectors/Surface	2002	8128	8160
Total Sectors	*3874	8128	16320
Total Data Bytes	998,400	2,080,768	4,177,920
Sector Addresses	* 0-3873	0-8127	0-16319

- * The first track on side zero is single density, and is accessed by sector addresses 16384-16409. NOTE: The sector addresses for a single-density single-sided diskette are 16384-18386.
- ** Actually 256 -- the last track is reserved for alternate sector assignment, and the next to last track is reserved for diagnostic testing purposes.
- *** Actually 256 -- the last cylinder is reserved for alternate sector assignment and for diagnostic testing purposes.

NOTES

SECTION 2 SYSTEM PROGRAMMING AND OPERATION

Refer to the following Corporate Publications manuals for detailed information concerning system programming, system operation, and user-memory organization. These concepts are identical to those of the 2200VP CPU.

Wang BASIC-2 Language Reference Manual, WL# 700-4080 -- IV.C.2

Describes all facets of the BASIC-2 language, except disk statements. This manual includes discussions on internal memory organization and the representation of data in internal format. Also covered are system commands, errors and error recovery, addressing of peripherals, and the function and operation of each BASIC-2 statement and its proper syntax. This manual is intended for all users, but some programming experience is needed to understand the more complex statements.

Wang BASIC-2 Language Pocket Guide, WL# 700-5992 -- IV.C.2

Designed as a quick reference for BASIC-2 statement syntax. This guide is for use by those familiar with the BASIC-2 Language Reference Manual.

Wang BASIC-2 Disk Reference Manual, WL# 700-4081 -- III.A.0

Designed as a programmer's guide to disk operations on 2200VP/LVP/MVP/SVP systems, and as a reference manual for the BASIC-2 instructions governing disk operations. Syntax for all BASIC-2 disk instructions is included.

3740 Diskette Compatibility Software Rel 2 User Manual, WL# 700-4369C -- IV.C.3

Simplifies the programming requirements for applications where 3740 diskettes are accessed for data storage, retrieval, or updating. This manual includes software operating instructions for the utility programs and for application programmers.

Binary Synchronous 1 (BSC 1) TC Operator's Manual, WL# 700-4719 -- IV.C.3

Describes the operation of Wang's IBM 2780, 3780, 3741, and HASP multileaving emulators, and 2200-to-2200 communications.

3275 BSC Emulator User Manual, WL# 700-4826A -- IV.C.3

Describes software features, including modem considerations and operating instructions, to be used in conjunction with information which must be supplied by the host data center supporting 3275 communications with the Wang 2200 system.

Integrated Support System (ISS) Rel 5 User Manual, WL# 700-5010A -- IV.C.3

Discusses the ISS utilities and Screen/Disk subroutines, KFAM-5, the SORT-4 Disk Sort subsystem, and ISS start-up software. This version of ISS is supported for systems with 2200VP/LVP/MVP/SVP Central Processors.

ISS Release 5 Reference Card, WL# 700-5560 -- IV.C.3

This folding pocket card summarizes the ISS Release 5 information.

IDEAS (Inquiry Data Entry Access System) User Manual, WL# 700-5778A -- IV.C.3

Designed for users with some programming experience. This manual includes an overview of IDEAS, describes system initialization procedures, and explains each of the IDEAS utilities—the Data File utility, the Application Initialization Program Generation utility, the Menu Program utility, the Screen Mask utility, the Data Entry/Inquiry/Update Program Generation utility, and the Report/Form Printing utilities.

IDEAS Familiarization Guide, WL# 700-5939 -- IV.C.3

As a supplement to the IDEAS User Manual, this guide is designed to allow anyone to easily demonstrate the power of the system, and to help new users become familiar with the operation of the utilities.

NOTES

SECTION 3 BOOTSTRAP OPERATION

3.1 BOOTSTRAP

A Bootstrap, by definition, is "that part of a computer program used to establish another version of the computer program."

In general, the 2200SVP Bootstrap, is a set of microcoded routines loaded in three 1024×8 -bit Intel 2708 PROM's. The purpose of the Bootstrap is to handle four system functions and make available certain subroutines which are used for I/O operations.

The four system functions handled by the Bootstrap are:

- 1) Master initialization (power-on).
- 2) Reset (initiated by depressing the RESET key on the keyboard).
- 3) Control and Data Memory parity error detection.
- 4) Loading the desired system software (i.e., stand-alone diagnostics, or BASIC-2) from disk and initiating execution.

An explanation of each of the above functions follows.

3.1.1 MASTER INITIALIZATION

Master initialization begins by setting the CPU power switch to the ON position. A branch to Control Memory address 8003 (HEX), located in the Bootstrap PROM's, is executed and the Bootstrap routine begins controlling and performing its various tasks.

The master initialization routine in the Bootstrap performs the following tasks:

- a) Exercises the CPU to determine if any obvious malfunctions exist.
- b) Verifies that the Bootstrap PROM's still maintain the desired data.
- c) Writes zeros to all locations in Data Memory in preparation for subsequent Data Memory read operations.

If all master initialization tasks are completed satisfactorily, the following prompt is displayed at the system console.

MOUNT SYSTEM PLATTER PRESS RESET

3.1.2 RESET

Reset is initiated by depressing the RESET key on the terminal keyboard. This action causes the execution of a branch to Control Memory address 8001 (HEX), located in the Bootstrap PROM's.

Depressing the RESET key is required when one of the following actions is desired:

- a) Pass control, from the present point of program execution, to the currently loaded system program, located in Control Memory (Bootstrap, Microcode diagnostics, or BASIC-2).
- b) Allow the user to recover from any of the various system error conditions which may be encountered.
- c) Abort a Bootstrap load.

Should task a) be called for, the user may expect those messages and/or actions designed into the particular system program. Activation of RESET would typically result in the occurrence of a display menu of user-selectable software options (select Special Function key), or, for instance, an automatic return to some predetermined starting point in the software currently resident in Data Memory.

Generally speaking, whenever task b) is to be performed, the user is expected to inform the Bootstrap of what action to take (by depressing a Special Function key, for instance).

3.1.3 CONTROL AND DATA MEMORY PARITY ERRORS

In both Data and Control Memory a bit has been set aside, called the parity bit, to aid in error detection.

In Control Memory, bit 24 is set aside for parity; it should be turned "on" by the programmer whenever an even number of the remaining 23 bits are turned "on". (This is called ODD Parity.) This bit must be properly set when the microprogram is written.

In Data Memory, a ninth bit is set aside for parity; it is turned "on" by the hardware whenever an even number of the 8 data bits are turned "on". (This is also ODD parity.) The hardware determines and sets this bit, whenever data is written into Data Memory.

Whenever the system detects bad parity in Control Memory, during an instruction fetch, a branch is made to location 8000 (HEX), located in the Bootstrap PROM's. The Bootstrap then displays the appropriate error message at the system console.

Similarly, whenever the system detects bad parity in Data Memory, during a read from Data Memory, a branch is made to location 8002 (HEX), located in the Bootstrap PROM's. The Bootstrap then displays the appropriate error message at the system console.

3.1.4 LOADING SYSTEM FILES

Whenever the operator responds to the Bootstrap request for a system file to be loaded, the following tasks are performed by the Bootstrap.

- a) Check for disk "ready".
- b) Verify whether the user-requested file exists on the mounted platter.
- c) Determine whether the requested file should be loaded into Control Memory and/or Data Memory, and then load the file.

- d) Verify Control Memory, checking instruction parity and built-in CRC and LRC checksums.
- e) Check Data Memory parity.
- f) Pass control to the newly loaded system file.

3.2 BOOTSTRAP ERROR MESSAGES AND RECOVERY

Three types of errors and five possible error messages can be reported by the Bootstrap. The three error types--initalization, reset, and system--are discussed below.

3.2.1 INITIALIZATION ERRORS

If an initialization error occurs, the Bootstrap does not display the complete

MOUNT SYSTEM PLATTER PRESS RESET

message upon the CRT.

This error implies that some routine of the SVP Bootstrap has failed. This may be due to either a CPU-related error or an I/O-related error. If an initialization error occurs, refer to Section 12.

In some cases, a device address may need to be corrected and the system powered on again.

The master initialization sequence is described on the following pages.

MASTER INITIALIZATION Step-By-Step Breakdown of Function

CRT DISPLAY	SEQUENCE OF OPERATIONS	POSSIBLE FAILURES
	1. Power On Trap to 8003	1. Hardware Trap, Branch Instruction
	2. Enable CRT, Clear Screen and Display "M"	2. CRT Address, I/O Register, I/O Lines, CIO Instruction
CLEAR SCREEN		
uMu		
	3. Test 24-Bit Parity Trap. Execute IC 800F which has Bad Parity	3. Parity Checking Logic, Hardware Trap, TSP Instruction (IC+1 stored in stack), PC's may not hold IC retrieved from Stack, Compare Instruction
uWOu	N. M. A. O. L Att	ll Cubusukkus Danah
	4. Test Subroutine Branch and Subroutine Return Instructions	4. Subroutine Branch Instruction, Subroutine Return Instruction, Stack
"MOU"	5. Clear CH, CL Parity Bits	5. Write/Read Data Memory
иWOЛИи	6. Check File Registers	6. Register Instruction, Register Chip, Compare Instruction
"MOUNT"	7 Obsels DO Transmenting on	7 DC Chin
	7. Check PC Incrementing on the A-BUS.	A-Bus Increment Hardware, Compare Instruction
"MOUNT S"	8. Test Auxiliary Registers	8. Auxiliary/Stack Chip, PC Chip, Auxiliary Register Instruction, Compare Instruction

MASTER INITIALIZATION Step-By-Step Breakdown of Function (Continued)

CRT DISPLAY	SEQUENCE OF OPERATION	POSSIBLE FAILURES
"MOUNT SY"	9. Test Binary ALU	9. Binary ALU, AC, ACX, AI, SC or SCX Instruction, Compare Instruction
"MOUNT SYS"	10. Test Stack.	10. Auxiliary/Stack Chip, PC Chip, Stack Instruction, Compare Instruction
"MOUNT SYST"	ll. Test Decimal ALU	11. Decimal ALU, DAC, DACI, DACX, DSC, DSCI or DSCX Instruction, Compare Instruction
"MOUNT SYSTE"	12. Test Binary Multiply	12. Multiply Logic, M OR MI Instruction, Compare Instruction
"MOUNT SYSTEM"	13. Test Shift	13. Shift Logic, Compare Instruction
"MOUNT SYSTEM "	14. Verify PROM	14. PROM Chip
"MOUNT SYSTEM P"	15. Zero 8-Bit Data Memory	15. SR Failure, Bad IC's
"MOUNT SYSTEM PLATTER" "PRESS RESET"		
	16. Write/Read Control Memory	16. WCM/RCM Instruction, Stack, Auxiliary Register, PC Chip, SB Instruction, Compare Instruction

3.2.2 RESET ERRORS

If a reset error occurs, the hexdigit display of the selected Special Function key does not appear upon the CRT when the operator has properly responded to the "KEY SF'?" message.

This implies that the Special Function key was not depressed sufficiently, the 2236DE or its controller may be defective, or an SF' key not defined was depressed. If a reset error occurs, refer to Section 12.

NOTE:

During the reset function, several of the SYSTEM ERROR messages may appear. If one does, consult the recovery procedure for that particular message, given in Section 3.2.3.

The system reset sequence is described on the following pages.

SYSTEM RESET Step-By-Step Breakdown of Function

CRT DISPLAY

SEQUENCE OF OPERATIONS

POSSIBLE FAILURES

- 1. Reset keyed while Bootstrap is in control
- 1. Reset Trap

CLEAR SCREEN

"KEY SF'?"

- Inactive SF is keyed,
 I/O Register,
 I/O Lines,
 CRB or KFN,
 Keyboard

NOTE: if any undefined SF' key is despressed, the "KEY SF" message re-appears and step 2 must be repeated.

#"KEY SF'?" (address)

- 3. Enable specified disk
- Improper disk address,
 I/O Register,
 I/O Lines,
 Disk Not Powered On,
 Disk Not Ready
- 4. Search disk for desired file; if file cannot be found, Step 2 is repeated
- 4. Wrong Special Function key depressed, Wrong disk mounted
- 5. Load desired file into Memory
- 5. I/O Register, I/O Lines, Disk Problems

NOTE: System files should contain a comment block containing file date. If a disk error results, the system error message will appear. Consult Error Recovery, for proper procedure. If a parity error occurs during loading, 'P' will be displayed and the previous sector will be reloaded. If no control memory data is found, skip to step 9.

^{*}The name of the file to load and the platter to load from is displayed.

SYSTEM RESET Step-BY-Step Breakdown of Function (continued)

CRT DISPLAY

SEQUENCE OF OPERATIONS

POSSIBLE FAILURES

"KEY SF'?" (address) "COMMENT"

- 6. Verify Control Memory. (Parity, LRC & CRC). If an error results, the system error message will appear. Consult Error Recovery, for proper procedure.
- 6. Memory, WCM/RCM Instruction
- 7. Check 8-Bit Data Memory. If an error results, the system error message will appear. Consult Error Recovery, for proper procedure.
- 7. Memory, Read/Write Instruction
- 8. Control is passed to loaded system file which now takes over control. Consult proper system file documentation. (Address = 3000).
- 9. Display Diagnostic Menu listing upon CRT.

"KEY SF'?"

- 10. Enable Keyboard (address 10. Inactive SF is keyed, = 01) and accept Special function key input. Operator keys the SF key of the desired diagnostic
- I/O Register, I/O Lines. CRB OR KFN, Keyboard

"KEY SF'?" (address)

11. Go to Step 4.

3.2.3 SYSTEM ERRORS

The third grouping of error conditions is reported to the operator via a SYSTEM ERROR message on the CRT.

First, should memory fail, the following message will appear:

*** SYSTEM ERROR MMMM XXXX ***
PRESS RESET

where: MMMM = PECM--Parity Error Control Memory
PEDM--Parity Error Data Memory
VECM--Verify Error Control Memory
VEDM--Verify Error Data Memory

XXXX = Various error information pertinent to the type of error.

Secondly, a disk error will result in the following message being displayed:

*** SYSTEM ERROR DISK OOXX ***
PRESS RESET

where: 00XX = is the Disk Error Code

The procedure used to recover from these system errors is similar. Therefore, the general procedure will be outlined and each error will be discussed.

The general procedure is:

- a) Key RESET in response to the "PRESS RESET" message on line 2 of the CRT.
- b) Choose one of the four following courses of action.
 - 1. Key SF'15 to resume, using the currently loaded system program (usually BASIC-2).

- 2. Key SF'00-'05, '08-'013 to load BASIC-2 from disk 310, B10, 320, B20, 330, B30, 350, B50, 360, B60, 370 or B70.
- 3. Key SF'16-'19 to load the User diagnostic menu from disk 310, BlO, 320, or B20, respectively.
- 4. Key SF'28-'31 to load the Field Service diagnostic menu from 310, B10, 320, or B20, respectively.

Use special caution when you choose #1 above: depending on what type of error and where it occured, BASIC-2 may not function properly in all cases.

The following discussion outlines each of the system errors and what may be done, in particular, to recover from them. (Also refer to Section 12 if a system error occurs.)

3.2.3.1 CONTROL MEMORY ERRORS

In both Data Memory and Control Memory, one bit has been set aside for parity error detection.

In Control Memory, the 24th bit (bit #23) of every microinstruction is set aside for parity (it is turned "on" whenever an even number of the remaining 23 bits are turned "on"). This is called ODD Parity. This bit must be properly set when writing the instruction into Control Memory.

*** SYSTEM ERROR (PECM aaaa dddddd) ***

The address of the instruction with bad parity. Where: aaaa =

> The instruction located at aaaa. The instruction is dddddd = reread when displayed and thus may not be the same as

when the error occurred.

This error implies that bad parity was detected while the system was trying to execute an instruction from Control or Bootstrap Memory.

Whenever the system detects bad parity in Control Memory (PECM message) during an instruction fetch, a branch is made to Control Memory address 8000 (HEX), located in the Bootstrap PROM's. The Bootstrap then performs its designated error routine and displays PECM aaaa, dddddd.

Bad parity may be the result of:

- a) Dropping of bits by Control/Bootstrap Memory.
- b) Picking up of bits by Control/Bootstrap Memory.
- c) Writing bad parity to Control Memory.
- d) Defective parity-checking logic.

This error should be serious enough to warrant the executing of a Control Memory diagnostic. However, it may be possible to resume execution of the currently loaded system program. If the error is reported again, a Control Memory diagnostic should be run to locate the defective memory chip.

*** SYSTEM ERROR VECM aaaa ***

Where: aaaa = An address in the section of Control Memory that does not verify correctly.

Case 1 (aaaa = 0000 thru 7FFF)

This error implies that the load of Control Memory from the disk was not successful. However, bad memory locations cannot be entirely ruled out.

This error is reported prior to a system program being given control and is the result of the program not being loaded properly into Control Memory.

The operator should attempt to reload that particular system program. However, should successive failures be reported, a Control Memory diagnostic should be run to determine if there are any bad memory chips. If no chips are reported defective, a CPU instruction may be failing, requiring a CPU diagnostic to be run.

Case 2 (aaaa = 8000 thru 83FF)

This error implies that the Bootstrap Memory is not as expected.

This error may be caused from dropping or picking up bits by one or more of the three PROM's that make up the Bootstrap.

Try to power on again, and if the problem still persists replace the Bootstrap PROM's and master initialization the CPU. If the error continues, the board containing the Bootstrap PROM's may have failed, or, in some cases, a microinstruction may have failed.

3.2.3.2 DATA MEMORY ERRORS

In Data Memory, a ninth bit allocated for each 8-bit byte is used in the same manner as described above. However, the CPU hardware determines the required state and sets this bit whenever a write is executed in Data Memory.

*** SYSTEM ERROR (PEDM ss.aaaa)***

Where: ss = Memory bank containing the error (00 = bank #1)

aaaa = Data memory address (i.e., the current value of the
PC's) at the time of the error. This is probably, but
not necessarily, the address of the memory location
with bad parity.

This error implies that bad parity was detected during a read of Data Memory.

Whenever the system detects bad parity in Data Memory (PEDM message) during a read from Data Memory, a branch is made to Control Memory address 8002 (HEX), located in the Bootstrap PROM's. The Bootstrap then performs another error routine and displays PEDM ss.aaaa.

Bad parity may be the result of:

- a) Dropping of bits in Data Memory.
- b) Picking up of bits in Data Memory.
- c) Defective parity checking logic.

This error should be serious enough to warrant the executing of a Data Memory diagnostic. However, it may be possible to resume execution of the currently loaded system program. If the error is reported again, a Data Memory diagnostic should be run to locate the defective memory chip.

*** SYSTEM ERROR (VEDM ss.aaaa)***

Where: ss = Memory bank containing the error (00 = bank #1)

aaaa = Address of the data in error

This error implies that the area of data memory used for system constants (verb tables, match constants, messages), was not loaded properly when BASIC-2 was loaded. However, bad memory locations cannot be entirely ruled out.

This error is reported prior to a system program being given control. The operator should attempt to reload BASIC-2. However, should successive failures be reported, Data Memory diagnostics should be run to determine if there are any defective memory chips.

3.2.3.3 DISK ERRORS

*** SYSTEM ERROR DISK OOXX ***

There are several possible disk errors that may occur while the Bootstrap is trying to load a particular system program. The possible disk errors, with causes and recovery procedures, are as follows.

DISK 0082

Error: File not in catalog

Cause: The file to be loaded does not reside on the platter specified.

DISK 0088

Error: Wrong record

Cause: The format of the record read, during a load operation, does not

conform to the Bootstrap format.

DISK 0090

Error: Disk Hardware Error

Cause: The disk did not recognize or properly respond to the system at

the beginning of a read or write operation. The read or write

has not been performed.

DISK 0091

Error: Disk Hardware Error

Cause: The disk is not in a ready state.

DISK 0092

Error: Disk Hardware Error

Cause: The disk did not respond to the system at the beginning of a

read or write operation in the proper amount of time (time-out). The read or write has not been performed.

DISK 0093

Error: Disk Format Error

Cause: A format error was detected during a read or write. The problem

can be either the disk platter or the hardware.

DISK 0095

Error: Seek Error

Cause: The specified sector could not be found.

DISK 0096

Error: Cyclic Read Error

Cause: A cyclic redundancy check error occurred during a read operation.

DISK 0097

Error: Longitudinal Read Error

Cause: A longitudinal redundancy check error occurred when reading a

sector.

DISK 0098

Error: Disk Addressing Error

Cause: The disk sector being addressed is not valid.

SECTION 4

OPERATION AND PROGRAMMING CONSIDERATIONS

4.1 POWER-ON

To begin, switch ac power ON in the terminal and the Central Processor.

After power is applied to the system, the prompt appears:

MOUNT SYSTEM PLATTER PRESS RESET

The system disk contains the BASIC-2 Operating System, as well as a variety of hardware diagnostics. Steps may now be taken to load the Operating System or hardware diagnostics via Special Function Keys on the terminal.

Mount the system disk, then press the RESET key (located in the upper-left corner of the keyboard). The following prompt is displayed:

KEY SF'?

4.2 LOADING THE OPERATING SYSTEM

A Special Function Key must be depressed to specify the address of the disk drive in which the system disk is loaded. The following options are available:

Key SF '00 to load BASIC-2 from the disk € address 310 (Hex).

Key SF '01 to load BASIC-2 from the disk @ address B10 (Hex).

Key SF '02 to load BASIC-2 from the disk @ address 320 (Hex).

Key SF '03 to load BASIC-2 from the disk ${\it e}$ address B20 (Hex).

Key SF '04 to load BASIC-2 from the disk @ address 330 (Hex).

Key SF '05 to load BASIC-2 from the disk @ address B30 (Hex).

Key SF '08 to load BASIC-2 from the disk @ address 350 (Hex).

Key SF '09 to load BASIC-2 from the disk @ address B50 (Hex).

Key SF '10 to load BASIC-2 from the disk @ address 360 (Hex).

Key SF '11 to load BASIC-2 from the disk @ address B60 (Hex).

Key SF '12 to load BASIC-2 from the disk € address 370 (Hex).

Key SF '13 to load BASIC-2 from the disk @ address B70 (Hex).

NOTE:

Normally, as viewed from the front of the unit, the drive (Winchester or diskette) mounted in the left side of the unit is assigned address 310 (HEX), and is referred to as the "Fixed" drive. The diskette drive mounted in the right side of the unit is assigned address B10 (HEX), and is referred to as the "Removable" drive. If the 2200SVP contains only one diskette drive and no Winchester drive, the DSDD drive is mounted on the right side of the unit, is assigned address 310 (HEX), and is referred to as the "Fixed" drive.

Approximately 15 seconds are required for the BASIC-2 Operating System to be loaded into Control Memory. While this takes place, the following message will appear on the display screen of the terminal:

Loading: 2200SVP BASIC-2 Release X.X

When loading is complete, the system displays the "READY (BASIC-2)" message.

If the wrong SF Key is depressed (i.e., if the system disk is mounted at address 310, but the operator depresses SF Key 02), an error message will be displayed:

*** SYSTEM ERROR (DISK OOXX) ***
PRESS RESET

Recovery from such errors may be accomplished by simply pressing RESET, followed by the correct Special Function key. If RESET fails, turn the Central Processor OFF then ON again. If this latter step is required, Master Initialization will be repeated.

In some instances, the Special Function key code is displayed. This may indicate that an incorrect disk address was specified, or that a disk controller has failed. Check the controller address, or replace the controller if that board is suspected to be defective.

4.3 COPYING THE SYSTEM DISK

Disk/Diskette Drives System

- 1. Be certain that the write-protect notch on the Operating System diskette is uncovered (write-disabled) and insert the diskette into the DSDD drive.
- 2. If the Winchester drive has not been formatted, do so by keying:

SELECT DISK B10 (RETURN) -- selects diskette drive

LOAD RUN "@FORMAT" (RETURN) -- loads and runs format utility program

from the Operating System diskette

- 3. Answer all screen prompts to format the Winchester drive at address 310 (HEX). (Formatting takes approximately 13 minutes.)
- 4. When formatting has been completed, enter the following to create a backup copy of the system diskette on the Winchester disk.

COPY RF (RETURN) or MOVE RF (RETURN)

- 5. Remove the Operating System diskette from the DSDD drive and insert a blank diskette in its place. (Ensure that the write-protect notch on the new diskette is covered (write-enabled).
- 6. If the blank diskette has not been formatted, do so by keying:

RUN (RETURN) -- runs the format utility that is already loaded in CPU memory

- 7. Answer all screen prompts to format the diskette at address B10 (HEX). (Formatting takes approximately 2.0 minutes.)
- 8. When formatting has been completed, enter the following to create a backup copy of the Operating System on diskette.

COPY FR (RETURN) or MOVE FR (RETURN)

Dual Diskette Drives System

- 1. Be certain that the write-protect notch on the Operating System diskette is uncovered (write-disabled) and insert the diskette into the Removable DSDD drive (on the right side of the unit).
- 2. Insert a blank diskette into the Fixed DSDD drive (on the left side of the unit). Be certain the diskette is write-enabled (notch covered).
- 3. If the blank diskette has not been formatted, do so by keying:

SELECT DISK B10 (RETURN) -- selects Removable DSDD drive

LOAD RUN "@FORMAT" (RETURN) -- loads and runs format utility program

from the Operating System diskette

- 4. Answer all screen prompts to format the Fixed DSDD drive at address 310 (HEX).
- 5. When formatting has been completed, enter the following to create a backup copy of the system diskette.

COPY RF (RETURN) or MOVE RF (RETURN)

4.4 PROGRAMMING CONSIDERATIONS

For detailed information concerning 2200SVP programming considerations, refer to Wang BASIC-2 Language Reference Manual, WL# 700-4080 (IV.C.2).

SECTION 5 HARDWARE THEORY OF OPERATION

5.1 CENTRAL PROCESSING UNIT

Refer to Section 5 of Model 2200LVP Maintenance Manual (IV.A.3 M) for an explanation of how the Central Processor operates. The SVP CPU boards are identical to those in the 2200LVP.

5.2 DISK/DISKETTE PROCESSING UNIT

Refer to Section 5 of Model 2200LVP Maintenance Manual (IV.A.3 M) for information concerning the operation of the 3-board Disk/Diskette Processing Unit (DPU). The LVP and SVP utilize the same DPU.

5.3 DUAL DISKETTE PROCESSING UNIT (ref: FIGURE 5-1 and 7890 schematic)

The Dual Diskette Processing Unit (DPU) is a Z80A based microcomputer responsible for controlling all diskette drive activities (reading, writing, and R/W head positioning), and for supervising data transfer between the 2200SVP CPU and the diskette drives. The major components of the one logic board (WL# 210-7890-A) that comprises the DPU are:

- -- A Z80A Central Processor IC: controls all DPU operations.
- -- 4K x 8-bit EPROM (Erasable Programmable Read Only Memory)--two 2716 IC's: contains the microprogram that controls the DPU.
- -- 2K x 8-bit static RAM (Random Access Memory)--four 4-bit 2114 IC's: stores the data to be transferred between the 2200SVP and the diskette, as well as quantities, values, and status required by the microprogram to perform its task.
- -- An Am9517 DMA (Direct Memory Access) IC: handles all DMA operations between the 2200SVP, DPU, and diskette drive.

-- A uPD765 diskette controller IC (FDC): monitors and initiates all diskette drive activities.

5.3.1 Z80A INPUT/OUTPUT PORT ADDRESSES

Following is a list of the DPU Z80A I/O Port assignments with the HEX address that selects each Port.

PORT DESCRIPTION	HEX ADDRESS
Read FDC Main Status Register	00
Write FDC Main Status Register	01
Read FDC Result Registers	01
Issue Terminal Count to FDC	10
DMA Read/Write Port Channel 0	20
DMA Read/Write Port Channel 1	22
DMA Read/Write Port Channel 2	24
DMA Read/Write Port Channel 3	26
DMA Status Port	28
Transfer Mode Address	2B
Reset 2200 Reset F/F	30
Read Controller Status	40
Unload Head of Drive 1	50
Load Head of Drive 1	51
Set Controller Busy	60
Set Controller Ready	61
Unload Head of Drive 2	70
Load Head of Drive 2	71
Reset FDC	90
Select Conversation Mode	AO
Select DMA Mode	A1
Select Drive 1	B 0
Deselect Drive 1	B 1
Single-Byte Output to 2200	CO
Select Drive 2	DO
Deselect Drive 2	D1
Single-Byte Input from 2200	EO
Enable NMI to Z80A	FO
Disable NMI to Z80A	F1

5.3.2 2200SVP CPU/DPU COMMUNICATION

The DPU transmits/receives data to/from the CPU in one of two modes—Conversation Mode or DMA Mode. In Conversation Mode, the Z80A routes a byte of data between memory or its own registers and the CPU; in DMA Mode the Am9517 routes a byte of data between memory and the CPU.

The 2200SVP CPU initiates all communication between itself and the DPU by placing the desired disk address on the Address Bus $(\overline{AB1}-8)$ and generating an Address Bus Strobe $(\overline{ABS}$ low, CABS high). $\overline{AB1}-8$ are applied to the DPU Address Comparator along with the outputs from the DPU Device Address Switch. If the desired disk address and the setting of the Device Address Switch are identical, the comparator applies an "equal" signal (active low) to the input of the DPU Select F/F. The low going edge of the Address Bus Strobe (CABS) clocks the "equal" signal through the Select F/F as $\overline{\text{SELECT}}$. This signal, when active, indicates the DPU is selected and allows communication between the CPU and the DPU by enabling buffers for the Input Bus Strobe $(\overline{\text{IBS}})$, the Output Bus Strobe $(\overline{\text{OBS}})$, the Output Bus Central Processor Busy $(\overline{\text{CPB}})$ signal.

5.3.2.1 CPU-TO-DPU

Once the DPU is selected, the 2200SVP CPU does not attempt to communicate with the DPU until the DPU is "ready". When all internal housekeeping has been completed by the DPU, the microprogram sets the DPU "ready" ($\overline{\text{ZIORQ}}$ low to Port 61 sets $\overline{\text{BUSY}}$ low and $\overline{\text{BAO}}$ low, which toggles the Ready/Busy F/F setting CRDY/ $\overline{\text{B}}$ high and $\overline{\text{R}/\text{B}}$ low). The CPU monitors the DPU ready/busy status ($\overline{\text{R}/\text{B}}$), and when the DPU is "ready", the CPU initiates a "reinitialize" sequence as follows.

The CPU sets $\overline{AB6}$ and $\overline{AB8}$ active (i.e., low) and generates an Output Bus Strobe (\overline{OBS} low, \overline{COBS} low), indicating the start of the "reinitialize" sequence. When all three of these signals are active, the DPU produces a Reinitialize signal (\overline{REIN} low). \overline{REIN} clears the CONV/DMA F/F (\overline{CONV} /DMA low), indicating the DPU is in Conversation Mode (CONV), and is also applied to the Z80A Interrupt input (\overline{INT}). When the Z80A receives the Interrupt (\overline{INT} low) the microprogram sets the DPU "busy" (\overline{ZIORQ} low to Port 60 sets \overline{BUSY} low and \overline{BAO} high, which toggles the Ready/Busy F/F setting CRDY/ \overline{B} low and \overline{R} /B high). The microprogram then checks the tri-state Status Buffer (\overline{ZIORQ} low to Port 40 sets \overline{STATUS} low). Upon detecting that the DPU is in Conversation Mode (D0 high, \overline{CONV} /DMA low), the microprogram enters a routine that sets the DPU "ready" and waits, by monitoring the Status Buffer, for the CPU to become "ready".

When the DPU finds that the CPU is "ready" (D1 high, CCPB low, CPB high), the microprogram sets the DPU "busy", sends a HEX D0 data byte to the CPU (indicating the DPU has been initialized and communication may continue), and then sets the DPU "ready" again. (Section 5.3.2.2 explains exactly how the DPU transmits this data byte to the CPU.)

After the DPU has been initialized, the CPU proceeds to send three bytes of address information to the DPU. These address bytes specify the required disk command (read, write, write compare), the diskette to be used (fixed or removable), and the address of the sector where the command is to be performed. The DPU echoes each address byte back to the CPU, where it is checked against the byte that was sent to ensure transmission integrity. (Again, Section 5.3.2.2 details how these data bytes are sent to the CPU.)

Each byte of address information is received on the Output Bus (OB1-8) and passes through the Output Bus Buffer, which was enabled when the DPU was selected (SELECT low). The data is then strobed into the tri-state Output Bus Latch by a 700 nsec one-shot pulse (active high) that is triggered by the Output Bus Strobe (COBS low). Next, the Output Bus Latch generates an Interrupt signal ($\overline{4INT}$ low) which is combined with \overline{CONV} /DMA and applied to the Status Buffer. When the microprogram detects this Interrupt request along with the selection of Conversation Mode (D2 high, CONV/DMA low, INT low), the program sets the DPU "busy" and enters a routine to service the Output Bus Latch. This servicing is accomplished by the Z80A issuing an Input Request $(\overline{ZIORQ} \text{ low to Port EO sets } \overline{ZIN} \text{ low)}$ and a Read signal $(\overline{ZRD} \text{ low})$. The Input Request signal is multiplexed through the Z80A/DMA I/O Multiplexer by the Read signal and applied to the Select 1 input $(\overline{S1} \text{ low})$ of the Output Bus Latch. With the Select 1 input low, the Output Bus Latch dumps the data byte onto the Data Bus (DO-7) for input to the Z80A, and clears the Interrupt request (4INT high). The Z80A accepts the data byte, examines it, and stores it in memory. This entire procedure is repeated for the remaining address bytes. After the DPU has received all three bytes of address information, the microprogram causes the DPU to enter the DMA Mode of data transmission (ZIORQ low to Port AO sets CONV/DMA high).

Once the DPU is in DMA Mode, the CPU sends 256 bytes of data. As was the case with the three address bytes, the data passes through the Output Bus Buffer and into the Output Bus Latch. In DMA Mode, the DPU is set "busy" every time the Output Bus Latch issues an Interrupt request (4INT low) and returns to the "ready" state after the latch has been serviced and the Interrupt request cleared. When in DMA Mode, the Am9517 services the Output Bus Latch in the following manner.

The Output Bus Latch Interrupt request (4INT low) and the selection of DMA Mode (CONV/DMA high) produce a Channel 1 Data Request signal (DREQ1 high), which is sent to the Am9517. Upon detecting the Data Request, the Am9517 issues a Hold Request ($\overline{\text{HREQ}}$ low) to the Z80A. No longer than one machine cycle later, the Z80A responds to the request with a Bus Acknowledge reply (ZBUSACK low). This signal informs the Am9517 that it now has control of the Address Bus, the Data Bus, and the control lines. During the S1 state of the Am9517, the Am9517 outputs the eight high order address bits (for the memory location where the data is to be transferred) to the DMA High Order Address Latch via the Data Bus. This information is strobed into the High Order Address Latch on the trailing edge of the Am9517 produced Address Strobe (ADSTB active high). The Am9517 also sends an Address Enable signal (AEN low) to the Address Latch enabling the outputs of the latch to be applied to the high order lines of the Address Bus (A8-15). The eight low order address bits (for the memory location where the data is to be transferred) are output by the Am9517 directly (A0-7). The Memory Selection circuit decodes A10-12 and enables the appropriate RAM's. (RAM addresses are HEX 1000-1800.) The Address Strobe produced by the Am9517 gates the Memory Selection circuit to ensure that RAM is not enabled until the high order address bits are latched. (The RAM outputs and the High Order Address Latch inputs are both connected to the Data Bus.)

Next, the Am9517 generates a Data Acknowledge signal ($\overline{DACK1}$ low) and a Read signal (\overline{ZRD} low). \overline{ZRD} gates $\overline{DACK1}$ through the Z80A/DMA I/O Multiplexer forcing the Select line ($\overline{S1}$) of the Output Bus Latch low. With the Select line low, the Output Bus Latch dumps its data byte onto the Data Bus and clears the Interrupt request ($\overline{4INT}$ high). The Am9517 activates the Memory Write line (\overline{MEMWR} low) which results in the data byte being written into RAM at the specified location.

The Output Bus Latch Select line (S1) returns to the inactive state at the completion of the memory write operation. This entire sequence continues for all 256 bytes of data, and the Am9517 then generates an End of Process signal (EOP low) which in turn issues a Non-Maskable Interrupt (NMI low) to the Z80A. The Z80A detects the Interrupt and jumps to microprogram address HEX 0066, where a routine determines which component generated the Interrupt (Am9517 or uPD765). The Z80A then returns to the appropriate location in the microprogram. This event completes the data transfer operation.

Two other signals produced by the CPU convey information to the DPU: Prime--CPRMS (PRMS buffered), and Control Bus Strobe--CCBS (CBS buffered). The RESET key on the terminal generates Prime (CPRMS low), and the CPU software generates a Control Bus Strobe (CCBS high). These combined signals produce a 2200 Reset pulse (22RST low). This signal issues an Interrupt request to the Z80A and presets the RESET F/F. The output of the Reset F/F is tied to D3 of the Status Buffer. When the Z80A receives the Interrupt, the microprogram checks the Status Buffer. Detecting the requested Reset (D3 high), the program initializes the DPU.

5.3.2.2 DPU-TO-CPU

NOTE:

The following discussion will be easier to comprehend if the preceding section (CPU-to-DPU communication) is read and understood first. For DPU-TO-CPU communications, the methods by which the DPU is selected and initialized, as well as the method of address byte reception are the same as for CPU-to-DPU communication.

When the DPU is in Conversation Mode, the Z80A routes data to the CPU in the following manner.

When the CPU is "ready", the Z80A applies the byte of data to be transferred to the Data Bus (D0-7), issues an Output Request ($\overline{Z10RQ}$ low to Port CO sets $\overline{Z0UT}$ low), and generates a Write signal (\overline{ZWR} low). \overline{ZWR} gates $\overline{Z0UT}$ through the Z80A/DMA I/O Multiplexer, forcing the Send line of the Output Data Buffer active (high). The Send line gates the byte of information on the Data Bus through the Output Data Buffer (OD0-7) and to the Input Bus Buffer.

At the same time, the Send signal produces an Input Bus Strobe (IBS low), which is sent to the CPU. \overline{IBS} also enables the Input Bus Buffer to allow the data to pass through and be received by the CPU. After the data has been accepted by the CPU, the CPU sets "busy" (\overline{CPB} low, CCPB high), which in turn drives the DPU Transfer line inactive (XFER low). This clears the Input Bus Strobe F/F (\overline{IBS} high), thus completing the data transmission.

When the DPU is in DMA Mode, the Am9517 routes data to the CPU in the following manner.

When the CPU indicates it is "ready" to receive the 256 bytes of data, the Am9517 Channel 2 Data Request line is activated (CPB high sets XFER high). Once the Data Request is detected, the Am9517 issues a Hold Request (HREQ low) to the Z80A. After the Am9517 has acquired control of the bus lines from the Z80A (ZBUSACK low), the Am9517 dumps a byte of data onto the Data Bus and generates a Channel 2 Data Acknowledge signal (DACK2 low) and a Write signal (ZWR low). ZWR gates DACK2 through the Z80A/DMA I/O multiplexer, producing a Send signal. Send gates the data through the Output Data Buffer to the Input Bus Buffer. The data is then strobed to the CPU by the Input Bus Strobe. After the data has been accepted by the CPU, the CPU sets "Busy" (CPB low, CCPB high), which in turn drives the DPU Transfer line inactive (XFER low). This event clears the Input Bus Strobe F/F (IBS high) thus completing transmission of the data byte. When the CPU sets "Ready" again, the entire sequence of events is repeated, until all 256 bytes have been sent to the CPU. At the end of the DMA transfer, the Am9517 generates an End of Process signal (EOP low) which in turn issues a Non-Maskable Interrupt (NMI low) to the Z80A. The Z80A detects the Interrupt and jumps to microprogram address HEX 0066, where a routine determines which component generated the Interrupt (Am9517 or uPD765). The Z80A then returns to the appropriate location in the microprogram. This event completes the data transmission operation.

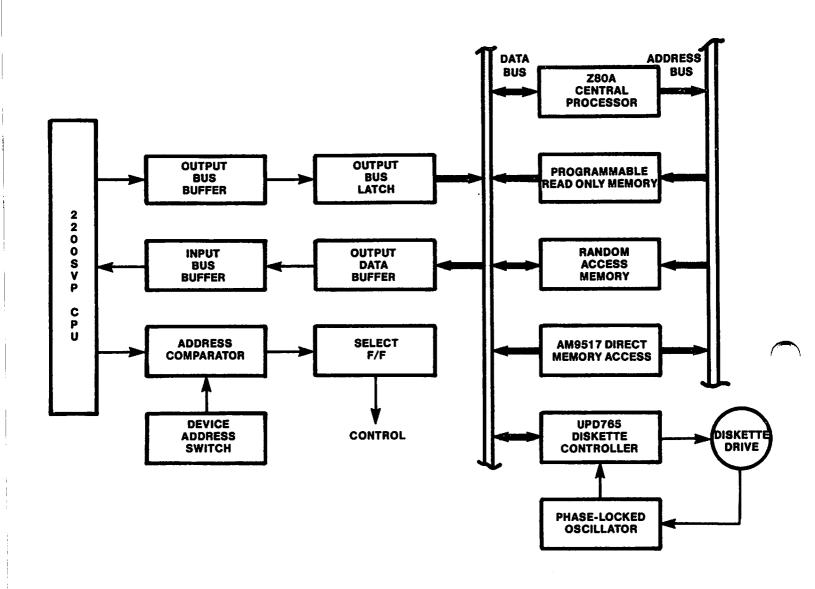


FIGURE 5-1 DUAL-DISKETTE PROCESSING UNIT BLOCK DIAGRAM

NOTES

SECTION 6 SITE PREPARATION

For information concerning preinstallation site planning and preparations, refer to the corporate "Customer Site Planning Guide" WL# 700-5978, its updates, and CE documentation category I.A.7.

SECTION 7 UNPACKING AND RECEIVING INSPECTION

7.1 TOOLS REQUIRED

Xacto knife (WL# 726-9493)

7.2 PRE-UNPACKING INSPECTION

Before unpacking the 2200SVP, check the packing slip to ensure that the proper equipment has been delivered. After checking the packing slip, visually inspect the container carefully for any indications of possible shipping damage (crushed edges or corners, puncture holes, tears, etc.). If any shipping damage is noted, file an appropriate claim promptly with the carrier involved and notify the WLI Distribution Center (Department 90), Quality Assurance Department, of the nature and extent of that damage, making arrangements for equipment replacement, as necessary.

7.3 UNPACKING INSTRUCTIONS

- 1. Using an Xacto knife, cut the tape securing the shipping carton cover.
- 2. Open the box and remove the instapack covering the top of the unit. (Four styrofoam corner molding pieces may be used instead of instapack.)
- 3. With the aid of another person, remove the unit from the carton.
- 4. Save the shipping carton and protective padding for use when reshipping the unit.

NOTES

SECTION 8 INSTALLATION

Following is a list of documentation categories referenced by this section. Documentation from these categories is required to ensure correct installation of a 2200SVP system.

Setting Device Address Switches -- IV.B.1
TC Controllers -- IV.B.2
I/O Cable Connector Installation -- I.B.0
2236DE Interactive Terminal -- III.D.1
DSDD Diskette Drive (SA850) -- III.A.11
Winchester Disk Drive (SA1002) -- III.A.12
Peripherals -- Appropriate categories

8.1 PRE-INSTALLATION INSPECTION

- 1. Be certain that the customer site has been prepared according to the guidelines referenced in Section 6, and then place the SVP unit in its assigned physical location.
- 2. Remove the top cover from the unit (ref: Section 11).
- 3. Inspect the SVP chassis assembly for damaged or loosened asemblies. Also check for loose hardware or debris. If any shipping damage is noted, notify the WLI Distribution Center (Department 90), Quality Assurance Department, of the nature and extent of the damage, making arrangements for equipment replacement, as necessary.
- 4. Ensure that the unit is thoroughly clean. Use a soft bristle brush and a vacuum cleaner to remove dust from the inside of the unit. Use a mild detergent and a soft cloth or sponge to remove dirt and grime from the cabinet. Do not use abrasive or corrosive materials.

8.2 INITIAL SETUP

This section consists of:

- -- photographs (Figures 8-1 through 8-6) in which the major components of the 2200SVP are pointed out--to familiarize the Customer Engineer with the physical aspects of the SVP.
- -- photographs of the circuit boards (CPU and DPU) showing PROM numbers and locations, switch settings, and component loading for the various versions of the same board (memory).
- -- an explanation (with photographs) of the units internal cable connections.
- -- references to the appropriate documentation categories that deal with equipment associated with (normally included with) the SVP system.

Section 8.3 (Installation and Power-On Procedures) helps link together the various information items contained in this section.

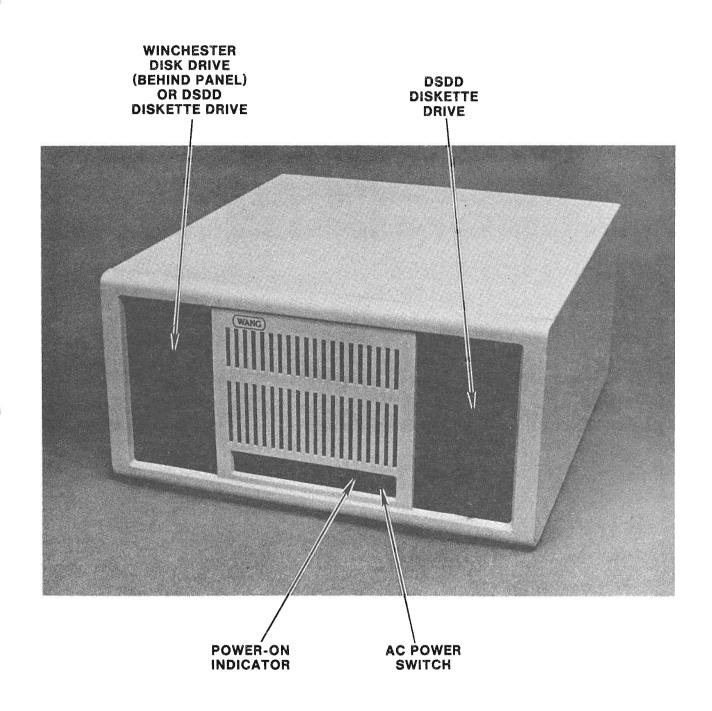


FIGURE 8-1 2200SVP (FRONT VIEW)

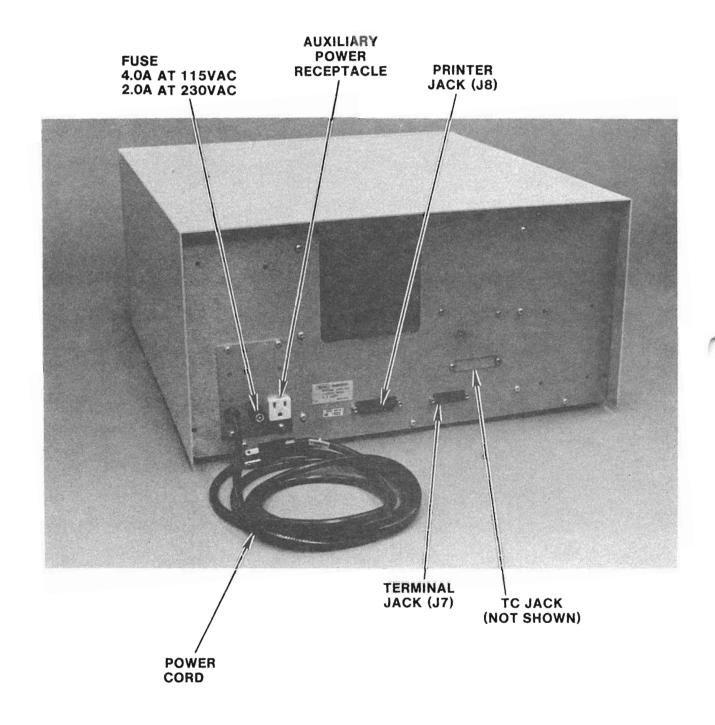


FIGURE 8-2 2200SVP (REAR VIEW)

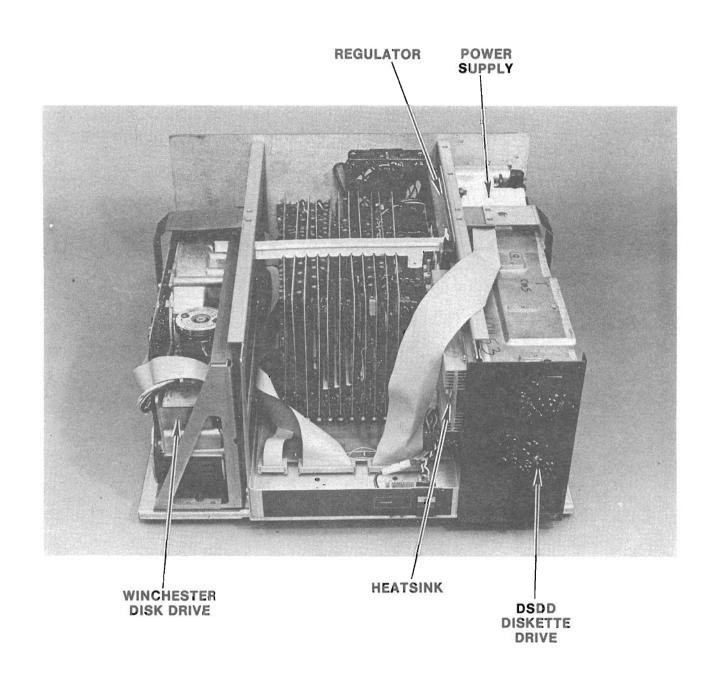


FIGURE 8-3 2200SVP WITH 3-BOARD DPU (INTERNAL FRONT VIEW)

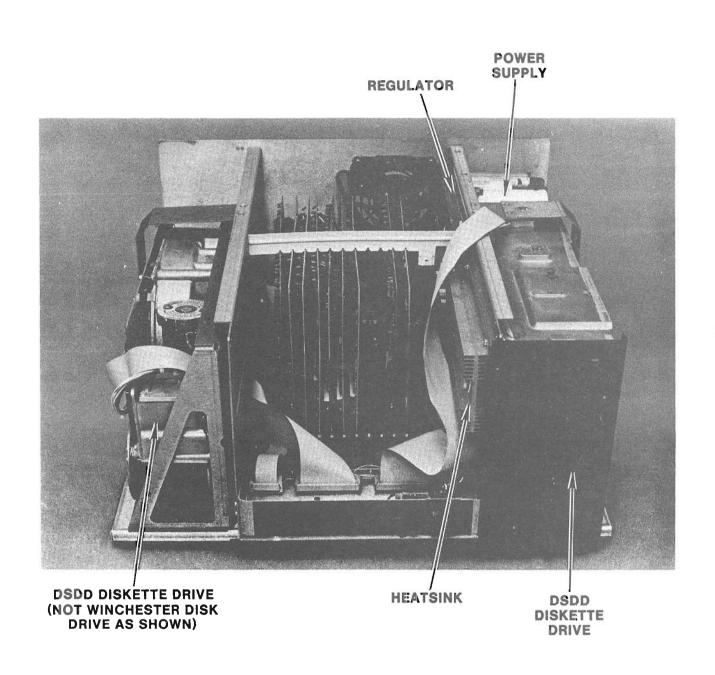


FIGURE 8-4 2200SVP WITH 1-BOARD DPU (INTERNAL FRONT VIEW)

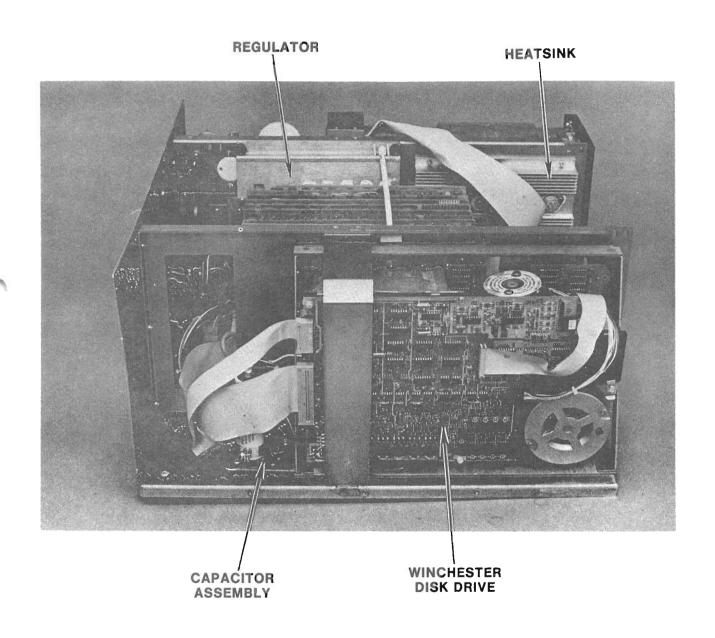


FIGURE 8-5 2200SVP (INTERNAL LEFT VIEW)

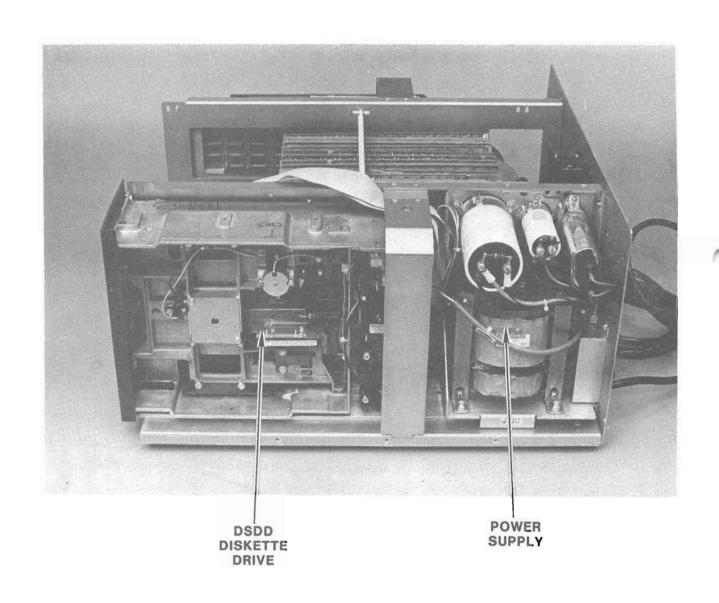


FIGURE 8-6 2200SVP (INTERNAL RIGHT VIEW)

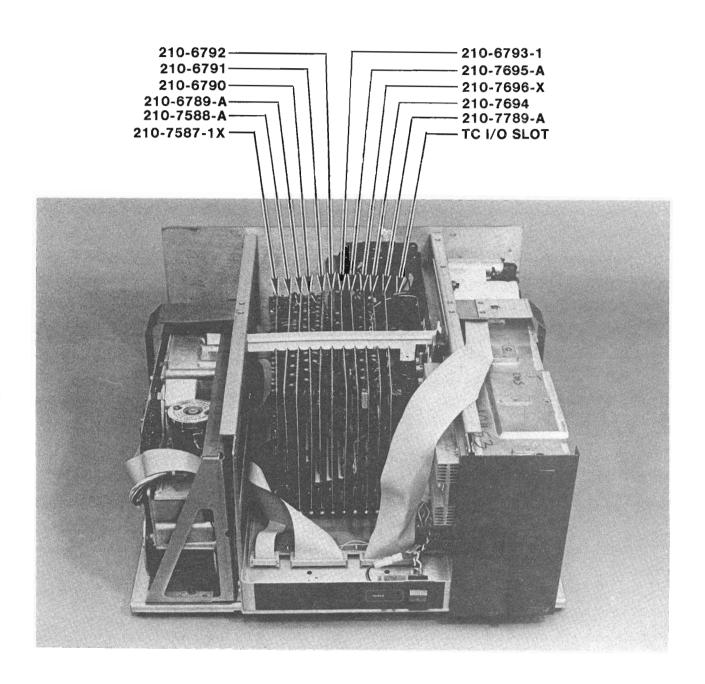


FIGURE 8-7 CIRCUIT BOARD LOADING (3-BOARD DPU)

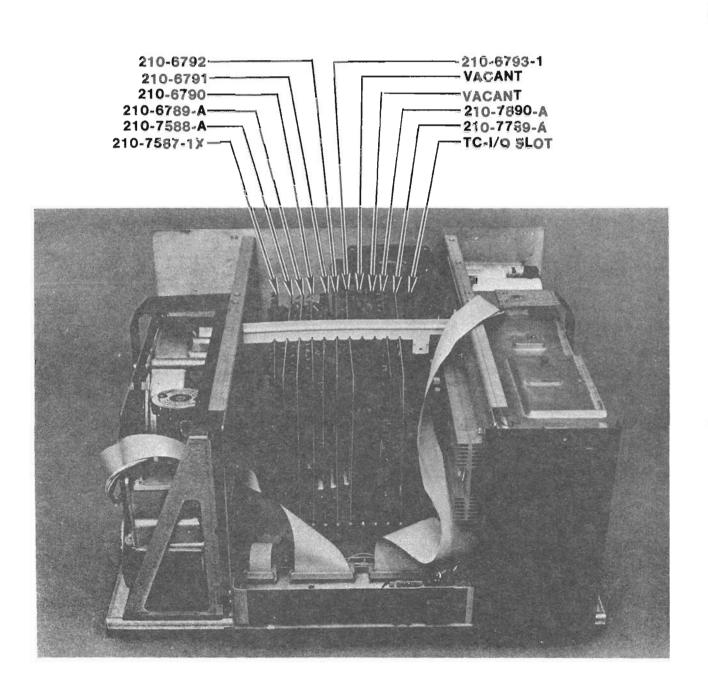


FIGURE 8-7A CIRCUIT BOARD LOADING (1-BOARD DPU)

Refer to Section 8.2.1 of Model 2200LVP Maintenance Manual, IV.A.3 M, for photos and information concerning the following logic boards.

WL#	DESCRIPTION
210-6789-A	Memory Control (CPU)
210-6790	Instruction Counter (CPU)
210-6791	Stack (CPU)
210-6792	ALU (CPU)
210-6793-1	Registers (CPU)
210-7587-1B	Data Memory32K (CPU)
210-7587-1A	Data Memory64K (CPU)
210-7695-A	Disk Controller (DPU, 3-board)

The WL# 210-7588-A Control Memory board--16K--(CPU) is the same as the WL# 210-7588-1A board--32K--used in the 2200LVP (ref: Section 8.2.1 of Model 2200LVP Maintenance Manual, IV.A.3 M) except that only the bottom two rows of RAM's are loaded.

The WL# 210-7694 2200/Disk Interface board (3-board DPU), and the WL# 210-7696-A, -B, -C Microcomputer/Memory board (3-board DPU) are the same as those used in the 2200LVP; however, the following two figures along with the PROM loading and switch setting explanations should be used as references.

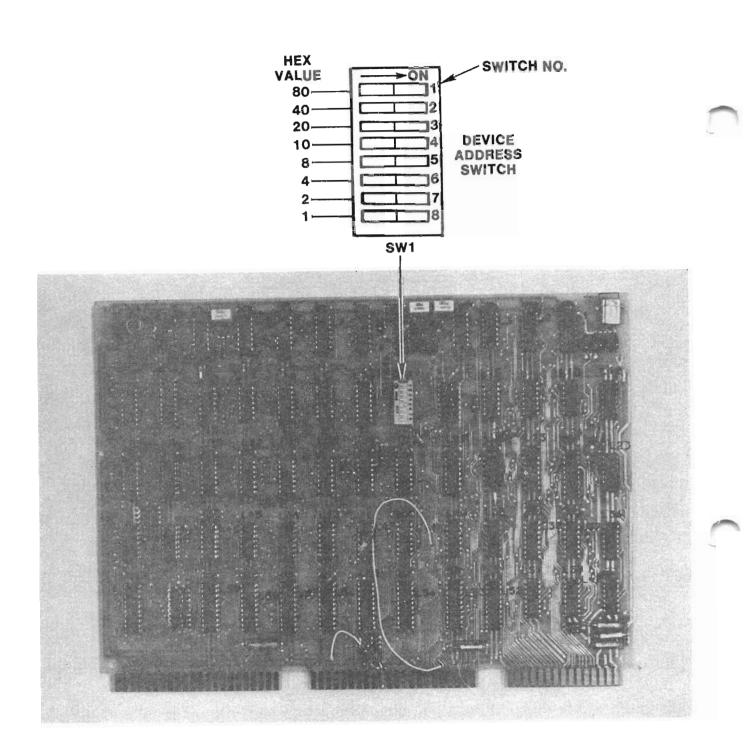
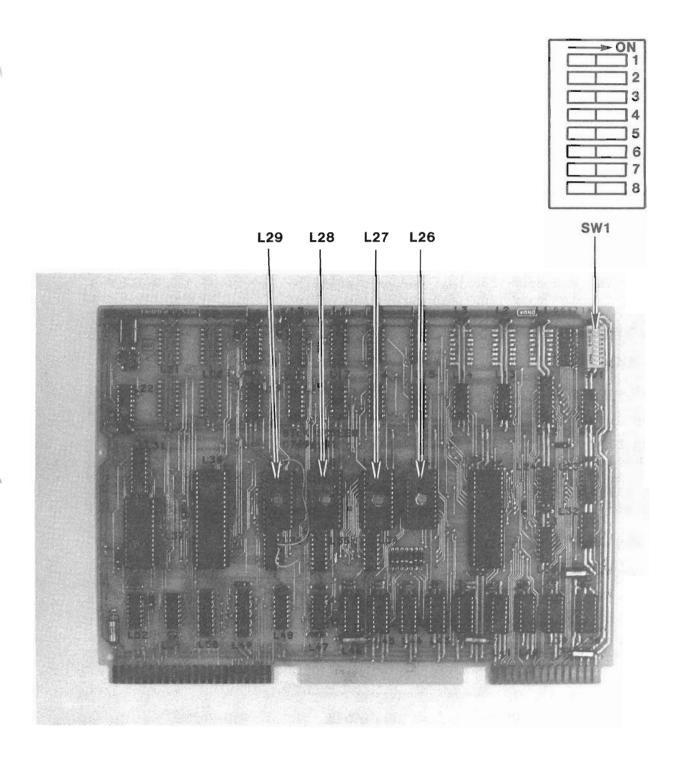


FIGURE 8-8 WL NO. 210-7694 2200/DISK INTERFACE (DPU)



NOTE: SEE FOLLOWING TEXT FOR PROM LOADING AND SWITCH SETTING EXPLANATION

FIGURE 8-9 WL NO. 210-7696-X MICROCOMPUTER/MEMORY (DPU)

NOTE:

The following PROM loading and switch setting explanation includes information concerning an 8 MB Winchester Disk Drive; however, this version of the drive is not sold with the SVP system.

WL# 210-7696-X Microcomputer/Memory--Switch Settings

NOTE: 1 = ON and 0 = OFF.

WL# 210-7696-A (4 or 8 MB Winchester Disk Drive):

CONFIGURATION	1					£S 6		8
Diskette drive only (for test purposes only)	-		_			-		1
4 MB Winchester only (for test purposes only)	1	1	0	0	1	1	1	1
8 MB Winchester only (for test purposes only)	1	0	0	1	1	1	1	1
4 MB Winchester and diskette drive	-		-	-	•	-		1
8 MB Winchester and diskette drive	1	0	0	1	1	0	1	1

WL# 210-7696-B (2 or 8 MB Winchester Disk Drive):

			T				_	
CONFIGURATION		2	3	4	5	6	7	<u>8</u>
Diskette drive only (for test purposes only)	1	1	0	1	1	0	1	1
2 MB Winchester only (for test purposes only)	1	1	0	0	1	1	1	1
8 MB Winchester only (for test purposes only)	1	0	0	1	1	1	1	1
2 MB Winchester and diskette drive	1	1	0	0	1	0	1	1
8 MB Winchester and diskette drive	1	0	0	1	1	0	1	1

WL# 210-7696-C (Dual Diskette Drives):

CONFIGURATION			3 3			ES 6	7	8
Removable diskette drive only (for test purposes only) Fixed diskette drive only			-	-		_	-	1
Fixed and removable diskette drives	1	0	0	0	1	0	1	1

WL# 210-7696-X Microcomputer/Memory--PROM Loading

	210-7696-A (4 OR 8 MB WINCHESTER)	210-7696-B (2 OR 8 MB WINCHESTER)	210-7696-C (DUAL DSDD DISKETTE)
L29	378-4220	378-4220	378-4231
L28	378-4221	378-4221	378-4232
L27	378-4222	378-4222	378-4233
L26	378-4223	378-4230	378-4234

NOTE: 1. TERMINAL BAUD RATE IS HARDWIRED TO 19.2K.

2. TERMINAL ADDRESS IS HARDWIRED TO HEX 00-07.

3. PRINTER ADDRESS IS HARDWIRED TO HEX 215.

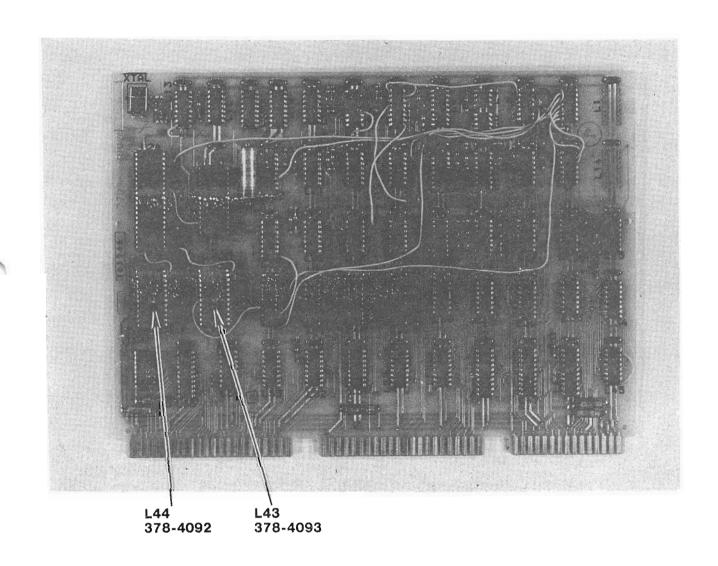
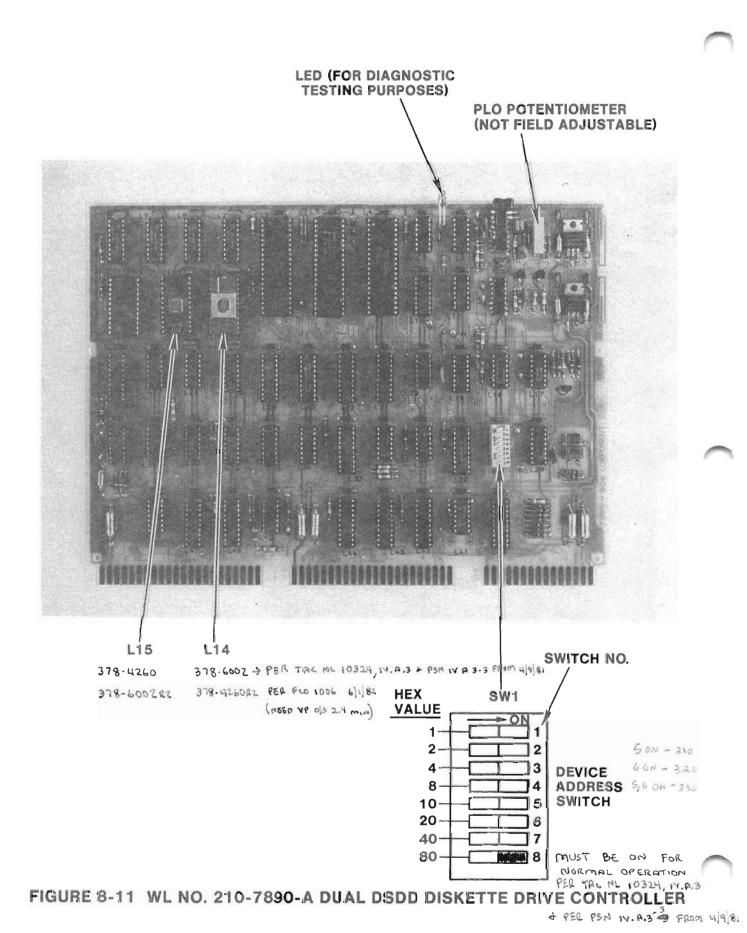


FIGURE 8-10 WL NO. 210-7789-A TERMINAL/PRINTER CONTROLLER



8-16

8.2.2 2200SVP CABLE CONNECTIONS

A 50-pin ribbon cable (WL# 220-3134) connects CPU motherboard connector 1 (ref: FIGURE 8-12) to jack J1 on the DSDD Diskette Drive (ref: FIGURE 8-13).

A 50-pin ribbon cable (WL# 220-3134) connects CPU motherboard connector 2 (ref: FIGURE 8-12) to jack J1 on the Winchester Disk Drive (ref: FIGURE 8-14).

A 20-pin ribbon cable (WL# 220-3133) connects CPU motherboard connector 3 (ref: FIGURE 8-12) to jack J2 on the Winchester Disk Drive (ref: FIGURE 8-14).

One disk drive ac power cord (WL# 220-0260) attached to the terminal block on the rear panel of the SVP connects to jack J4 on the DSDD Diskette Drive (ref: FIGURE 8-13); the second ac power cord (WL# 220-0259) connects to jack J4 on the Winchester Disk Drive (ref: FIGURE 8-15).

A 3-connector disk drive dc power harness (WL# 220-1473) connects jack J4 on the CPU motherboard (ref: FIGURE 8-16) to jack J5 on the DSDD Diskette Drive (ref: FIGURE 8-13) and to the capacitor assembly harness (ref: FIGURE 8-15). The capacitor assembly harness, in turn, attaches to jack J5 on the Winchester Disk Drive (ref: FIGURE 8-15).

A ribbon cable (ref: FIGURE 8-17) is used to connect the internal portion of the TC jack in the rear panel of the SVP (ref: FIGURE 8-2) to the TC jack on the TC Controller that is (may be) installed in the SVP's I/O slot. (The cable from the modem connects to the external portion of the TC jack.)

8.2.3 2200SVP POWER SUPPLY AC INPUT VOLTAGE SELECTION

There are two models of the 2200SVP power supply--one for 50 hertz applications and one for 60 hertz applications. The ac input voltage for both power supplies is switch selectable. The location of the 115/230 input voltage selection switch is shown in FIGURE 8-18). Be certain that the switch is positioned correctly for the supplied ac voltage.

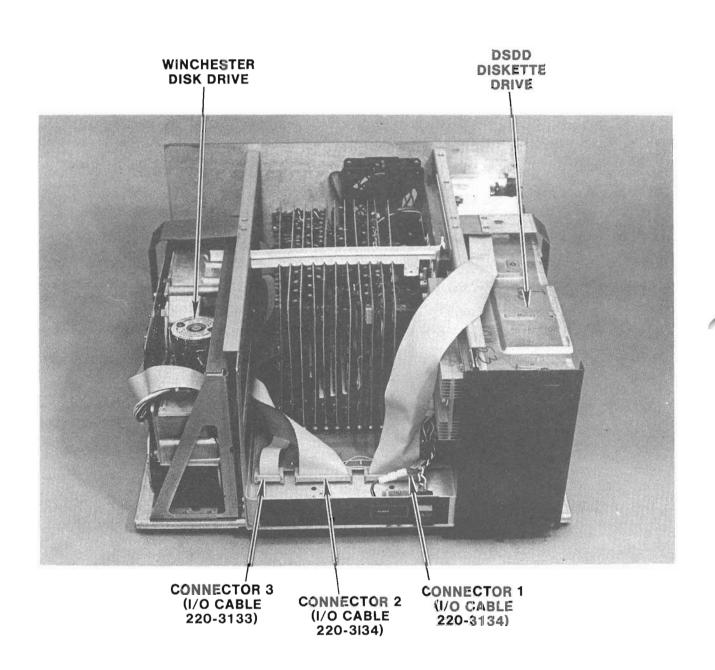


FIGURE 8-12 DISK/DISKETTE DRIVE I/O CABLE CONNECTIONS

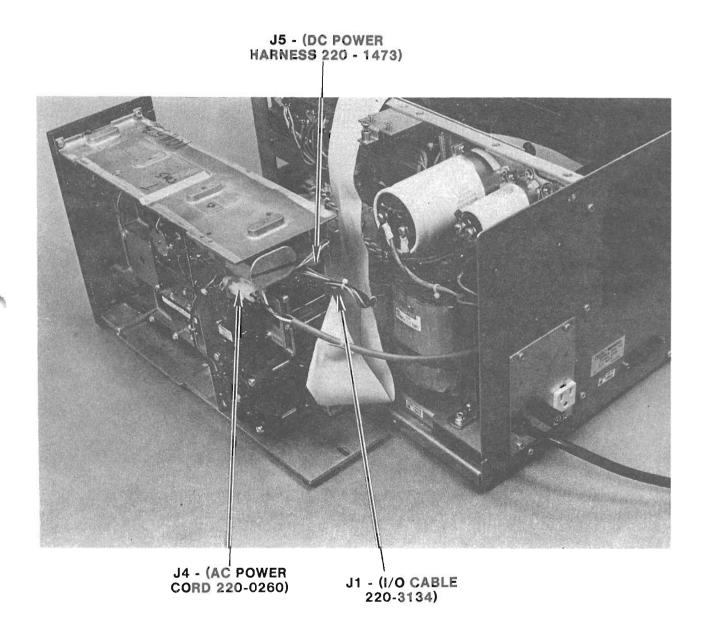
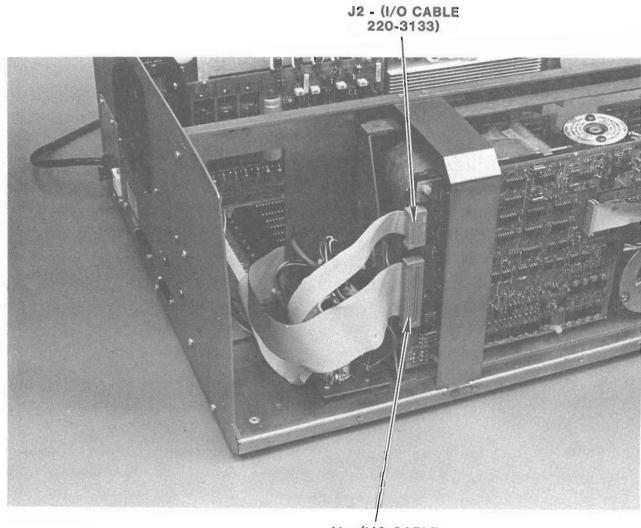


FIGURE 8-13 DSDD DISKETTE DRIVE CABLE CONNECTIONS



J1 - (I/O CABLE 220-3134)

FIGURE 8-14 WINCHESTER DISK DRIVE I/O CABLE CONNECTIONS

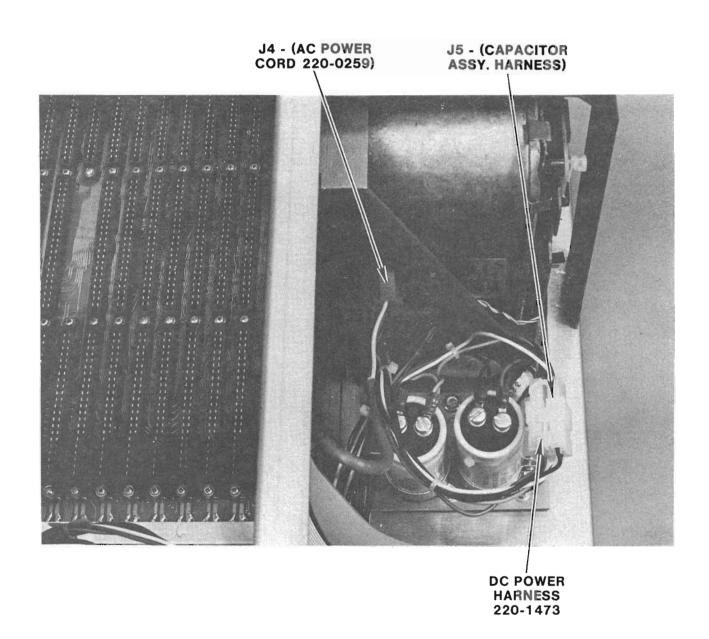


FIGURE 8-15 WINCHESTER DISK DRIVE POWER CABLE CONNECTIONS

J4 (DC POWER HARNESS 220-1473)

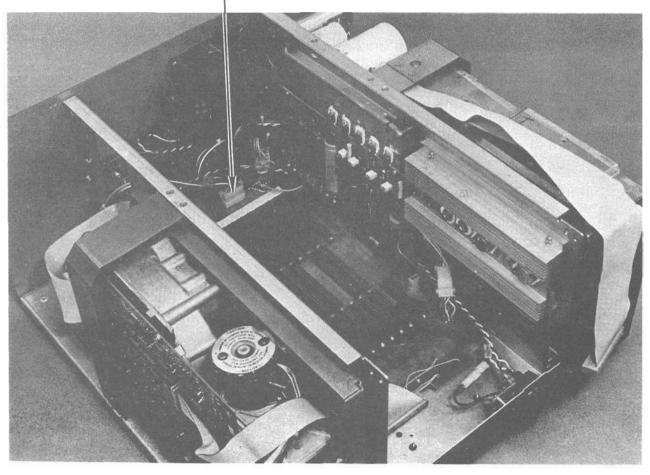
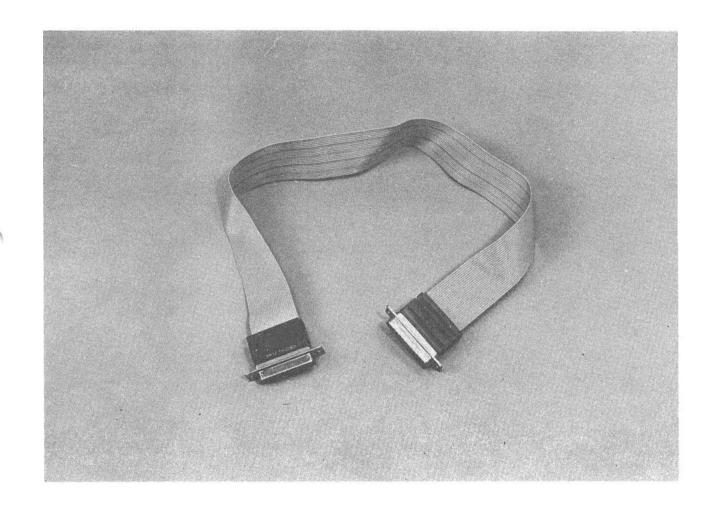


FIGURE 8-16 DISK/DISKETTE DRIVES DC POWER HARNESS CONNECTION



220-3109

FIGURE 8-17 TELECOMMUNICATIONS JUMPER CABLE

8-23

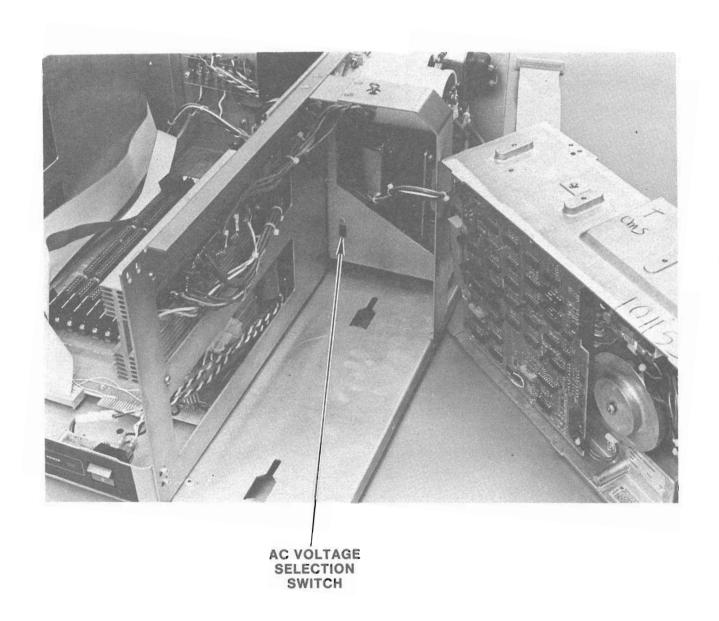


FIGURE 8-18 AC VOLTAGE SELECTION SWITCH

8.2.4 TELECOMMUNICATIONS CONTROLLERS

Refer to documentation category IV.B.2 for information concerning TC Controllers.

8.2.5 DISK DRIVES

Refer to documentation categories III.A.11 and III.A.12 for information concerning initial setup, adjustments, off-line diagnostic tests, etc.

8.2.6 2236DE INTERACTIVE TERMINAL

Refer to documentation category III.D.1 for information concerning unpacking, initial setup, adjustments, off-line diagnostic tests, system interconnection etc.

8.2.7 PERIPHERALS

Refer to the appropriate documentation category for information concerning unpacking, initial setup, adjustments, off-line diagnostic tests, system interconnection etc.

8.3 INSTALLATION AND POWER-ON PROCEDURES

- 1. Ensure that the CPU power supply ac input voltage selection switch is positioned correctly for the supplied ac voltage (ref: Section 8.2.3).
- 2. Check to see that all circuit boards are properly seated in their appropriate locations, and that all switches are set correctly (ref: Section 8.2.1--Figures 8-7 through 8-11).
- 3. Check to see that all cables are firmly attached to the appropriate connectors (ref: Section 8.2.2).
- 4. Remove the shipping diskette from the DSDD Diskette Drive(s). Save the diskette(s) for use when reshipping the drive(s)/unit.

- 5. If the unit contains a Winchester Disk Drive, remove the shipping clamp that secures the ac spindle motor. (This clamp is located on the side of the drive opposite the circuit board.) Save this clamp for use when reshipping the drive/unit.
- 6. Remove the spring clip that prevents the Winchester Disk Drive head actuator damper from rotating. The spring clip fastens the tab on the actuator damper to the track 00 photocell. The damper can be readily indentified by the yellow CAUTION label attached to it. Save the clip for use when reshipping the drive/unit.
- 7. Be certain that the CPU ac power switch is OFF, and then plug the CPU ac power cord in.
- 8. Set the CPU ac power switch ON, then check and adjust, if necessary, all CPU power supply voltages (ref: Section 11).
- 9. Set the CPU ac power switch OFF.
- 10. Attach the system terminal and peripherals to the appropriate jacks in the rear panel of the SVP (ref: Section 8.2). (Unlike other 2200 systems, all peripherals connect to the rear panel of the SVP.)

NOTE:

If peripheral I/O cables are routed through conduit, ceilings, walls, or floors, it will be necessary to install connectors on the ends of those cables. The procedure for connector installation is documented in category I.B.O.

- 11. Set the terminal ac power switch ON; set the CPU ac power switch ON; set the ac power switches of all peripherals ON.
- 12. At this point, the terminal should have the "MOUNT SYSTEM PLATTER--PRESS RESET" prompt displayed (ref: Section 4). If this message is not displayed, set the CPU ac power switch OFF. After 2 or 3 seconds, set the switch back ON. If the message is still not displayed, refer to Sections 3 and 12.

- 13. After the power-on prompt is displayed, insert the 2200SVP Operating System diskette (WL# 704-0001) into the DSDD Diskette Drive, and then press RESET on the keyboard of the terminal.
- 14. The prompt "KEY SF'?" should now be displayed (ref: Section 4). If this message is not displayed, refer to Sections 3 and 12.
- 15. After the "KEY SF'?" prompt is displayed, load and run the SVP User and Field Service diagnostics (ref: Section 9). If the system will not load the diagnostic programs, refer to Sections 3 and 12. If any diagnostic errors occur, refer to Section 12.
- 16. After successful completion of all Microcode diagnostics, load BASIC-2 (ref: Section 3).
- 17. After BASIC-2 has been loaded, load and run the BASIC-2 Language diagnostics (ref: Section 9).
- 18. Upon completion of the BASIC-2 diagnostics, load and run the appropriate peripheral diagnostics (ref: Section 9).
- 19. After all peripherals are proven to be operational, format the Winchester Disk Drive by loading and running the format utility program "@FORMAT" (resident on the Operating System diskette).
- 20. When formatting has been completed, load and run the disk diagnostics (ref: Section 9) to test the Winchester Drive.
- 21. Check all DSDD Diskette Drive adjustments/alignments to ensure that they are correct (ref: Section 11.5 and documentation category III.A.11).
- 22. The system is now ready for customer use.

SECTION 9 DIAGNOSTICS

Following is a list of documentation categories referenced by this section. Diagnostic information in these categories is required to fully test a 2200SVP system.

2200SVP CPU/DPU, disk drives, and peripherals -- IV.C.1 2236DE Terminal -- III.D.1

CPU Diagnostics

There are three classes of diagnostic tests available for the 2200SVP CPU:

1) "Bootstrap" diagnostics (resident in the 2200SVP firmware), 2) Microcode diagnostics (contained on the 2200SVP Operating System diskette), and 3)

BASIC-2 Language diagnostics (available on diskette). Refer to Section 3 of this manual for an explanation of the Bootstrap diagnostics. Refer to documentation category IV.C.1 for information concerning the Microcode and BASIC-2 Language diagnostics.

DPU Diagnostics

The Disk Processing Unit has a built-in power-on diagnostic. If a failure is detected, the activity LED in the door latch release button of the DSDD Diskette Drive will blink on and off. As of February, 1981, the diagnostic program and the DPU boards are not finalized. Refer to documentation categories IV.C.1 and IV.A.3 for later developments on this system element.

Terminal Diagnostics

Refer to documentation category III.D.1 for information concerning 2236DE Terminal power-on diagnostics.

Disk Diagnostics

Refer to documentation category IV.C.1 for information concerning Disk diagnostics.

Peripheral Diagnostics

Refer to documentation category IV.C.1 for information concerning Peripheral diagnostics.

SECTION 10

PREVENTIVE MAINTENANCE

To ensure trouble-free operation, the 2200LVP/SVP must have periodic preventive maintenance, consisting of inspection, cleaning, and adjustments. The following preventive maintenance routines should be performed once every six to twelve months. This preventive maintenance schedule assumes a clean operating environment and a normal operating time during the standard five-day, 40-hour weeks. A dusty environment or any substantial increase in system operating time will require that the preventive maintenance be scheduled at closer intervals. In addition, these preventive maintenance routines should be performed during each unscheduled service call.

- 1. Set the CPU ac power switch OFF.
- 2. Check the unit cooling fan for proper operation.
- 3. Use a soft-bristle brush and a vacuum cleaner (WL #726-9518) to remove dust from the inside of the CPU.

- 4. Ensure that the 2200SVP is kept up-to-date by verifying and installing all required ECN's (ref: Mandatory Update Bulletin, CE #03-0085--I.B.O).
- 5. Set the CPU ac power switch ON.
- 6. Check and adjust, if necessary, the CPU power supply voltages according to the procedure given in Section 11.2.

CAUTION:

Before making any adjustments, be certain that the measuring instruments are properly calibrated, and then test the item. Adjustments, particularly electrical adjustments, should be performed only when the parameter measured proves to be out of tolerance. Do not make electrical or mechanical adjustments indiscriminately.

- 7. Perform all preventive maintenance measures for the DSDD Diskette Drive (ref: documentation category III.A.11).
- 8. Run the SVP diagnostics referenced in Section 9, as needed, to confirm proper operation of the CPU circuitry.
 - 9. Use a mild detergent and a soft cloth or sponge to remove dirt and grime from the CPU cabinetry. Do not use abrasive or corrosive chemicals.

NOTES

NOTES

SECTION 11

REMOVAL/REPLACEMENT AND ADJUSTMENT PROCEDURES

11.1 RECOMMENDED TEST EQUIPMENT/TOOL LIST

 Digital Voltmeter (WL# 726-9595), with an accuracy of at least + 1% of full scale and 1 mv resolution factor. Analog Multimeters have accuracy and resolution factors that are unacceptable for certain critical measurements.

Acceptable Type/Equivalent: FLUKE #8000A

2. Multimeter, 20,000 ohms/volt (minimum); 2% or better full scale accuracy; for less critical measurements.

Acceptable Type/Equivalent: TRIPLETT VOM #630NA

- 3. Oscilloscope, with two Xl probes and two XlO probes. Acceptable Type/Equivalent: TEKTRONIX #465
- 4. Heavy duty screwdriver with well-insulated handle (WL# 726-9411).
- 5. Small screwdriver with insulated shank (WL# 726-9406).
- 6. 5/16" nut driver (WL# 726-9473).
- 7. Nut driver handle (WL# 726-9478).

11.2 CPU VOLTAGE ADJUSTMENT PROCEDURE

Note that when increasing RAM capacity or adding an additional disk drive, all voltages must be rechecked and readjusted when necessary.

If the voltage level of +5V, +12V, or -5V drops .3V (+4.7V, +11.7V, or -4.7V), +24V is shut off, and the unit remains in an initialized state.

- 1. Set the CPU ac power switch OFF.
- 2. Remove the top cover of the unit (ref: Section 11).
- 3. Set the CPU ac power switch ON.
- 4. Check the dc voltages with a digital voltmeter for the values listed in TABLE 11-1. (The test points for monitoring the voltages are shown in FIGURE 11-1.) Adjust the trimpots where indicated in FIGURE 11-2 to obtain correct voltage levels where necessary.

IMPORTANT:

Be sure to connect the COMMON lead of the voltmeter to a $\pm 0V$ connection, NOT the chassis or I/O controller rail. Erroneous readings will result if chassis ground is used as the voltmeter reference. The oscilloscope ground clip should also be attached to $\pm 0V$, NOT chassis ground.

5. Using an oscilloscope, with the vertical sensitivity set at 1V/cm, and a X1 probe, measure the ripple at the points indicated in FIGURE 11-1. Ac ripple should not exceed the limits specified. If any voltage or ripple measurement is out of specification, troubleshoot the CPU power supply.

TABLE 11-1 DC VOLTAGE SPECIFICATIONS

	LIMIT	'S
VOLTAGE	VOLTAGE	RIPPLE
+5	+4.75 to +5.25	100 mv p-p
+12	+11.70 to +12.40	100 mv p-p
+24	+21.60 to +26.40	100 mv p-p
- 5	-4.75 to -5.25	100 mv p-p
- 12 *	-11.50 to -12.50	100 mv p-p

⁻¹²V is not adjustable.

11.3 DISK/DISKETTE PROCESSING UNIT PLO ADJUSTMENT

Adjustment of the phase-locked oscillator in the 3-board DPU should be performed only by board-repair personnel. For this reason, the potentiometers are glyptolled after the PLO has been adjusted in Manufacturing. If the PLO is suspected of being out of adjustment, simply change the WL# 210-7694 board.

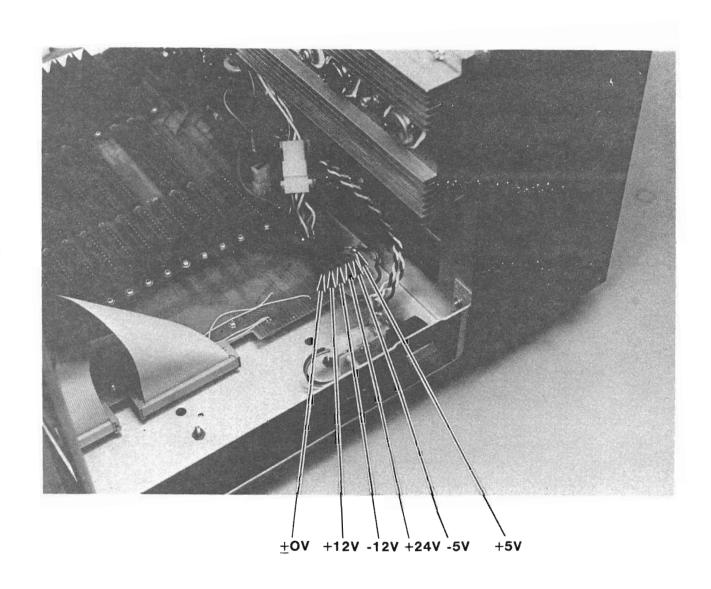


FIGURE 11-1 DC VOLTAGE TEST POINTS

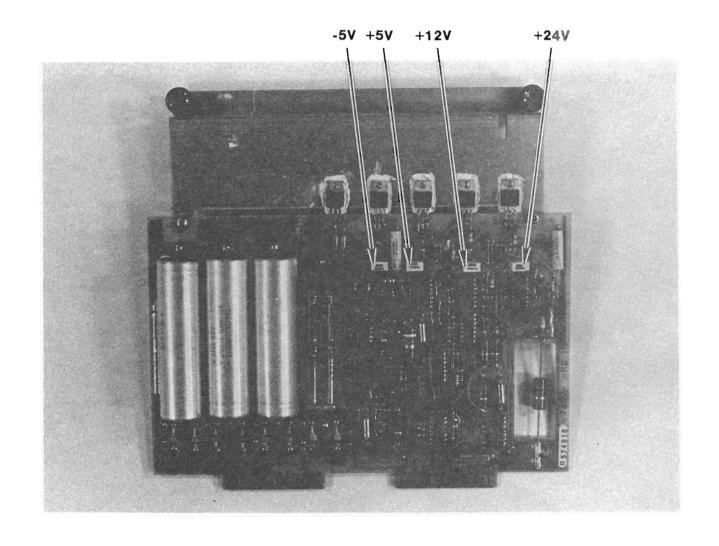


FIGURE 11-2 WL NO. 210-7887 REGULATOR DC VOLTAGE POTS

11.4 DUAL DISKETTE PROCESSING UNIT PLO ADJUSTMENT

Adjustment of the phase-locked oscillator in the single-board DPU should be performed only by board-repair personnel. For this reason, the potentiometer is glyptolled after the PLO has been adjusted in Manufacturing. If the PLO is suspected of being out of adjustment, simply change the WL# 210-7890-A board.

11.5 DSDD DISKETTE DRIVE ADJUSTMENTS/ALIGNMENT

Refer to documentation category III.A.11 for information concerning the adjustment and alignment procedures for the DSDD Diskette Drive.

An alignment PROM (WL# 378-4252) is available to allow the Customer Engineer to perform any required adjustments on a diskette drive whenever BASIC-2 cannot be loaded. Documentation explaining how to use the alignment PROM is also available and should be received with the PROM when the PROM is ordered.

11.6 REMOVAL/REPLACEMENT PROCEDURES

11.6.1 TOP COVER

- 1. Using a phillips screwdriver, remove the six screws securing the sides of the cover (three on each side of unit) and the two screws securing the cover to the rear of the chassis (ref: FIGURE 11-3).
- 2. Slide the cover toward the front of the unit, and then lift the cover off.

11.6.2 CIRCUIT BOARD RETAINER

1. Squeze the two clips that fasten the retainer to the regulator board (ref: FIGURE 11-4), and lift the retainer out of the slot in the regulator board.

2. Slide the left side of the retainer down and out of the slot in the chassis frame while lifting up on the right side of the retainer.

11.6.3 DISKETTE DRIVE

- 1. Insert the cardboard shipping diskette into the drive.
- 2. Disconnect the ac power cord from the drive (ref: FIGURE 8-13).
- 3. Using a slot screwdriver, remove the screw that secures the fastening bracket to the top of the drive (ref: FIGURE 11-5).
- 4. Slide the drive toward the front of the unit to disengage the mounting blocks that are located on the bottom of the drive from the slots in the chassis.
- 5. Lift the drive out of the unit and remove the dc power cable and the I/O cable (ref: FIGURE 8-13). (The length of the dc power cable limits the distance that the drive can be moved.)

11.6.4 WINCHESTER DRIVE

- 1. Disconnect the the ac power cord (ref: FIGURE 8-15) and the I/O cable (ref: FIGURE 8-14) from the drive.
- 2. Using a 5/16" nut driver, remove the hex bolt that secures the rear of the drive and the capacitor assembly to the chassis (ref: FIGURE 11-4).
- 3. Slide the drive toward the front of the unit to disengage the mounting blocks that are located on the bottom of the drive from the slots in the chassis.
- 4. Disconnect the dc power cable from the drive (ref: FIGURE 8-15).
- 5. Lift the drive out of the unit.

11.6.5 HEATSINK ASSEMBLY

- 1. Remove the Diskette Drive (ref: Section 11.6.3).
- 2. Disconnect all heatsink harness cables (ref: FIGURE 11-5).
- 3. Using a phillips screwdriver, remove the four screws securing the heatsink to the chassis (ref: FIGURE 11-5), and remove the heatsink.

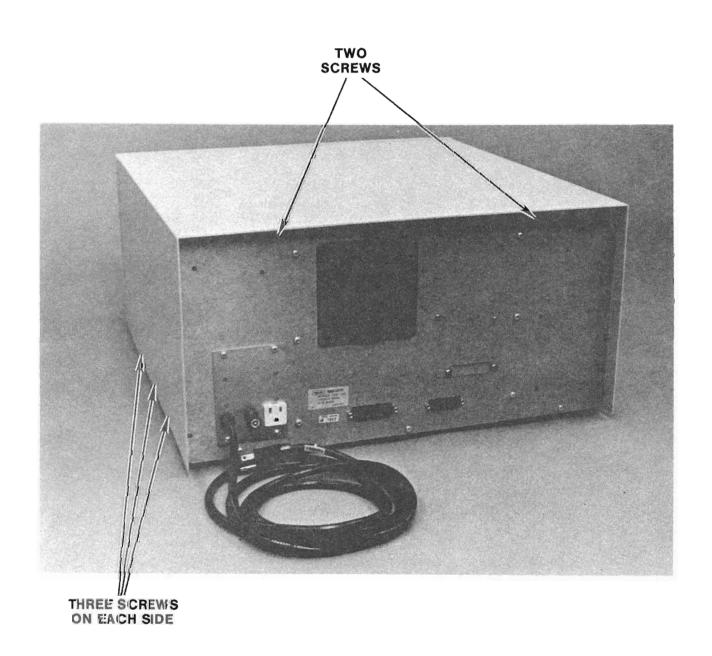
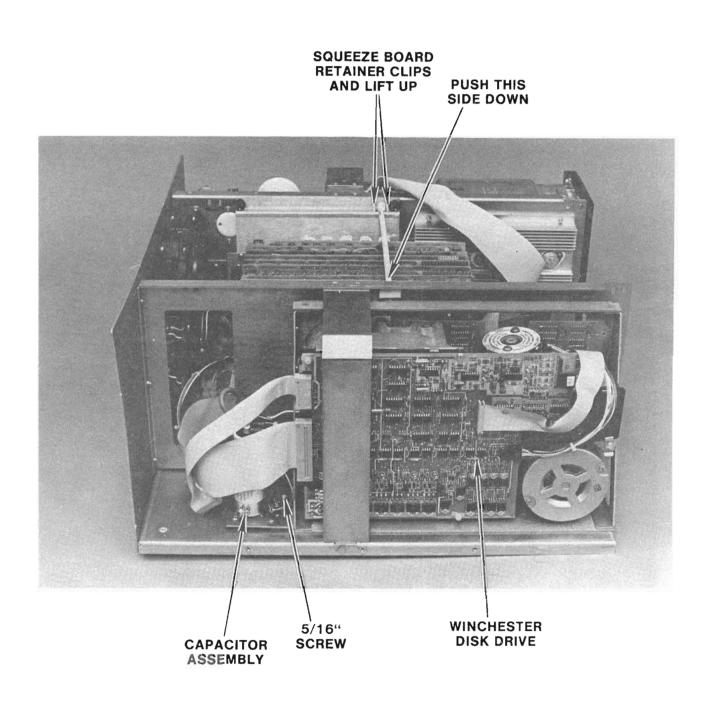


FIGURE 11-3 COVER REMOVAL



IGURE 11-4 CIRCUIT BOARD RETAINER REMOVAL; WINCHESTER DISK DRIVE REMOVAL

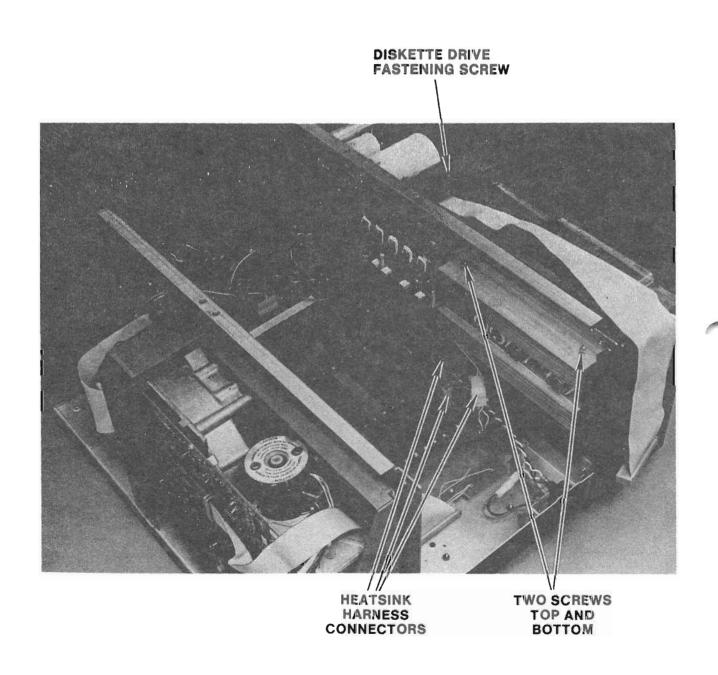


FIGURE 11-5 DSDD DISKETTE DRIVE REMOVAL; HEATSINK REMOVAL

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SECTION 12 TROUBLESHOOTING

Refer to Section 12 of Model 2200LVP Maintenance Manual (IV.A.3.M) for detailed information concerning 2200SVP troubleshooting. The procedures for troubleshooting the SVP and LVP are basically the same. (The 2200SVP uses only one Data Memory board, which contradicts certain sections of the troubleshooting flowchart in the LVP manual.)

SECTION 13 CONVERSIONS

Refer to documentation category I.B.2 for information concerning Data-Memory capacity, and disk drive type/capacity conversions.

SECTION 14 PARTS LIST

DESCRIPTION	WL #
Memory Control Board (CPU) Instruction Counter Board (CPU) Stack Board (CPU) ALU Board (CPU) Register Board (CPU) Data Memory Board32K (CPU) Data Memory Board64K (CPU) Control Memory Board64K (CPU) Control Memory Board64K (CPU) 2200/Disk Interface Board (DPU) Disk Controller Board (DPU) Microcomputer/Memory Board4 MB Drive (DPU) Microcomputer/Memory Board2 MB Drive (DPU) Microcomputer/Memory Boarddual Diskette (DPU) Terminal/Printer Dual Controller DSDD Diskette Controller Power Supply Regulator Board Indicator board CPU/DPU Motherboard Fixed-Disk Drive2/4MB (60 Hz) Fixed-Disk Drive2/4MB (50 Hz) DSDD Diskette Drive (60 Hz) DSDD Diskette Drive (50 Hz) DSDD Diskette (10-pack) Fuse, 2.0A (230 VAC) Fuse, 4.0A (115 VAC) LED, Red Bootstrap PROM #1 Bootstrap PROM #2 Bootstrap PROM #3 DPU PROM #1 (Pwr-On Diag.; 2 MB Disk Drive) DPU PROM #1 (Pwr-On Diag.; 4 MB Disk Drive) DPU PROM #3 (Disk/Diskette Drives) DPU PROM #4 (Disk/Diskette Drives) DPU PROM #3 (Disk/Diskette Drives) DPU PROM #4 (Dual Diskette Drives) DPU PROM #3 (Dual Diskette Drives) DPU PROM #3 (Dual Diskette Drives) DPU PROM #4 (Dual Diskette Drives) DPU PROM #3 (Single-Density Diskette) PLA PROM #3 (Single-Density Diskette) RAM, 16K x 1-Bit Dynamic SVP Chassis Assembly (50 Hz)	210-6789-A 210-6790 210-6791 210-6792 210-6793-1 210-7587-1B 210-7587-1A 210-7694 210-7696-A 210-7696-B 210-7696-B 210-7696-C 210-7789-A 210-7890-A 210-7887 210-7887 210-7887 210-7890-A 210-7888 210-7888 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-788 210-789 210-788 210-788 210-789 210-788 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-789 210-
Power Supply Heatsink Assembly Power Box Assembly Transformer (60 Hz) Transformer (50 Hz) Fan, Muffin M747 Mark IV	270-0159 279-0374 270-0619 270-0619-1 400-1003

Cable, 20-Pin Ribbon (Disk I/O)	220-3133
Cable, 50-Pin Ribbon (Disk I/O)	220-3134
Cable, AC Power (SVP)	220-1462
Cable, AC Power (Winchester)	220-0259
Cable, AC Power (Diskette)	220-0260
Cable, DC Power (Disks)	220-1473

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APPENDIX A

2200SVP ERROR CODES

Refer to 2200VP BASIC-2 Language Reference Manual, WL #700-4080C (IV.C.2), for more detailed information concerning the nature of, and the recovery from the following errors.

Error	Code:	NONRECOVERABLE ERRORS
Misc.	Errors:	
	AOl	memory exceeded (overlap: text & symbol table)
	A02	memory exceeded (overlap: text & value stack)
	A03	not enough memory (LISTDC, MOVE, COPY)
	A04	stack overflow (operator stack)
	A05	line too long
	A06	program protected
	A07	illegal immediate mode statement
	A08	statement not legal here
	A09	program not resolved
Syntax	x Errors:	
	S10	missing left parenthesis
	S11	missing right parenthesis
	S12	missing equal sign
	S13	missing comma
	S14	missing asterisk
	S15	missing angle brackets
	S16	missing letter
	S17	missing hex digit
	S18	missing relation operator
	S19	missing required word
	S20	expected end of statement
	S21	missing line number
	S22	illegal PLOT argument
	S23	missing literal string
	S24	illegal expression or missing variable
	S25	missing numeric scalar variable
	S26	missing array variable
	S27	missing numeric array
	S28	missing alpha array
	S29	missing alpha variable
Progra	am Errors:	
	P32	starting address greater than ending address
	P33	line number conflict
	P34	illegal value
	P35	no program
	P36	underfined line number or CONTINUE illegal

P37	underfined special function subroutine
P38	underfined FN function
P39	FN nested too deep
P40	NEXT without FOR
P41	RETURN without GOSUB
P42	illegal image
P43	illegal matrix operand
P44	matrix not square
P45	operand dimensions not compatible
P46	illegal microcommand
P47	missing buffer variable
P48	illegal device specification
P49	interrupt table full
P50	illegal dimensions or variable length
P51	variable or value too short
P52	variable or value too long
P53	noncommon variables already defined
P54	common variable required
P55	undefined array
P56	illegal subscripts
P57	illegal STR () arguments
P58	illegal field/delimiter specification
P59	illegal redimension

Error Code: RECOVERABLE ERRORS

Computation Errors:

C60	underflow
C61	overflow
C62	division by zero
C63	zero divided by zero, or zero raised to zero power
C64	zero raised to negative power
C65	negative number raised to noninteger power
C66	SQR of negative power
C67	LOG of zero
C68	LOG of negative power
C69	argument too large

Execution Errors:

X70	insufficient data
X71	value exceeds format
X72	singular matrix
X73	illegal INPUT data
X74	wrong variable type
X75	illegal number
X77	invalid partition reference

Disk Errors:

D80	file not open
D81	file full
D82	file not in catalog

D83 D84 D85 D86 D87 D88 D89	file already catalogued file not scratched index full catalog end error no end file wrong record type sector address beyond EOF
I/O Errors:	
190 191 192 193 194 195	disk hardware error (X'CO' not rec'd) disk hardware error disk hardware error (timeout) disk format error format key engaged seek error
195 196 197 198 199	CRC error LRC error illegal sector address read-after-write error

APPENDIX B MECHANICAL DRAWINGS

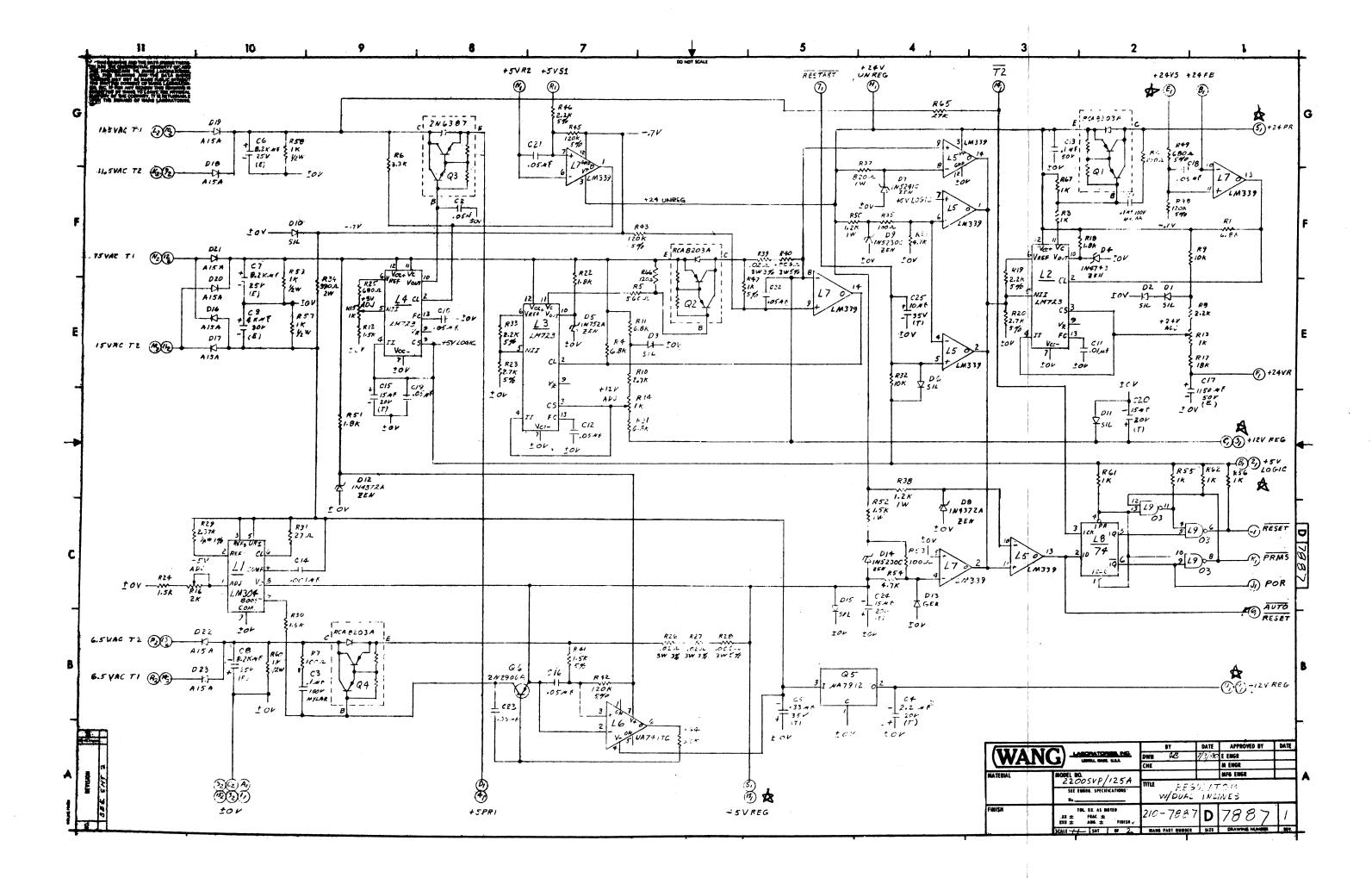
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APPENDIX C SCHEMATICS

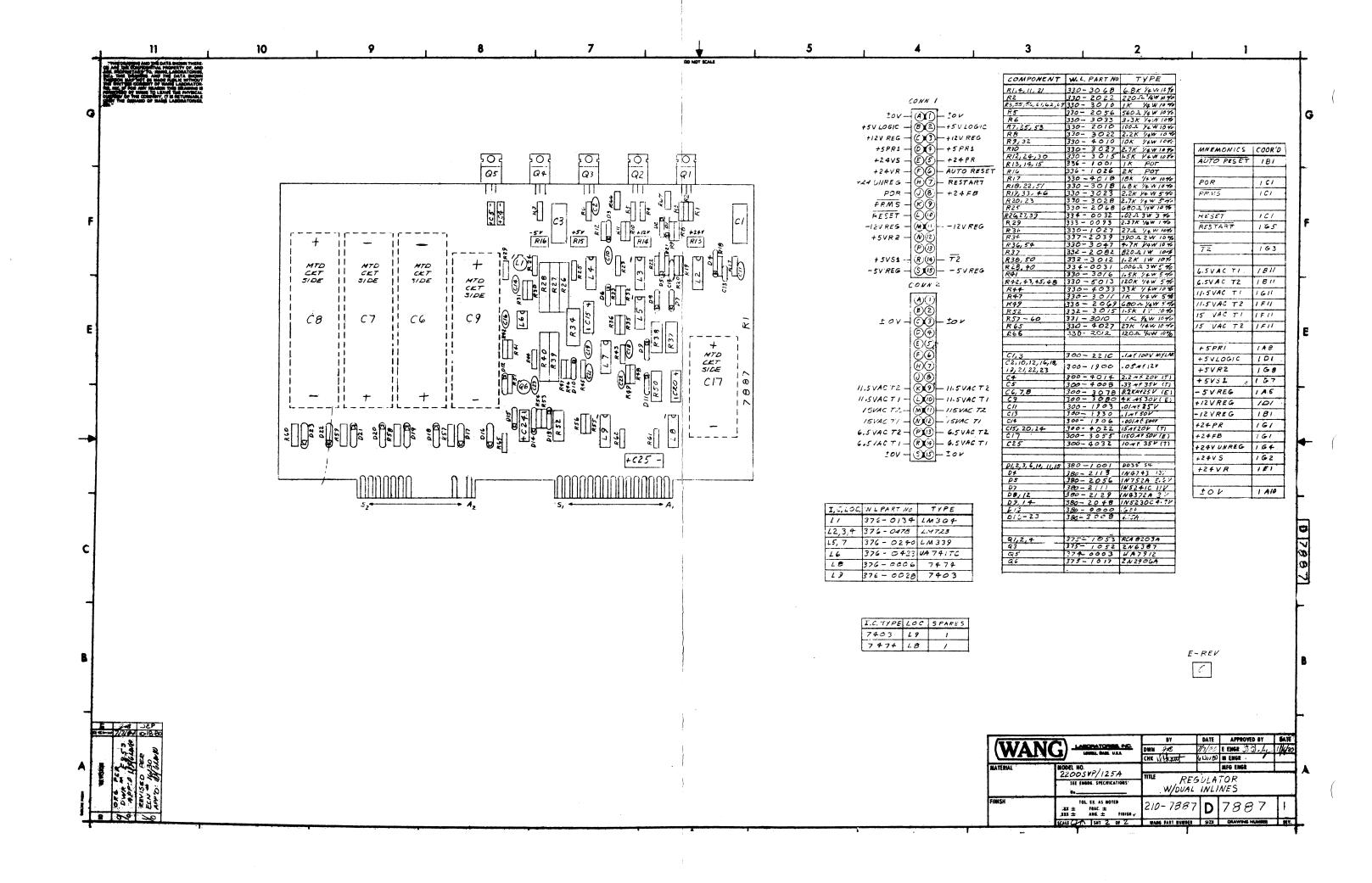
The following schematics are contained in this Appendix.

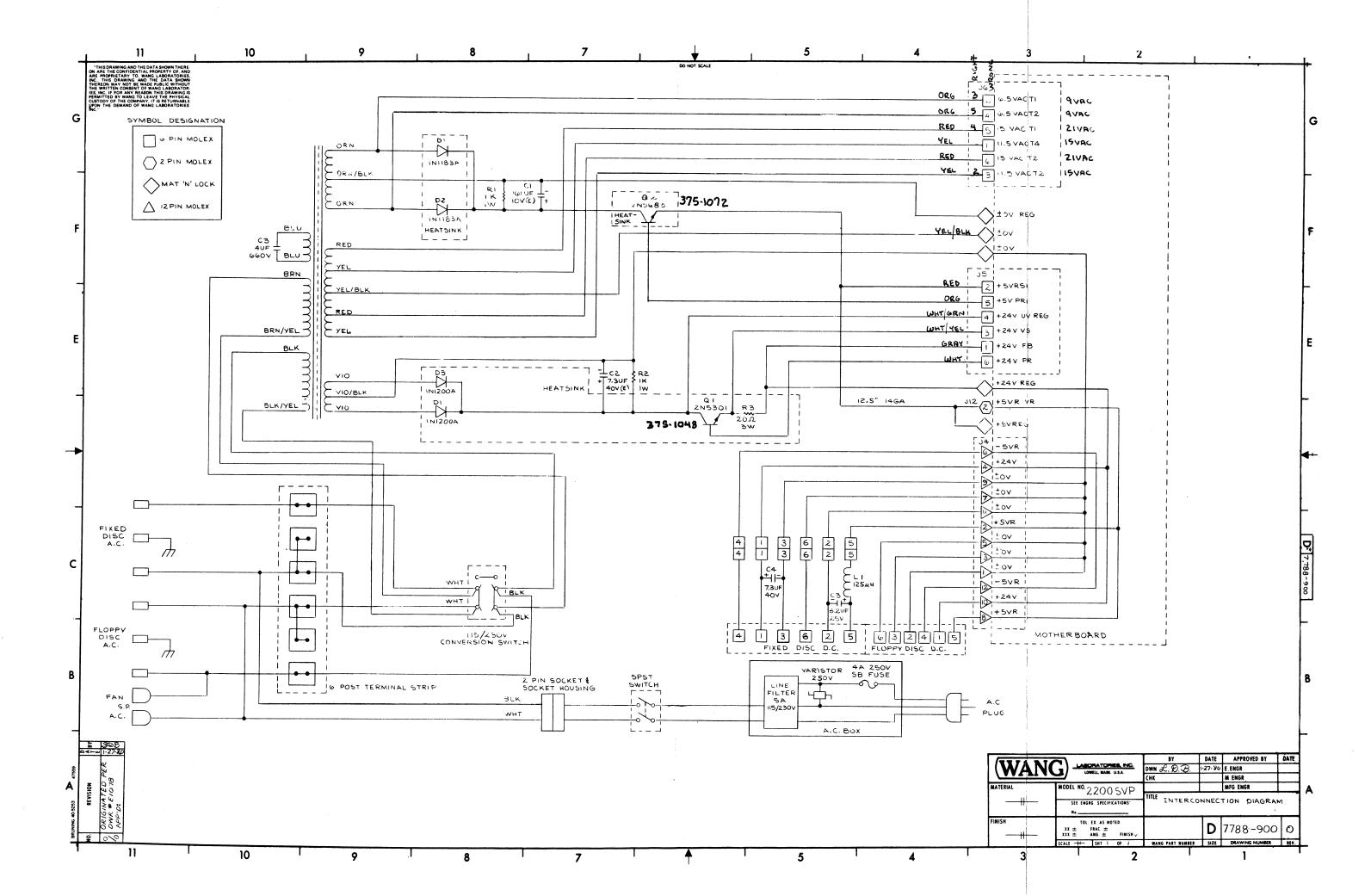
210-7887 Regulator 7788-900 Interconnection Diagram 210-7890 Dual-Diskette Controller

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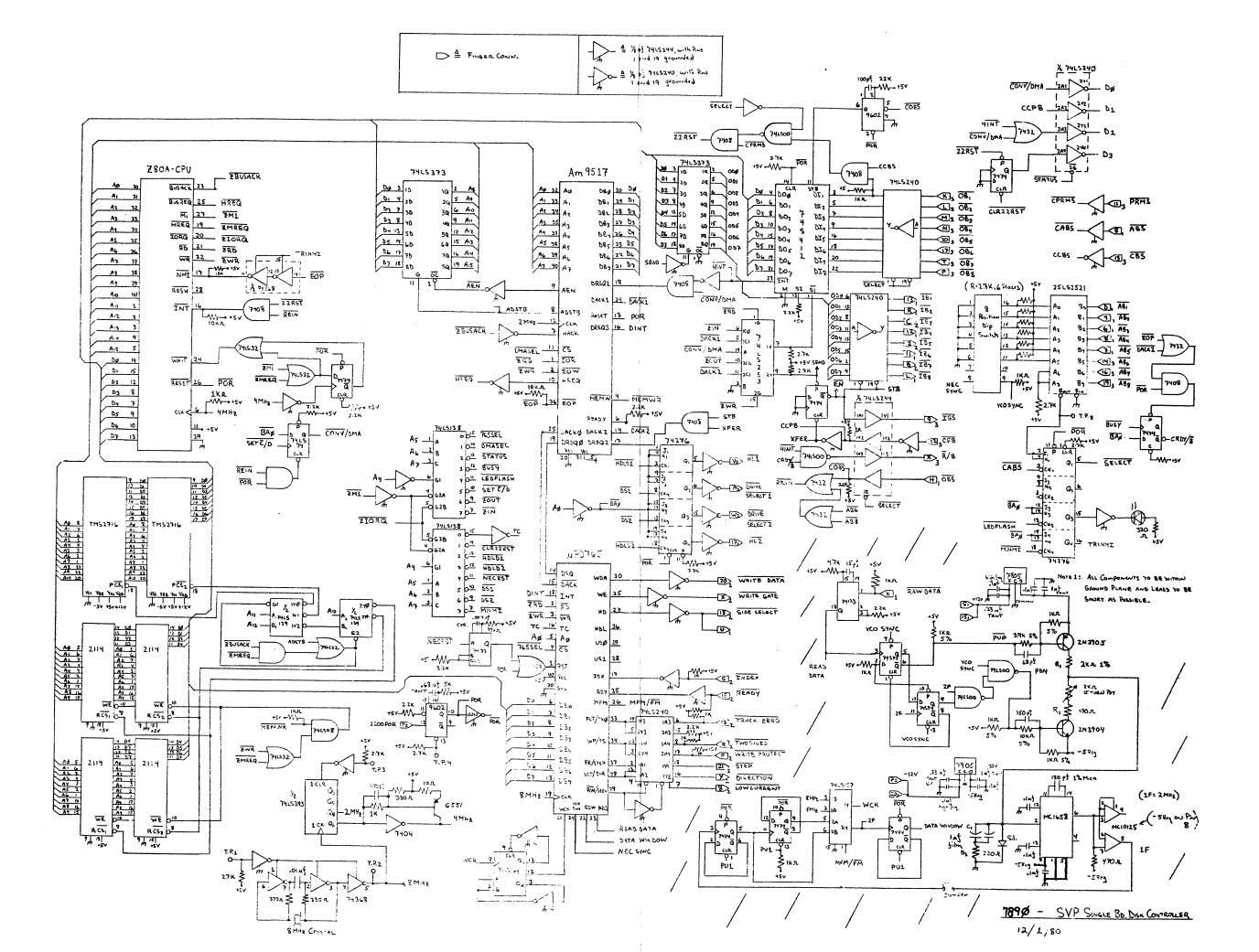
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Nevada Las Vegas Reno

New Hampshire Manchester

New Jersey Toms River Mountainside Clifton

New Mexico Albuquerque

New York Albany Buffalo Fairport Lake Success New York City Syracuse

North Carolina Charlotte Greensboro Raleigh

Ohio Cincinnati Cleveland Middleburg Heights Toledo Worthington

Oklahoma Oklahoma City Tulsa

Oregon Eugene Portland

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Rhode Island Cranston

South Carolina Charleston Columbia

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