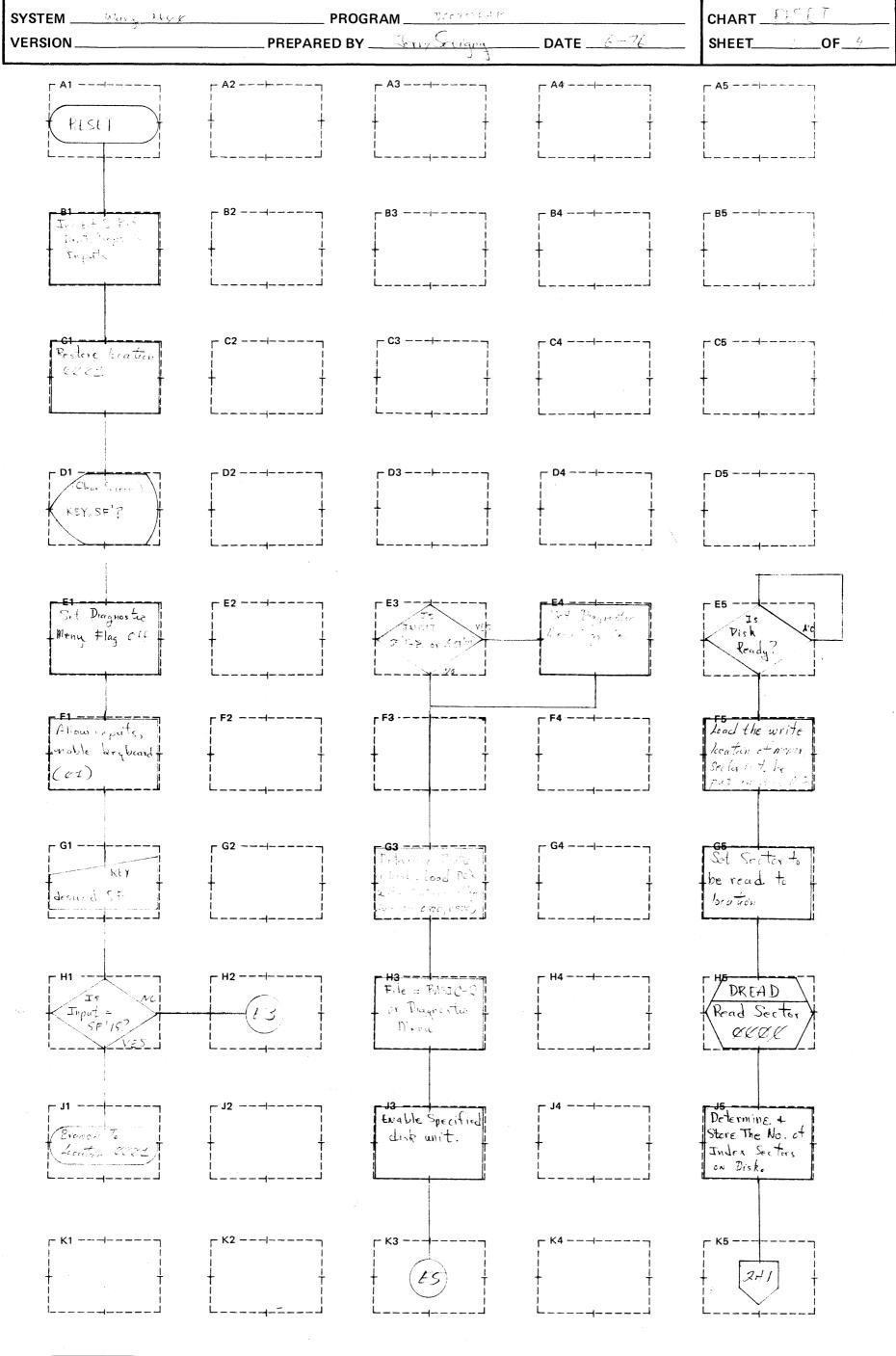


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EM2206VP		OGRAM BOOTSTRAP BY I Sevigny	DATE6/76	_ CHART MASTER INSTITUTIONS PARTS _ SHEET 2 OF 2
Δ1	- A2	- A3	- A4	
VERIFY BOOTSTRAP	MOUNT SYSTEM (SPACE)			_ A5
PROM's	342 LEVI (TIME)	+ +	+ +	†
i			<u></u>	
₹550 € E,4	MICHALT.	ВЗ	F 84	B5
Datla Memory	SYSTEM P	+ +	+ +	+
Helitory				
				·
<u>C1</u>	C2	г cз	r c4	C5
nom/som cpeck	MOUNT SYSTEM			
	PL.			T T
	L	L	L	L
MOUNT SYSTEM PLATTER -	D2	D3	D4	D5
PRESS RESET	+	† †	+	+
F E1	┌ E2	FE3	F E4	_ E5
END				
Hang-Awart Roset				
		<u> </u>	<u> </u>	
FF1	ŗ F2	r F3	F4	r F5
+ +			1	
			-	
F G1	r G2 ¬	- G3	r G4	г G5
† † ! !	† †	† †	† †	† †
L	L	Ĺ	ĹJ	<u> </u>
F H1	⊢ H2	L H3	F H4	Г H5
+ +	+ +	† †	†	†
_ J1 	_ J2	L 13		_ J5
<u> </u>	+ +	+ +	+ +	+ +
<u> </u>				<u> </u>
г K1	۲ K2 −−−−−−¬	г K3	_ K4	г к5⊹¬
T † 	† †	† †	† †	† †
<u></u>	L	Ĺ	·	i



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SYSTEM	PROGRAM	BOCTSTRAP	CHART RESET
VERSION	PREPARED BY JERRY	Svigna DATE 5	76 SHEET 2 OF 4
Set-up Road address (Sion S-bil) Most Evry Adder Most Soly Adder	Znores Entry Addre	Read CS	Point at File Add Round & Store File Heldings
Move Read Address To Pe's and Road Fitty Usage Code.	B3	his r d' kva' YCS	Initialize 8 B. C. Zen & Misses. Réall File Address To Pels.
twhy (cde = Free?	Does S	ector = End of Sectore.	DREAD Read File S'ector
Is listing Code = Active? VES	2	yes 1A1	Store next Store next Old contex decres
Read File	Restore Write Update Adding	Toration. Sector	Road Record Type From S Bit Memory.
FILE Type a Data File? YES		Juntary Contains	F5 - VES Troiler?
Por point at Start of revier Read 1st 20 or	Inition 8 Bit Acidi	G4 Read Re	G5 NC Data? Y45
Nanc Name Search fee	2	B1	3P1 +
J1	2		
F K1	2		K5

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SYSTEM		OGRAMECOTY BY		CHART <u>NESE /</u> SHEET 3_OF _//_	
Point at and Read Black (Comment March)	- A2	Tritializa Interim Dala Canat	A4	Interim Data Count.	
Campend ?	B2	Road data at Road Location et 5' Bit.	F 84	Read 3 char. of Data Front Read Loca Son of 8 B.t.	
Co C	C2	Write data ate New Acoston of 8 P. I. Pota Non	C4	Ling 3 Changes as K, P.4, P. 189	
Stors Block Type	D2	Decrement Data Count	D4	Decrement Data Court	
Read block Start Address. And Stare.	E2	Pola Court	2B5	Pala Cont	
Read Stere	F2	Decrement Juterim Pata Court	F4	Decrement Juteville Data Count.	Fold unde
Slore Start	G2	July in Date (cut	B3	G5 Je Krish Dala-Fi B5	r at dotted line.
Plack Type Data?	H2	Adjust Road	H4	Adjust Rend Lecution	
A5)	Evable CRT	Display Comment	Enable Disk	J5	
K1	K2	K3	ZBS	K5	
+ +	· · · · · · · · · · · · · · · · · · ·	+	285	+	

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SYSTEM		BUTSTRAP	CHART
VERSION	PREPARED BY A3	A4	SHEETOF
Neva Elan VESI	Enalla Cry Read !		† †
VE RJFY2Y	B2	a, B4	B5
Verify Centre L	New wide	*** † † †	† † † † † † † † † † † † † † † † † † †
C1 - Verily Ac	Vent, Errer	C4	C5
Chay?	Centrel Memory)		
VERIFYE VERIFYE	D2	Fr. D4	□ D5
Mentery			
Verify A a	Part, Erver Pata Memery		F E5
Prach to	F2	F4	F F5
	r G2		
+ +	+ + +	+ + +	† + +
└- H1}	⊢ Н2 −−−┤−−−−		ŗ н5⊢¬
			+
_ J1			「J5
			+ +
F K1	Г K2 Г K3		Г КБ ————————————————————————————————————
+ +	+ + + + + + + + + + + + + + + + + + + +		+ +
	,		

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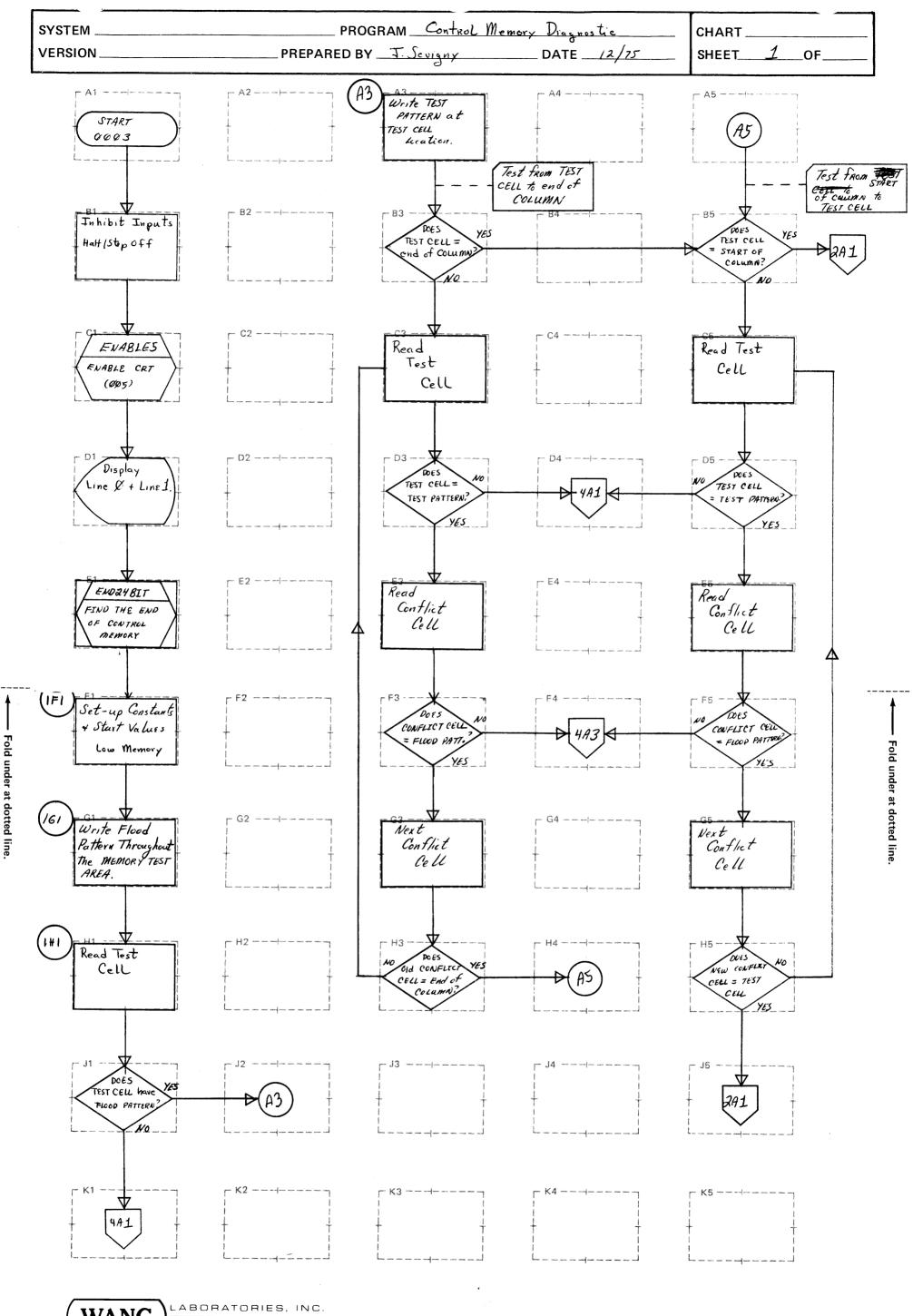
CONTROL MEMORY DIAG.

	003 *	TITLE CONTROL MEMORY DIAG. ROWP24:
	004 *	This routine will perform a test of 24
MARK THE MARK THE TOTAL CO. CO. ST. ST. ST. ST. ST. ST. ST. ST. ST. ST	005 *	bit CONTROL MEMORY. The algorithm used is a
	00€ *	modified ROWPAT.
	007 *	
	008 *	To explain the algorithm it is necessary
	009 *	to define certain terms -
	010 *	TEST CELL - that location being tested.
	011 *	CONFLICT CELL - that location being
		tested for a CONFLICT
	W	with the TEST CELL.
	W 45 447	
A CONTRACTOR OF THE CONTRACTOR	014 *	ROW - a row of addresses within the
	015 *	memory chip of which the TEST
	016 *	CELL is one of the addresses.
	017 *	COLUMN - a column of addresses within the
	018 *	memory chip of which the TEST
	019 *	CELL is one of the addresses.
AND THE RESERVE OF THE PROPERTY OF THE PROPERT	020 *	BOARD ROW - a row of memory chips located
	021 *	on the memory board.
	O22 *	TEST PATTERN - that pattern expected to
	* 650	be found in the TEST CELL.
	024 *	FLOOD PATTERN - that pattern expected to
	025 *	be found in all other cells.
	026 *	MEMORY TEST AREA
	027 *	- from 0000 to END OF MEMORY - 0800
	028 *	if program is in low memory.
	029 * •	- from 0800 to END OF MEMORY if
	030 *	program is in high memory.
	031 *	program 15 10 memory:
	032 *	The ALGORITHM is -
STREET, CONTROL OF THE STREET,	033 *	1. Write zeroes to all locations in
		the current MEMORY TEST AREA.
	~ · ·	
And the second s	035 *	2. Read current TEST CELL and check
	036 *	for TEST PATTERN.
	037 *	3. Write the TEST PATTERN at the
and a Market definition of the contract of the	038 *	TEST CELL.
	O39 *	4. Read TEST CELL and check for TEST
	040 *	PATTERN.
NAME OF MARKET AND ASSOCIATION OF THE PROPERTY	W FA	and it to send the grid for an interest and send on a second send on a construction of the send of the send of
	042 *	for FLOOD PATTERN.
	043 *	6. Repeat steps 4 and 5 making the
	044 * *	CONFLICT CELL the next location
	045 *	within the COLUMN and then within
	046 *	the ROW.
CONTRACTOR	047 *	7. Repeat steps 2 through 6 making
	048 *	the TEST CELL the next location
	049 *	within the CHIP ROW until the TEST
	050 *	CELL has occpuied each memory
	051 *	location within the CHIP ROW.
	052 *	8. Repeat steps 2 through 7 for each
Management and Assessment of the Reserve		CHIP ROW within the MEMORY TEST
And the second s		
	- · · · ·	AREA.
	055 *	9. Write all one's into the MEMORY

```
056
        쑛
                                TEST AREA and repeat steps 2
     4
                              through 8.
057
                           10. Move the program from low memory
058
     35.
                              to high memory and repeat steps 1
059
                              through 9.
060
     ¥
     뀾
061
062
     ¥
                 MODIFIED REGISTERS:
063
                      FO - F5. AUXOO - AUX17. PL. PH
     Ŋ.
064
065
     놧
066
                 REGISTER USAGE:
                      AUX OO - start address of CHIP ROW
067
     4
                      AUX O1 - end address of CHIP ROW minus 1.
830
     ж.
                      AUX 02 - start address of COLUMN
     4
069
                      AUX 03 - end address of COLUMN
070
     뀾
     *
                      AUX 04 - start address of ROW
071
                      AUX O5 - end address of row minus 1
072
                      AUX 06 - TEST CELL address
073
     쏬
                      AUX 07 - CONFLICT CELL address
074
     4
     ж.
                      AUX 08 - END OF MEMORY minus 1
075
                      AUX 09 - constant 0020
076
                      AUX OA - constant OFCO
     ¥
077
                      AUX OB - constant FO3F
078
     괒.
                      AUX OC
                             - constant OFFE
079
     *
     *
                      AUX OD - temporary storage
080
                      AUX OE - temporary storage
081
     *
                      AUX OF - temporary storage
082
                      AUX 10 - loop counter
083
     놧
084
     ¥.
                      AUX 11 - temporary storage
                      AUX 12 - old MEMORY TEST AREA pointer
085
                      AUX 13 - new MEMORY TEST AREA pointer
     4
086
                      AUX 14 - end of program pointer
087
                      AUX 15 - end of MEMORY TEST AREA pointer
880
                      AUX 16 - start of MEMORY TEST AREA point.
089
     ÷
                      AUX 17 - start low memory address pointer
090
                              - TEST PATTERN
     汝
                      FO
091
                              - constant 00
092
     *
                      F1
660
                      F3,F2
                              - constant 0020
                      F5.F4
                              - working register pair
094
     *
095
     *
                 SCREEN DISPLAY AND MESSAGES
098
     4
097
     ¥
                       line O - ROWPAT TEST - 24 BIT RAM
     Ŋ.
098
                       line 1 - # LLLL
     ¥
099
     *
100
                      where: line O = diagnostic title
101
     *
                                LLLL = # of completed loops
102
                                        through diagnostic
103
     쑛
104
     ¥
105
     *
                 ERROR MESSAGES
106
     뀾
                   1. FAILURE AT PC'S FFFF
                                              (EEEEEE/RRRRRR)
107
     *
                                            XOR = XXXXXX
108
     괒
                   2. CONFLICT BETWEEN TITT AND CCCC
109
```

And the contract of the contra

	- Tomas	The second of th	F all Super for
· · · · · · · · · · · · · · · · · · ·	110 *		
	110 * 111 *	where Europe	failing memory address
•	112 *		expected pattern
	113 *	EEEEE -	
		nnnnn .	form (K,PH,PL)
		RRRRR	= actual pattern
•	115 *		form (K,PH,PL)
The second secon	116 *		XOR of expected/actual
	117 *		TEST CELL address
	118 *	cccc :	= CONFLICT CELL address
en e	119 *		
	120 *	DISCUSSION OF ERRO	OR MESSAGES
	121 *		
	122 *	ERROR 1 oc	curs when either registers K,
	123 *		contain the expected pattern.
	124 *	ERROR 2 oca	turs when an ERROR 1 occurs
· · ·	125 *		read and either K,PH or PL
	126 *	contain the TEST F	
	127 *	the took of the tentral of the fittee of the control of	
	128 *	**** RESET ***	\$- 3 \$
	129 *		s keyed a branch to the
			SYSTEM DISK' routine is
	an my ha		SYBIEM DISK, LOUTING 12
	131 *	executed.	
	132 *		
	133 *	***** HALT/STEP	
· · · · · · · · · · · · · · · · · · ·	134 *		may be interrupted by keying
	135 *	HALT/STEP. However	r, the program will only halt
	136 *	after an error mes	ssage has debb displayed. To
<u> </u>	137 *		program, key HALT/STEP again.
	138 *	·	
	139 *	***** I/O SUBROU	TINES ****
	140 *		makes use of the BOOTSTRAP
	141 *	subroutines whenev	
	142 *		
	143	SYMBL JSMDDO2\$	
	144 *	STREE JSREDGET	
	145	nra.	
	145	B MUUN1	
	147	B PE8	
	148	B START	
The second of th	149		
	150		
	151		
w	152		
	153		
	154		



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SYSTEM	PROG	RAM Control Men	mory Diagnostic	CHART
VERSION	PREPARED BY	J. Sevigny	DATE	SHEETOF
- A1	- A2	- A3	p. A4	_ A5
		(4.43)		
(441)		443		
7	. C 11		Conflict Cell	The same same same same same same same sam
lest	Cell adure		Failure	
Stove a ctual Road		Store actual Rod	84	B5
Failing PC's Expected Road		Expected Read		
Expected Road		Failing R3		
Man day and and and and and	Notes come danne come come come come dans come dans dans dans dans dans dans dans dans		how were care and over each over one you me, you knot	have survey comes comes comment quarter comes comes comes comes comes
Display	C2	NO K, PH or PL	C4	C5 and
ERROR 1		= TEST PATERN?		
	men, anne men some men anne anne anne men ran ran men anne	YE-5	THE MAIN AND ALL OLD THE BEST STORE AND AND THE	Notes that have been place again again that the real rate and
D1 - V	- D2	_ D3	D4	r D5
HALTSTEP		Display FRROR 2		
Check Halt/Step		The same of the sa	†	
	Make total rate when come desire cores years more want come	The same was the same and the s	The same will state and same same same same same same	The case was now and over any over the case and over the
	pro E2 me and and an and an and	E3		Les E2 con one tout one are one and
tero Loop Counter				
	the contract of the contract o	house come Arm was well created from was come come come and	have now more than the same and form the contract and their	have now now more and pool over now and the control over
. F1	per \$52 ver was word as we are were were war	po \$3 a cas and confront one were some true to	poor Fi 4 com com complecio com com com comp	pour F. C. and and and and and and and and
Display				
New Loop Count				†
	were store come come man, come factor store taken appet taken and	The state of the s	have seen over over made and seen take also the true	have now now now comprise the same was now and
G1	G2	G3	pu G4	G5
Prog NO	354		+	
The Deal Western				
house never track while trick shall because was was care care read.	have now and van van mad and and and and and and and	have their come over the second of the trip the second over th	have never some some money power some some some some some	have used used used and standy used state above used used and
Part 141 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	F H2	H3	pur field our own real our own our own our real	р H5 — — р — — — — — — — — — — — — — — — —
141	+			
And 1000 0000 0000 0000 0000 0000 0000 00	was care was some and designed and some some some some some	The case was and many care that and the	The right with 1670 alon stand date. Mark made once over and	Market Colors State Annual Color State Colors Annual Colors Annual Colors Color
	,			
and J1 were seen compared once seen some some some	r J2	r J3	pm J4	r J5
T				
the over our our tool one one our our our	has also seen seen some page also man one one with and	have seen to see that were was page one and the true and	The same same same sound notes about some same sound sound sound	
K1	K2	K3	K4	K5
<u> </u>	<u> </u>	+		
and the second course when the second course were the second course when	The state of the same of the state of the st		AND THE PERSON NAMED AND ADDRESS OF THE PERSON NAMED AND ADDRE	States about which waster colors departed market mirror about popular sports.

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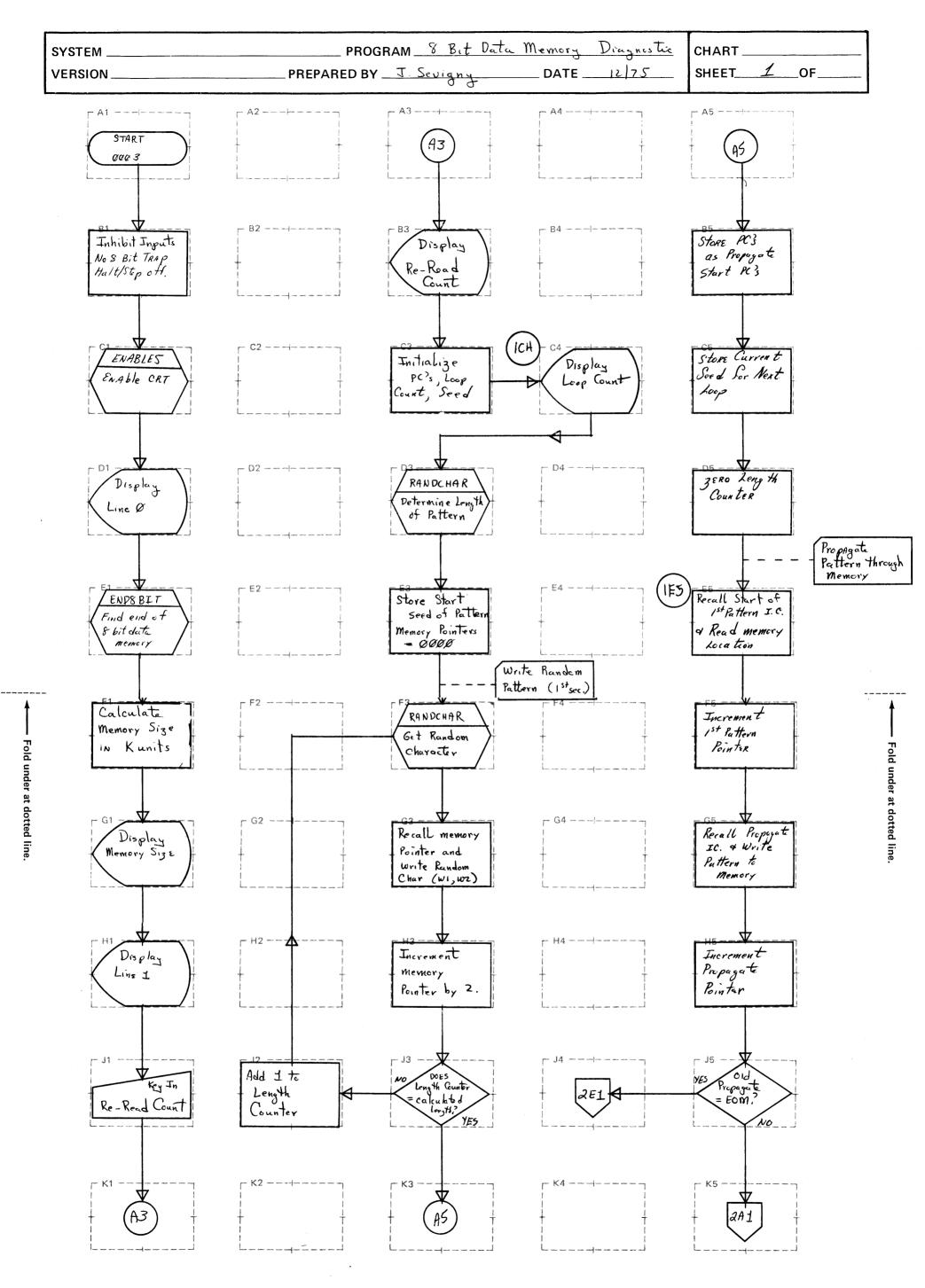
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2600	MAT	COPY &	SEARCH FILE
	002	TITLE	2600 MAT COPY & SEARCH
	003 *		
	004 *		
	005 *		This diagnostic attempts to duplicate the OPT 5 BASIC diagnostic for memory. The
	005 *		algorithm used is as follows:
	007 *		marrian decare as as introduced and an interest
	009 *		STEP 1.
	010 *		Determine the length of the RANDOM
	011 *	But appears on Marchan and Appears of the second of the se	PATTERN to be written to all of memory.
	012 *		The length is from 1 to 256 8 bit
	013 *		RANDOM CHARACTERS.
	014 *	ter angeleigen mer melde er i begrenne mende in men. S. de France	. The second
	015 *		STEP 2.
	016 *		Write the RANDOM PATTERN into
	017 - *		memory.
	018 *		per, representation and
	019 *		STEP 3. Read the last written section of
	020 * 021 *		memory and write it into the next
	055 *		section of memory.
	∨cc ^ 023 *		Section of memory:
	024 *	Programme and the second of th	STEP 4.
	025 *		Repeat step 3 until all of memory is
	ŏ≥€ *		filled with the RANDOM PATTERN.
	027 *	•	
	028 *	•	STEP 5.
	029 *		Read the contents of the 1st pattern
	030 *		in memory and verify that it is correct
	031 *		by re-generating the pattern.
	033 *		STEP 6.
	034 *		Using the 1st pattern section of
managagaganakan managagagan kelalang kangan kengan kelalah di danagan salah dalah dalah dalah dalah dalah dalah	035 *		memory as the original, read the remaining
	036 *		patterns in memory and verify them
	037 *		against the 1st pattern section.
BETTER B	038_ ≉	the special property of the special sp	
	Ø39 *		STEP 7.
	040 *		Repeat steps 5 and 6 the RE-READ
TRANSPORTED TORONO TO STATE OF A PROCESSION OF THE STATE	041 *		COUNT # of times. The RE-READ COUNT is
	042 *	And the second s	decided by the operator.
	% E40 * 440		MODIFIED REGISTERS
A CONTRACTOR OF THE CONTRACTOR	045 *		FO - F7, PC'S, CH, CL, SH
	046 *		AND AUX OO - AUX OC
	047 *		THOUGHT DOWN TOWARD TO SERVE WE WE
	048 *	•	REGISTER USAGE:
	049 *		FO - high 8 bits of END OF MEMORY
MERCAL ZANTARIE PAR ALERA, "A PARENTAMENTA PRINCIPAL PARENTA AND EMPLOYMENT AND EMPLOYMENT AND ANALYSIS AND	050 *	Management of the second secon	F1 - RE-READ COUNT (USER INPUT)
	051 *	•	F2 - length of RANDOM PATTERN
	052 *		F3 - current byte of pattern
			F4 - constant FE
The contract of the contract o	053*		
	054 * 055 *		F5 - length counter F6 - temporary storage

2600 MAT COPY & SEARCH

	056 *	F7 - RE-READ COUNTER
	057 *	CH,CL - read registers
	058 *	SH - status register
	059 *	
	060 *	
	061 *	AUX 1.0 - random charactern seed
	062 *	AUX 3,2 - current pattern initial seed
	063 *	AUX 4 - 1st section memory pointer
	064 *	AUX 5 - loop counter
A	0 65 *	AUX 6 - previous section mem pointer
	066 * 067 *	AUX 7 - current section mem pointer
	068 *	AUX 9,8 - next loop seed AUX 8,A - spare
	069 *	AUX C - last full section in memory
	070 *	TON U TOST TUIL SECTION IN MEMOTY
THE STREET PROPERTY AND ADDRESS OF THE STREET STREET, THE STREET STREET STREET STREET, THE STREET,	071 *	erander er en erande er en
	072 *	SCREEN DISPLAY AND MESSAGES
	073 *	
Not high and the second of the control of the contr	074 *	line O - MATC&S - MEM SIZE = SSK
	075 *	line 1 - RC = RR
	076 *	line 2 - # XXXX
	-077 *	
	078 * 079 *	where: MATC&S - diagnostic title
	080 *	SS - memory size RR - RE-READ COUNT
The second of the second secon		
	081 * 082 *	XXXX - # of completed loops
		through diagnostic
. /	083 * 084 *	ERROR MESSAGES
	085 *	ERRUR PIEDOMGED
	086 *	1. ERR - (PATTERN) L = YYY
	087 *	2A. PC'S = XXXX (EE/RR) BIT(S) N N N
	088 *	OR 28. PC'S = XXXX (EE/RR) BIT(S) N N N OR
	089 *	PC'S = ZZZZ
	090 *	3. CH/CL PARITY BIT ERROR PC'S = XXXX
	091 *	
	092 *	where: PATTERN = RANDOM PATTERN
	093 *	YYY = length of pattern
	094 *	XXXX = failing PC's
	095 * 096 *	EE = expected pattern
	097 *	RR = read pattern N = failing bits
AND CONTRACTOR OF THE PROPERTY OF THE PROPERTY AND THE PROPERTY OF THE PROPERT	098 *	ZZZZ = location of another
	099 *	possible failure.
	100 *	
NAMES TO THE OWNER OF THE PROPERTY OF THE PROP	101 *	DISCUSSION OF ERROR CONDITIONS
e de la companya del companya de la companya del companya de la co	102 *	
	103 *	1. Error 1 & 2A is displayed when a hard error
Make the country of the second of the Astronomy of the second of the sec	104 *	causes all of memory from the discovered
	105 *	memory location to the end of memory to be
	106 *	to be bad.
	107 *	2. Error 1 & 28 is displayed when the
	108 *	discovered point of error does not cause
-	109 *	the rest of memory to be bad. This may be

×		0	* the result of a toggling bit prior to the
•	111		discovered error.
	112	*	3. Error 3 is displayed when the system
And continued the continued th	113	*	detected bad parity but the read was found
	114	*	to be good. This may be the result of a bad
	115	*	parity bit. However it is not possible to
	116	*	decide whether the CH or CL parity bit was
	117	*	in error.
	118	*	In error.
	119	*	***** HALT/STEP *****
	120	*	It is possible to halt the program by keying
	121	*	HALT/STEP. However the program will only HALT
	122	**	after it has reportes an error. To resume with
	123	*	this program, key HALT/STEP again.
	124	*	
	125		***** RESET *****
	126	*	When RESET is keyed the program will execute
	127	*	the POWER ON routine in BOOTSTRAP.
	128	*	
	129	*	***** I/O SUBROUTINES *****
	130	*	The program uses BOOTSTRAP I/O ROUTINES
	131	*	whenever possible.
보고하는데 기념하는 것 같습니다. 이 시간에 되었다. 1980년 - 1985년 1일 전 1980년 1일	132	*	
	133	*	SET PARALLEL TRAP LOACTIONS
	134	*	
	135	₩	



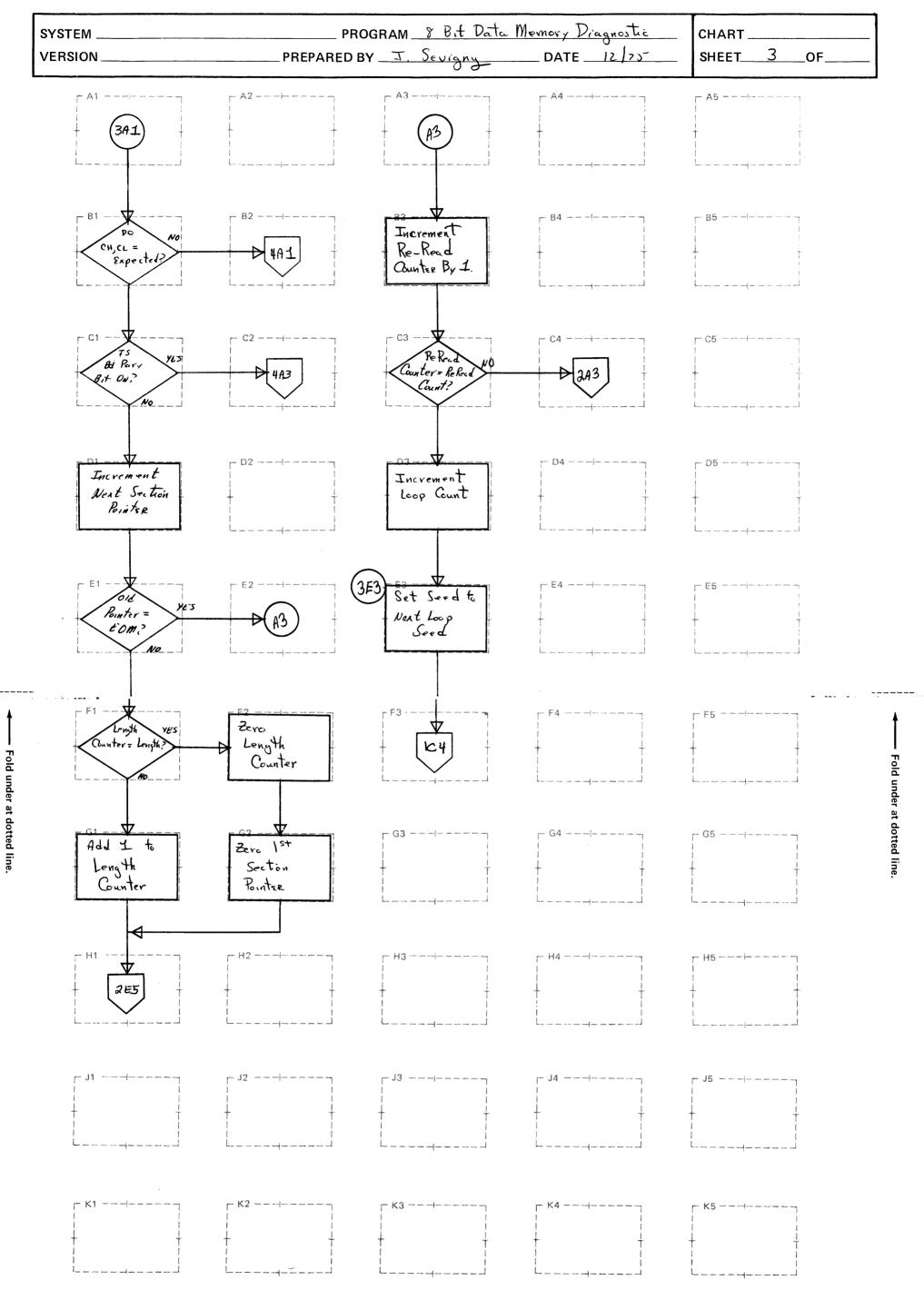
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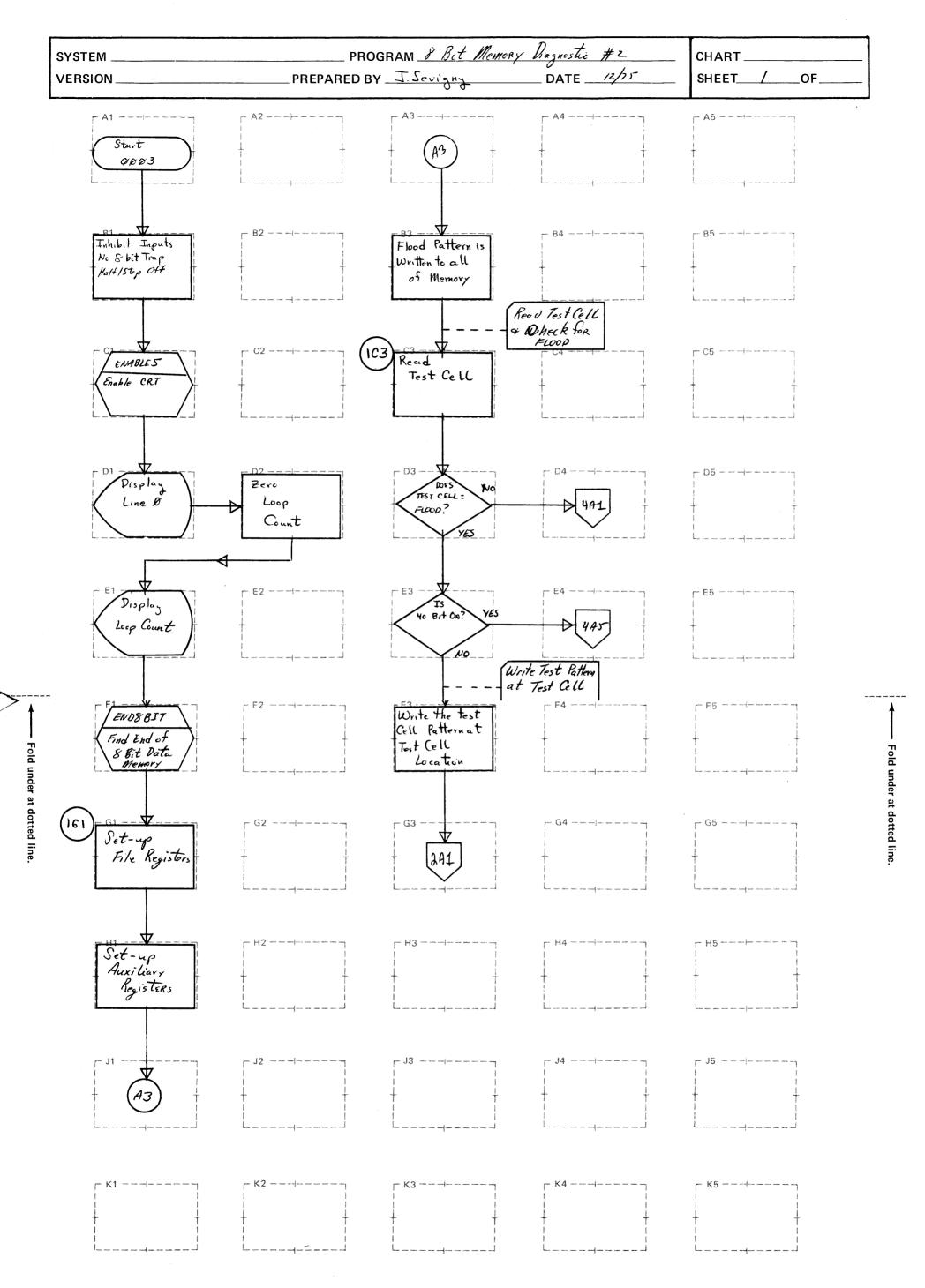
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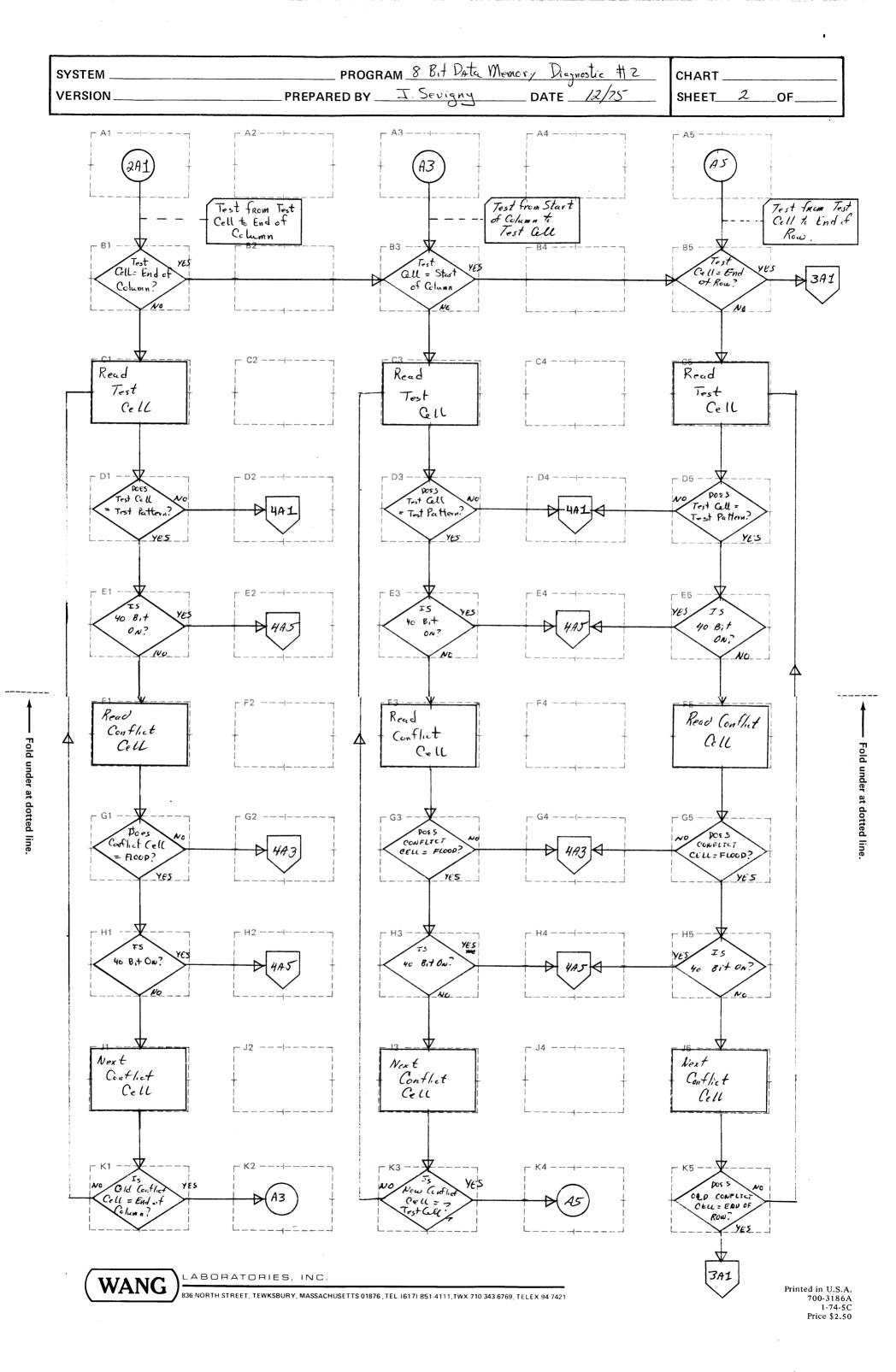
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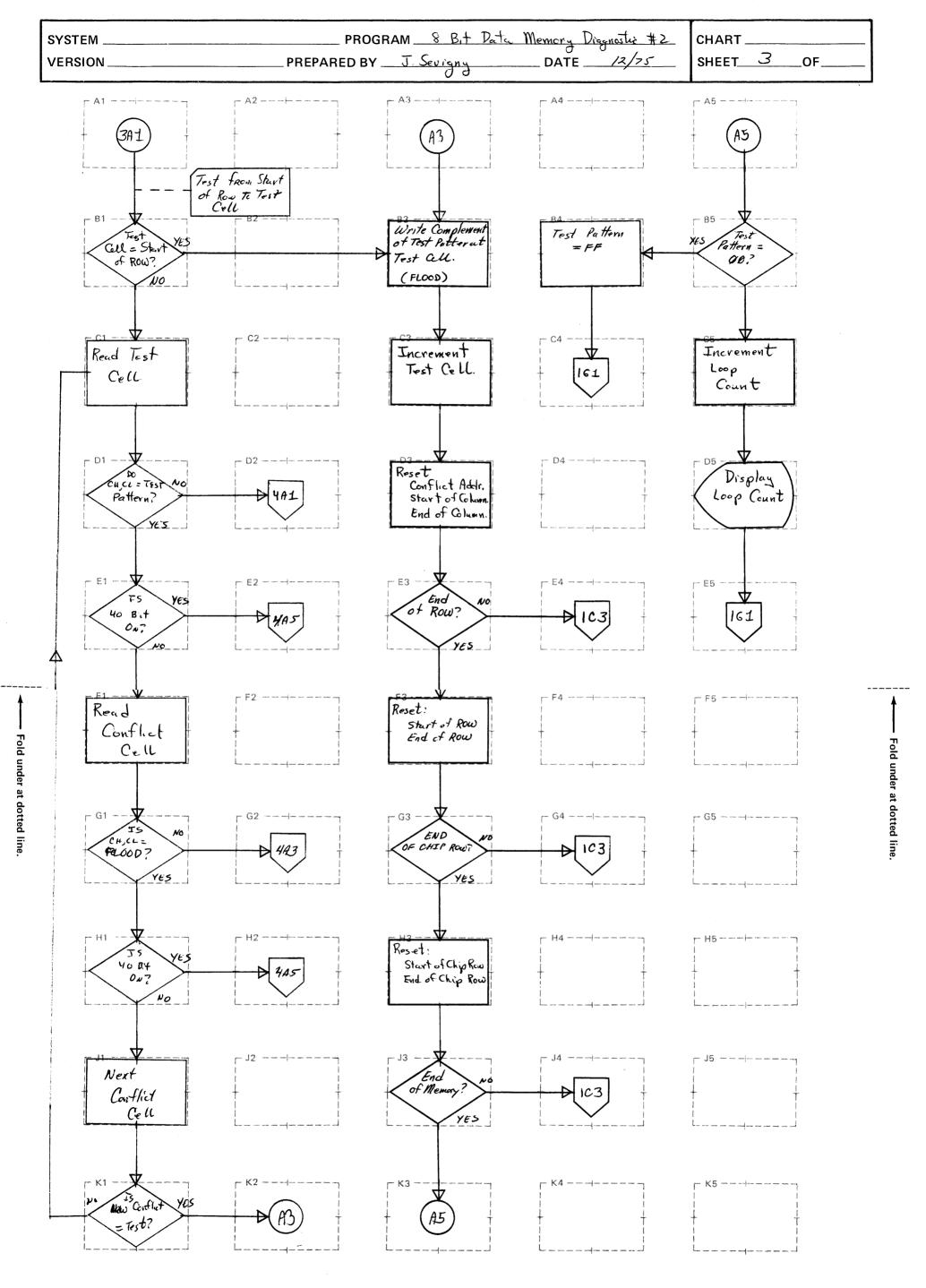
	002	TITLE ROWPAT 8 BIT MEMORY
\(\frac{1}{2}\)	003 *	ROWPOS:
	004 *	This routine will perform a test of 8
	005 *	BIT DATA MEMORY. The algorithm used is a
	006 *	MODIFIED ROWPAT.
		HUDITICO ROWEH!
		,
en deservation of the second o	008 *	To explain the algorithm it is necessary
	009 *	to define centain terms -
	010 *	TEST CELL - that memory location being
	011 *	tested.
	012 *	CONFLICT CELL - the other memory location
	013 *	being examined for a conflict
	014 *	with the TEST CELL
	015 *	ROW - those addresses making up a ROW
	016 *	within the memory chip of which
	017 *	the TEST CELL is one of the addr.
	018 *	COLUMN - those addresses making up a
	019 *	COLUMN within the memory chip of
	020 *	which the TEST CELL is one of the
SECTION OF MARKET A 200 MAYS A CONTINUE OF MARKET SECTION SECTION SECTION OF A CONTINUE AND A CONTINUE OF A CONTIN	021 *	addresses.
	ter Ann Ann	CHIP RDW - a row of memory chips located
	The state of the s	on a memory board.
	024 * 025 *	TEST PATTERN - that pattern written at
		the TEST CELL location.
	026 *	FLOOD - that pattern written to all
	027 *	memory locations except for the
	058 *	TEST CELL location.
	029 *	
	030 *	
	031 *	The ALGORITHM is -
	032 *	1. Write the FLOOD PATTERN of all
	033 *	zeroes throughout all of memory.
	034 *	2. Read TEST CELL and check that it
	035 *	contains the FLOOD PATTERN.
ente entre est est entre l'ances e l'est acteur deserments et l'est est est l'arce les estes et l'est est est	036 *	3. Write the TEST PATTERN (the
	036 *	complement of the FLLOD PATTERN)
		at the TEST CELL.
		4. Read the TEST CELL and check for
	040 *	the TEST PATTERN.
	041 *	5. Read the CONFLICT CELL and check
	042 *	for the FLOOD PATTERN.
	043 *	6. Repeat steps 4 and 5 with the
dente del 100 de como de descripción de la composição de composição de como de como de como de como de como de	044 *	CONFLICT CELL at each location in
	045 *	in the COLUMN.
	046 *	7. Repeat steps 4 and 5 with the
	047 *	CONFLICT CELL at each location in
	048 *	the ROW.
	049 *	8. Write the FLOOD PATTERN at the
	050 *	TEST CELL location.
antennational and engineer represents 1 (1979) 1 - Entennis (1970) 10 (1971) 11 (1971) 12 (1971)	051 *	9. Repeat steps 4 through 8 with the
	052 *	· · · · · · · · · · · · · · · · · · ·
		TEST CELL at each location in the
	053 *	
	054 *	10. Repeat steps 4 through 9 with the
	055 *	TEST CELL at each location in the
2		AND THE RESERVE OF THE PROPERTY OF THE PROPERT

	056 *	CUID DOW
The second secon	057 *	CHIP ROW.
		11. Repeat steps 4 through 10 with
	058 * 059 *	the TEST CELL at each location in memory.
	O6O *	12. Write a FLOOD PATTERN of all
	061 *	ones into memory.
	062 *	13. Repeat steps 2 through 11.
	0 6 3 *	
	064 *	MODIFIED REGISTERS:
	065 *	FO - F5, AUXOO - AUX10, SL, PL, PH
	066 *	10 10% MONOO MONTOS CES 1125 111
	067 *	REGISTER USAGE:
	068 *	AUX OO - start address of CHIP ROW
	069 *	AUX 01 - end address of CHIP ROW minus 1
	070 *	AUX O2 - start address of COLUMN
	070 *	AUX OB - end address of COLUMN
With Mark and State and St	was an extension over the common same and the common and the common same and the common same at the common same and the common same at the common	
		AUX 04 - start address of ROW
	.	AUX 05 - end address of ROW
	w : .	AUX 06 - TEST CELL address
	w	AUX 07 - CONFLICT CELL address
	076 *	AUX OB - end of memory minus 1
**************************************	077 *	AUX 09 - constant 0040
	078 *	AUX OA - constant OFCO
•	079 *	AUX OB - constant FO3F
	080 *	AUX OC - constant OFFE
	081 *	AUX OD - temporary storage
	082 *	AUX OE – temporary storage
	083 *	AUX OF - temporary storage
	084 *	AUX 10 - loop counter
	085 *	FO - TEST PATTERN
	086 *	Fi - constant 00
Marine Sales and Substantia, An Administration (A) and definitions of the Sales and th	087 *	F3,F2 - constant 0040
	088 *	F5,F4 - working register compare
	089 *	
	090 *	MEMORY BOARD LAYOUT (CHIP #'S)
	091 *	MEMORY BONKO CHIODI (CHIF # 5)
		L ENEW L DOD L
		and an artist of the state of t
	093 * 094 *	! ADDRESS ! ADDRESS !
•		!16
		16 09!08 01! 2ND 4K
	096 * 097 *	
	tor or r	100 0010A 471 40T AV
<u> </u>	w	32 25!24 17! 1ST 4K
	099 *	
	100 *	and and and and and table and
	101 *	
	102 *	SCREEN DISPLAY AND MESSAGES
	103 *	
	104 *	line # 0 - RDWPAT TEST - 8 BIT RAM
	105 *	line # 1 - # LLLL
	106 *	
	107 *	where: line O = diagnostic title
\\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	108 *	LLLL = # of completed loops
	109 *	through diagnostic
/		

	110	*	
	111		ERROR MESSAGES
	112		ERROR MEDDINGED
$I_{ij} = I_{ij}$	113	*	1. FAILURE AT PC'S XXXX BOARD # N
4. 	114	**************************************	(EE/RR) CHIP(S) CC CC CC CC CC CC
	115		TEE/RRY CHIFTS) CO CO CO CO CO CO
	116	*	2. CONFLICT BETWEEN YYYY AND ZZZZ
	117	*	E. ODM ETC. DE MEEN III FRAD 2222
	118	*	3. CH/CL PARITY BIT ERROR PC'S = XXXX
	119	*	were better between the entire to the same to the board to the same entire to
	120	*	where: XXXX = failing PC's
	121	*	N = board # (1,2,3 OR 4)
	122	*	EE = expected pattern
	123	*	RR = actual pattern
	124	*	CC = chip #(s) in error
	125	*	YYYY = TEST CELL address
The second secon	126	*	ZZZZ = CONFLICT CELL addr
(x,y) = (x,y) + (y,y) = (x,y) + (y,y) = (y,y) + (y,y) + (y,y) = (y,y) + (y,y) + (y,y) + (y,y) = (y,y) + (y,y) + (y,y) + (y,y) = (y,y) + (y,y	127	*	do de de de Control V des de Control de de Control de de Control d
	128		DISCUSSION OF ERROR MESSAGES
AMERICAN STREET, AND ADDRESS A	129	*	And the hard hard hard has been the second of the second o
	130	*	ERROR 1 occurs when either the TEST CELL
	131	*	or the CONFLICT CELL failed to maintain it's
And the second s	132	*	expected pattern.
	133	*	
•	134	*	ERROR 2 occurs when the CONFLICT CELL
	135	*	fails to maintain it's expected pattern and
	136	*	the actual pattern equals the TEST PATTERN.
	137	*	This error may indicate an addressing problem.
7	138	*	
	139	*	ERROR 3 occurs when the actual pattern
	140	*	equals the expected, however the hardware
	141	*	detected a parity problem. This error may
	142		indicate a parity bit error.
	143	*	
	144		***** RESET ****
	145	*	When RESET is keyed the program will
	146	*	execute the 'MOUNT SYSTEM DISK' routine
	147	*	located in BOOTSTRAP.
	148	*	
Control of the Contro	149	*	***** HALT/STEP ****
	150	*	The HALT/STEP key may be used to HALT the
	151	*	program. The program will HALT ONLY after an
	152	**************************************	error condition has beed displayed. To resume
	153	*	key HALT/STEP again.
	154	*	
	155	*	***** I/O SUBROUTINES *****
	156	*	This program will use the BOOTSTRAP
	157	*	I/O subroutines whenever possible.
	158	*	Prof. 26.4973 7 7 Prof. 4 Prof. 3 Prof. 3
	159	. Sec.	SYMBL JSMODO2\$
	160	*	n nma.
N. Carlotte and Carlotte	161		B PE24







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	^^~	"T T "T 1
Control of the Contro	002 * E00	TITLE 24 BIT ADDRESSING TEST
	004 *	This diagnostic will read from the end of the
	005 *	program to the end of memory and vica versa
	006 *	searching for a memory location which may have
	007 *	been changed by a previous write instruction.
	008 *	
The second secon	009 *	The algorithm goeslike this -
	010 *	
	011 *	STEP 1. flood memory with SA's (0101 1010)
	012 *	STEP 2. starting at 0200 and searching forward
	013 *	to the end of memory, read each location
	014 *	and check for the SA pattern. If location
	015 *	is okay then write an A5 (1010 0101) at
	016 *	that location.
A	017 *	STEP 3. starting at the end of memory and
	018 *	searching down to location 0200, read
	019 *	each location and check for an A5. If
	020 *	the location is okay then write a 5A
	021 *	(0101 1010) at that location.
	022 *	
-	023 *	MODIFIED REGISTERS:
	024 *	AUX 00 - AUX 07, AUX 11
	025 *	F0 - F7
	026 *	the face to the formal state of the formal sta
	027 *	REGISTER USAGE -
	028 *	F1,FO - end of memory
	029 *	F2 - constant 5A
	~~~~~	F3 - constant A5
and the second s	031 * 032 *	F5,F4 - start of test area (0200)
		F6 - search direction flag
	w	F7 - constant 00
		ANY OF THE PROPERTY.
	" " " " " " " " " " " " " " " " " " "	AUX OO - end of memory
	036 *	AUX 01 - memory pointer
	037 *	AUX 02 - failing memory pointer
		AUX 03 - loop count
	039 * 040 *	AUX O4 - failure pattern (PH,PL) (search) AUX O5 - failure pattern (K) (search)
	041 *	AUX 06 - initial failing pattern (PH,PL)
**************************************	042 *	AUX 07 - initial failing pattern (K)
	043 *	AUX 11 - storage for WCM
	044 *	
Business research control of the con	045 *	***** HALT/STEP ****
	046 *	The program may be interrupted after
	047 *	displaying an error message by keying
	048 *	HALT/STEP. To resume after the program has
	049 *	HALTED key HALT/STEP again.
	050 *	
No. of the Control of	051 *	***** RESET ****
	052 *	When RESET is keyed the program will
	053 *	execute the 'MOUNT SYSTEM PLATTER' routine
A second commence of the second commence of t	054 *	in BOOTSTRAP.
	055 *	
*		

### 24 BIT ADDRESSING TEST

	O!	5€. *	****	I/O SUBROUTINES *****
Control of the contro	057	*	Th	e program uses the BOOTSTRAP I/O
	058	*		s whenever possible.
	059	*		
	060	*	SCREEN	AND ERROR MESSAGES
	061	*		
	062	*		ne #O 24 BIT ADDRESSING TEST
	063	*	lin	ne #1 # LLLL
	064	*		
	065	*		where line #O = TITLE
	066	*		LLLL = # of completed loops
	067	*		
	068	*	ERROR T	YPE O
-	069	*	ERROR BI	ETWEEN XXXX AND YYYY (ZZZZZZ)
	070	*		
	071	*	ERROR T	YPE 1
manufacture and the second of	072	*	POSSIBL	E CHIP FAILURE PC'S = XXXX (ZZZZZZ)
	073	*		
	074	*	wh	ere XXXX = failing memory location
	075	*		YYYY = location causing error
	076	*		ZZZZZZ = XDR (expected/actual)
	077	*		·
•	078	*	DISCUSS	ION OF ERROR TYPES
	079	*		ERROR TYPE O is caused when writing to
	080	*		n YYYY all or part of the pattern is
	081	*		at location XXXX. This is indicative
	082	*	of an a	ddressing problem. However, never rule
	107 1007 1007	. <b>☆</b>	out a c	hip failure.
$\mathcal{F}_{\mathcal{F}}$	084	*		
	085	*	An	ERROR TYPE 1 is caused when the
	086	*	expecte	d pattern is not found and no other
	087	*	location	n seems to cause the problem. This may
	088	*	be a ch	ip or chips error.
	089	*		
	090		SYMBL	JSMOD02\$
	091	*		
	0.35		B	PE24

SYSTEM		ROL MEMORY ADDRESSING TEST	1
VERSION	PREPARED BY J. Sevigr	DATE 12/75	SHEET/OF
Start at 0003	A2	A4	A5
Inhibit Inputs Halt/Stip Off	Set-up Regrit Start Pt Search F	ERS cr. =/ag. Search Memory	B5 Search Memory
ENABLES Enable CRT (Ø5)	Read Memory Locatio	From Low to Hish	Read Memory Location
Display Diagnostia Title	D3 D0 K, PH 4 PL = 5A?	No 2A1	D5 D0  K, Pl+ a PL  = A5?  VES
Zero Loop Count	Write A5  Memory  Location	at	Write 54 at Memory Location
Display Loop Count	The rement  Mevnory  Location	F4	Decrement  Memory  Location
END 24 BIT Find end of Control Memory	G3 - Find cf Memory?	G4	Of Test ARIA?
Initialize Start of Memory Pointer	Setup to Search Mem From High Low	acry to	Increment Loco Count
Flood memory with 5A.	J3 - J3 - B5	J4	Display Loop Count
A3	K2 K3	K4	K5

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PROGRAM Control Memory Addressing Test

PREPARED BY J. Sevigny

CHART _____

SHEET__2__OF_

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**WANG** 

SYSTEM .

**VERSION**_

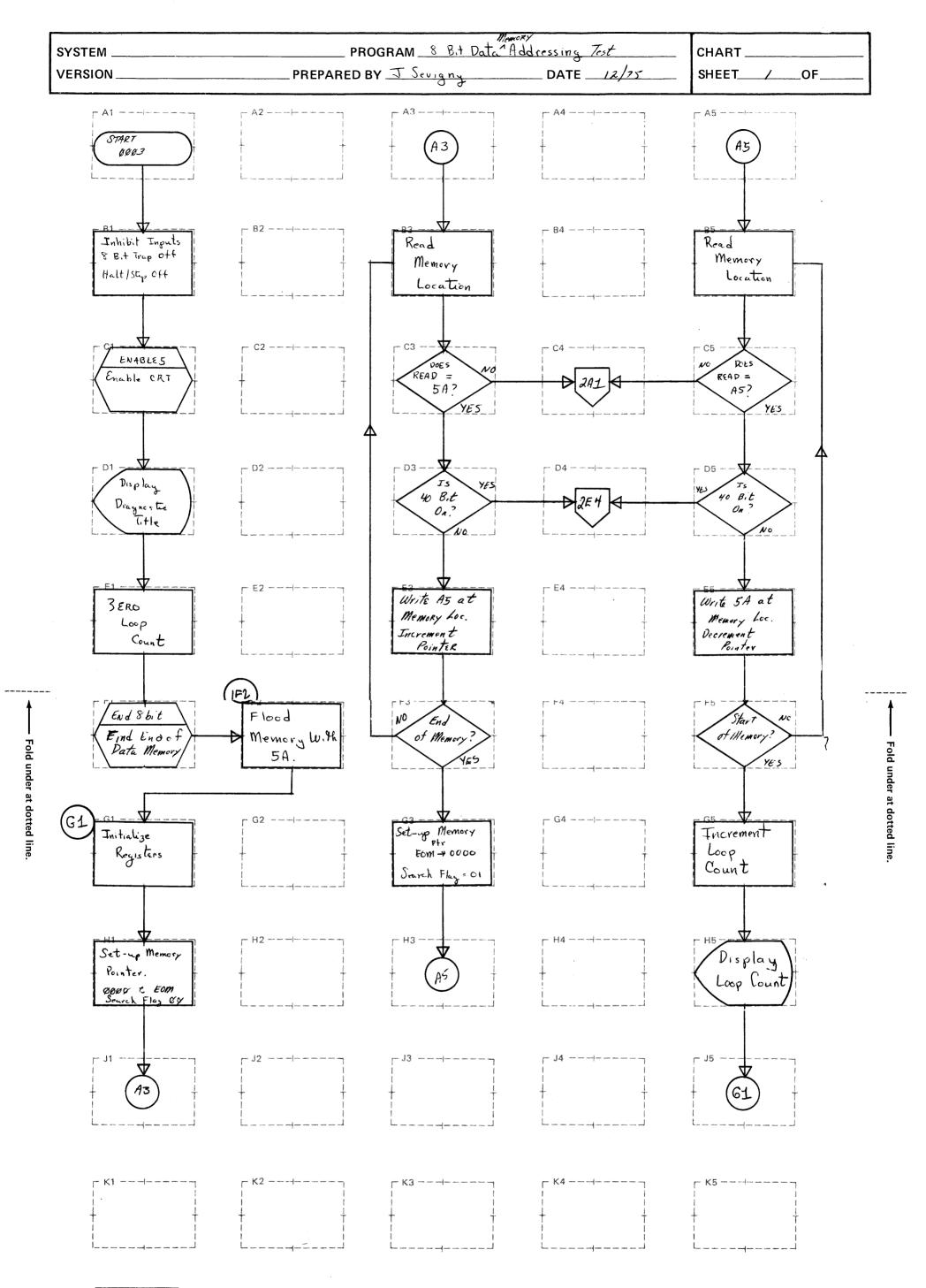
Printed in U.S.A. 700-3186A

1-74-5C Price \$2.50

The second secon	00		TITLE 8 BIT ADDRESSING TEST
	003		8 BIT ADDRESSING TEST
	004		This diagnostic will read from the start of
	005		memory to the end of memory and vica versa
	006		searching for a conflict between two addresses.
	007		
Milder (America) on a modulated consistence of a construction of the construction of t	008		The ACORITHM goes like this -
	009	*	
	010	*	STEP 1. Flood memory with SA's (0101 1010)
	011	*	STEP 2. For each location from the start to
	012	*	the end of memory, read the location,
	013	*	check for a 5A and write an A5 in it's
	014	*	place.
	015	*	STEP 3. For each location from the end to the
	016	*	start of memory, read the location, check
	017		for an A5 and write a 5A in it's place.
	018		
	019		MODIFIED REGISTERS:
Official and the state of the s	020		AUX OO - AUX O3
	021		FO - F7
	022		
	023		REGISTER USAGE -
	024		F1,F0 - end of memory (XFFF)
	025		F2 - constant SA
	026		F3 - constant A5
	027		F5,F4 - start of memory (0000)
	028	*	F6 - search direction flag
	-029		F7 - failing read value
	030		
	031	*	AUX OO - end of memory (XFFF)
	032		AUX O1 - end of memory plus 1 ((X+1)000)
	033	*	AUX O2 - failing memory pointer
	034	*	AUX 03 - loop counter
	035	· · · · · · · · · · · · · · · · · · ·	en e
	036	*	***** HALT/STEP *****
·	037	*	The program may be interrupted by keying
	038	*	HALT/STEP. However, the program will only HALT
		*	after displaying an error condition.
-	040		To resume the program, key HALT/STEP
	041		
	042		
		*	***** RESET ****
	044		When RESET is keyed, the program will
	045	**	execute the 'MOUNT SYSTEM PLATTER' routine
	046	*	located in BOOTSTRAP.
		.5E	<del>na kanala ka</del>
***************************************	047		
	048	*	***** I/O SUBROUTINES *****
	048 049	*	This program uses the BOOTSTRAP I/O
	048 049 <del>05</del> 0	*	
	048 049 050 051	* * * *	This program uses the BOOTSTRAP I/O routines whenever possible.
	048 049 050 051 052	* * * *	This program uses the BOOTSTRAP I/O
	048 049 050 051 052 053	* * * * *	This program uses the BOOTSTRAP I/O routines whenever possible.  SCREEN AND ERROR MESSAGES
	048 049 050 051 052	* * * *	This program uses the BOOTSTRAP I/O routines whenever possible.

### 8 BIT ADDRESSING TEST

The second secon	0	56		
	057	<b>⊹</b> ⊁		where line #O = TITLE
	058	*		LLLL = # of completed loops
And the second s	059			
	060	*	ERROR T	YPE O
	061		ERROR B	ETWEEN XXXX AND YYYY (ZZ)
**************************************	062			
	063	*	ERROR T	
	064		POSSIBL	E CHIP FAILURE PC'S = XXXX (ZZ)
	065			en e
	066	*	ERROR T	
	067	*	CH/CL P	ARITY BIT ERROR PC'S = XXXX
	068		<del>.</del>	
	069	<b>*</b>	wh	ere XXXX = failing memory location
	070	*		YYYY = conflict location
	071			ZZ = XDR (expected/actual)
	072	*		
	073	*		ION OF ERROR TYPES
The state of the s	074			ERROR TYPE O is caused when writing to
	075			n YYYY all or part of the pattern is
	076	*		at location XXXX. This is indicative
Here we have the second of th	077		of an a	ddressing problem.
	078	*		handan kan ban kan kan kan kan
	079			ERROR TYPE 1 is caused when the
A CONTRACTOR OF THE CONTRACTOR	080		•	d pattern is not found and no other
	081	*		n seems to cause the problem. This may
	082	*	be a ba	d memory chip or chips.
į.	- 083		The second secon	
	084	*		ERROR TYPE 2 is caused when the system
	085	*	detecte	d a parity problem but the read value
	086	<b></b>	was as	expected. This may be a parity bit
	087	*	error.	
	088	*		
<del></del>	- 089		SYMBL	JSMCDO2\$
	090	*		
	091		В	PE24
	092		8	MOUNT



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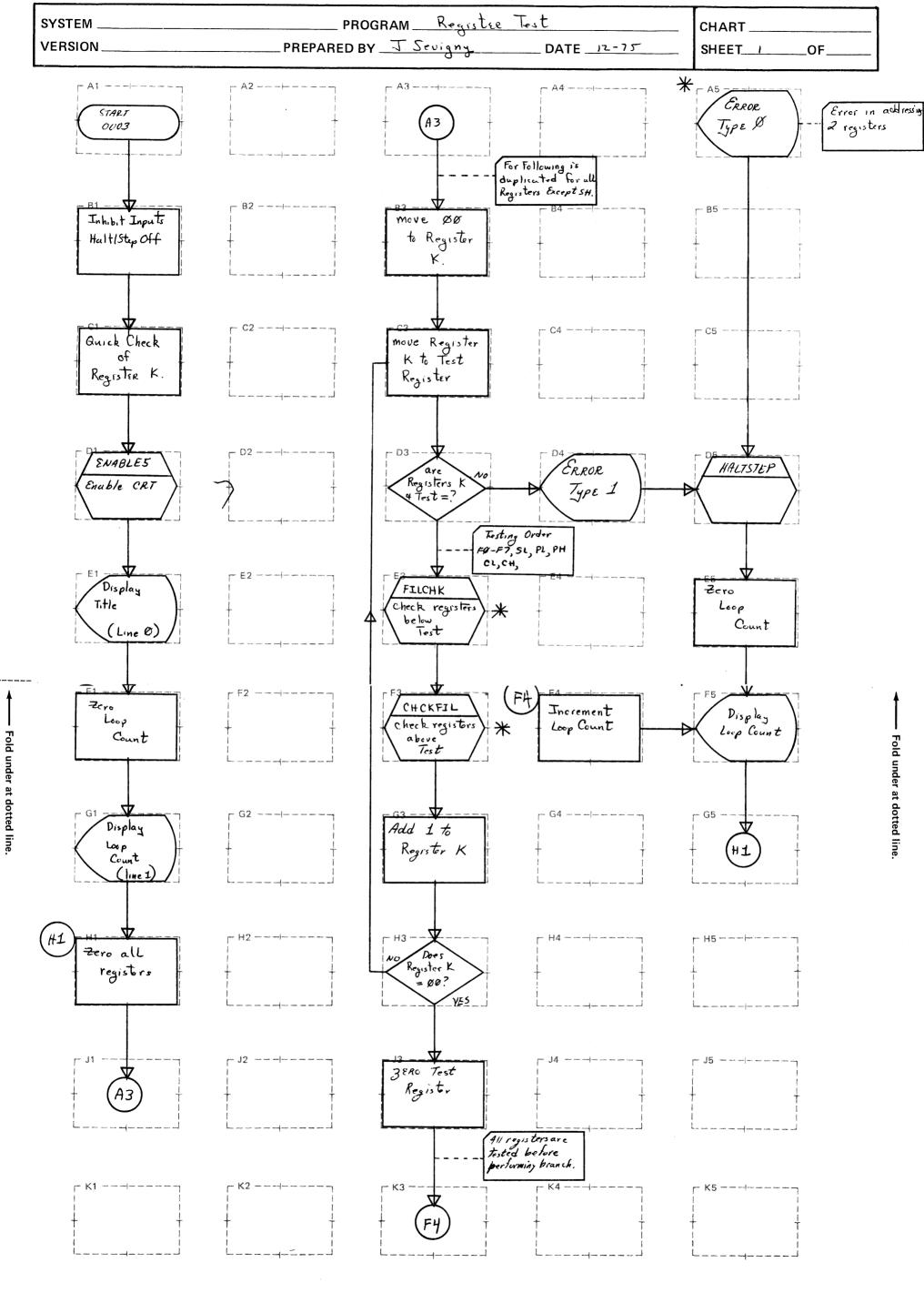
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#### REGISTER TEST

Management of the content of the management of the content of the	003	<b>⊒</b> *	TITL REGTES	
		 **	1/1/2 / 1	This diagnostic was designed to test the
·	005		regi	ster chip in such a manner as to determine
		*		ner bits have gone bad or a conflict in
	007	*		essing exists.
	008	<del></del>		to the second of
	009	*		The test is performed in the following
	010	*	mann	er:
	~ ~ ~	*		and the second of the second o
	for, by pers	<b>*</b>		1. Flood all registers with all zeroes.
		*		2. For each register (FO-F7,CH,CL,PH,PL
		**************************************		"SL AND K) A) move OO to test pattern
		*		B) set test register to test pattern
		*		C) check if test register holds test
		*		pattern.
		*		D) check if other registers have
	020	*		been changed.
	les' from ede	*		E) add Oi to test pattern
	No. President	*		F) repeat steps B through E until
	· ·	*	er en vegen en seren	test pattern equals OO.
	ter have 1	*		G) repeat steps A through F until
	Jan. State Atria.	*		all registers have been tested.
AND THE PROPERTY OF THE PROPERTY OF A STATE OF THE PROPERTY OF		*	MODIFIE	ED REGISTERS:
		*	I Flooring the F. Co. b.	FO-F7, PL, PH, CL, CH, SL AND K
		<b>*</b>		AUX 00, 01
		*		
제국 문의 그들의 일본 사	031	*	POSSIBL	_E PROGRAM HANG-UPS
	032	#	and the second second second second second	- A quick check of register K is made
	per, mee, mee,	*		prior to any displaying being done.
		*		Should 'TESTING REGISTER' fail to appear
Section 1	Im. orn. see.	*		on the CRT then register K is failing
	m,, r	*		which may hinder I/O.
	037	*	<u></u>	A LAS TE SPOTETTO SERVER M.M.
		*	****	HALT/STEP *****
		**		The program may be interrupted by keying HALT/STEP. However, the program
And the second content of the conten	<del>-040</del> - <del>041</del>	<u>*</u>	and the state of t	will HALT only after displaying an error
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	* .		condition.
		*		To resume the program, key HALT/STEP
	044	<u>*</u>		again, a sa s
	045	*		
	046	*	****	RESET *****
	047	4		When RESET is keyed the program will
	048	*		execute the 'MOUNT SYSTEM PLATTER'
	049	*		routine located in BOOTSTRAP.
PARTIES MARTIN PRO SECURIO ANTICOLO CONTRACTOR DE RESPUESTA A LA CASA DE LA CASA DE CA	050	*		T - 2 P'' - P''' 3 31"'' 3"'' 3" 3 31"'' 1" 5 32 32" 1" 5 32 32 32 32 32 32 32 32 32 32 32 32 32
	051	*	***	I/O SUBROUTINES *****
,	052 - <del>053</del>	*		The program uses the BOOTSTRAP I/O
		*	A CONTRACTOR OF THE CONTRACTOR	routines whenever possible.
	***************************************	*	SCREEN	DISPLAYS AND MESSAGES:
en e	**************************************	Committee for the second control of the seco	mar mer t dans bane 1 T	

## REGISTER TEST

Section (1997)		
	057 *	line O - REGISTER TEST
	058 *	line 1 - # LLLL
ACCORDING CONTRACTOR C	059 *	
	060 *	where: line O = Title
	061 *	LLLL = # of completed loops
		through diagnostic
	063 *	
	06.4 *	ERROR TYPE O
<del></del>	065 *	REGISTER XX AND YY ERROR (XX) (CR/LF)
	066 *	
	067 *	ERROR TYPE 1
	<del>06</del> 8	REGISTER XX ERROR (ZZ) (CR/LF)
	O69 *	
	070 *	ERROR DISCUSSION
THE TANKS VERNING PROPERTY AND	07 <del>1</del> *	An ERROR TYPE O is caused when while
	072 *	testing register XX, register YY was found
	073 *	not to contain the expected.
	074 *	ranga kanalangan di katalangan di katalangan di katalangan di katalangan di katalangan di katalangan di katala
	075 *	An ERROR TYPE 1 is caused when
	076 *	register XX fails to hold the test pattern.
	<del></del>	
	078 *	



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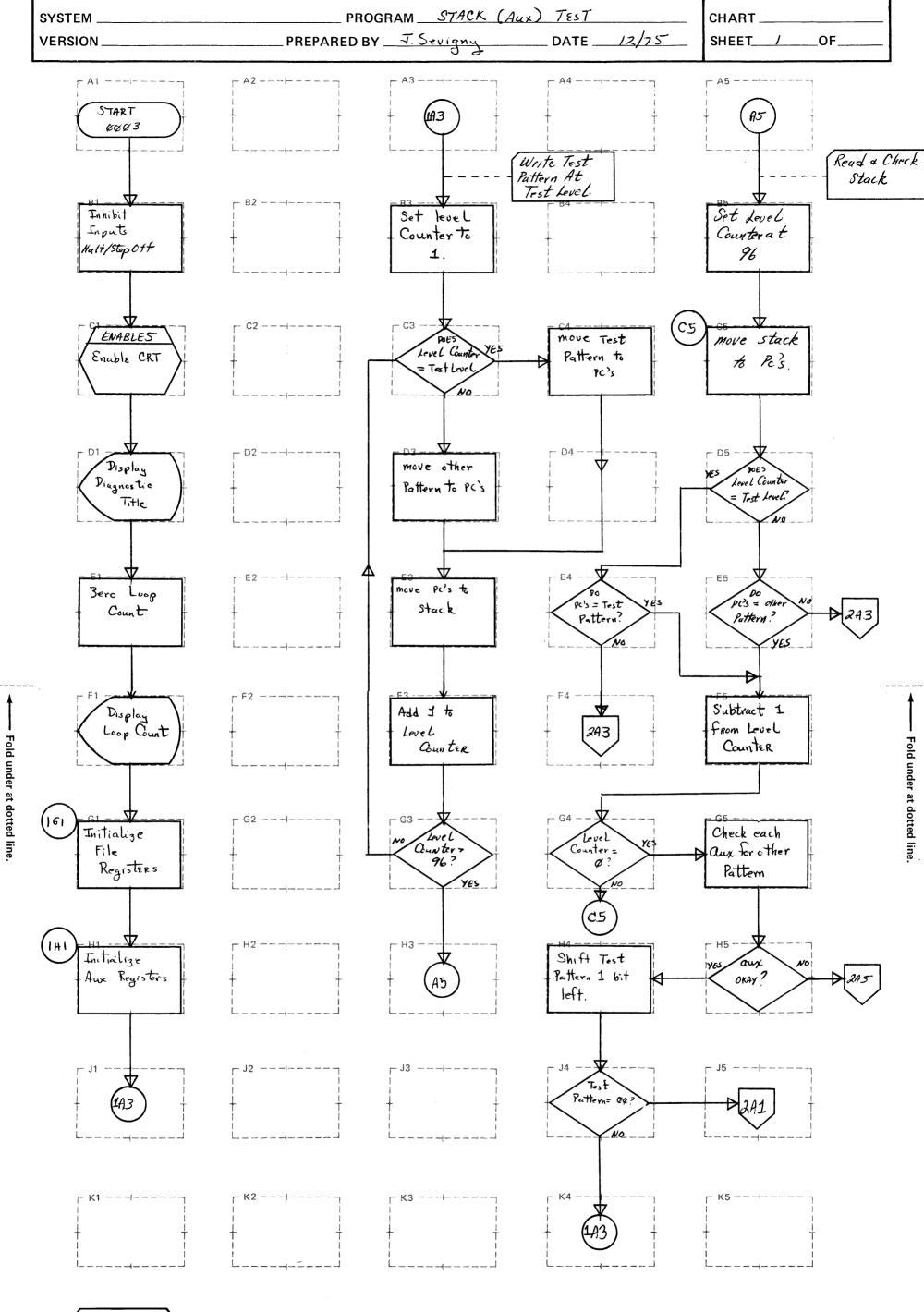
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## STACK / AUXILIARY TEST

The second commences with a residence of the relative entire enti	ÖÖS	TITLE STACK / AUXILIARY TEST
k	003 *	ST/AUX: (STAUX1 AND STAUX2)
	004 *	This routine checks the STACK to determine
The state of the s	005 * 005 *	whether each level in the STACK will -
	les les les	<ul><li>1) hold a particular bit pattern.</li><li>2) have any effect upon another STACK</li></ul>
	007 * 	level.
	002 *	and 3) have any effect on an AUXILIARY
	010 *	register.
Magazia da Magazia da Marakana da Sangga - Namara penggahangan anga angan angangga serias, at panggahan		·····································
	011 * 012 *	Two distinct patterns are used by the
	012 *	routine and these are -
	013 *	1) TEST PATTERN - the pattern which is
	015 *	expected to be at the TEST LEVEL of the STACK.
	016 *	There are 8 TEST PATTERNS -
No seeming the largest contract to the contract of the contrac	<del>017 *</del>	1. 0000 0001 0000 0001
	018 *	2. 0000 0010 0000 0010
	019 *	3. 0000 0100 0000 0100
AND THE RESIDENCE AND THE PROPERTY OF THE PROP		4. 0000 1000 0000 1000
	O21 *	5. 0001 0000 0001 0000
	022 *	6. 0010 0000 0010 0000
The second secon	<del>023 *</del> -	7. 0100 0000 0100 0000
•	024 *	and 8. 1000 0000 1000 0000
	025 *	
	026 *	2) OTHER PATTERN - either all O's or all
	027 *	1's depending the point of execution.
	028 *	
	0 <del>29</del> *	The testing is performed via the following
e di	m, m, m,	ALGORITHM -
	031 * 032 *	PASS 1:  A) The AUXILIARY registers are
Secretary Control of the Control of	033 *	initialized with all O's (OTHER PATTERN)
	034 *	B) The TEST PATTERN is set to (01 01)
	035 *	C) The current TEST PATTERN is
	036 *	written into the current TEST LEVEL of the
	037 *	STACK. While all other levels are written
	038 *	with the OTHER PATTERN.
1	039 *	D) Each level of the STACK is read to
	040 *	determine whether that level holds the
	041 *	expected pattern.
	042 *	E) All of the AUXILIARY registers are
	043 *	checked to determine whether they still
	044 *	
	045 *	F) The next TEST PATTERN is generated
	046 *	and steps B, C and D are repeated.
NAME AND A STATE OF THE PARTY O	047 *	
	048 *	and TEST PATTERN is set to (01 01) and
	049 *	steps B through F are repeated until all
	per, erro, per,	96 STACK levels have been checked.
	051 *	m. a m.m.
	O52 *	PASS 2:
Application of the control of the co	pto, mos, mos,	115 The Aliver TATAL
	054 * 055 *	H) The AUXILIARY registers are set to
	055 *	all 1's (the OTHER PATTERN) and steps B
And the second control of the control of the second control of the	Maria Contraction and Association of Contraction of	

## STACK / AUXILIARY TEST

```
056
                     through G are repeated.
     ¥
057
     뇆
058
               MODIFIED REGISTERS:
                     FO - F7, PL, PH, and K.
059
060
     ж.
061
     4
               REGISTER USAGE:
oe.e
                     FO - TEST PATTERN
     4
063
                     F1 - TEST LEVEL within STACK
064
     4.
                     F2 - level counter
065
                     F3 - max level 96
                     F4 - constant 1
066
                     F5 - constant O
     뀾
067
058
                     F6 - OTHER PATTERN (all O's [OO] or
069
                                 all 1's [FF])
     뇿
070
                     F7 - AUXILIARY register pointer
071
                         - I/O register
072
                      HALT/STEP ****
073
     4
               ****
074
                      The program may be interrupted by
075
               keying HALT/STEP. However, a HALT will be
     ¥
     -3-
076
               executed only after an error message is
077
     4
               displayed.
078
                      To resume executing the program, key
079
     *
               HALT/STEP again.
ORO
081
               상상상상상
                      RESET ****
082
     ييز
                      When RESET is keyed the program will
083
               execute the 'MOUNT SYSTEM PLATTER' routine
084
               located in BOOTSTRAP.
085
     4
086
               ****
                      I/O ROUTINES *****
087
                      The program uses BOOTSTRAP I/O
088
               routine whenever possible.
089
090
               SCREEN DISPLAYS AND MESSAGES
091
092
                     line O - STACK TEST
093
                     line 1 - # LLLL
094
095
                             where LLLL = # of completed loops
098
     4
                                          through diagnostic
097
     ij.
                STACK FAILURE
098
099
     *
                    STACK FAILURE (XXXX)
100
101
                AUXILIARY FAILURE
102
                    AUX YY FAILURE (XXXX)
103
104
     *
                            where XXXX - XOR of the expected
105
     ¥.
                                       and actual.
106
107
                ERROR DISCUSSION
108
                      A STACK FAILURE is when a particular
109
                 STACK LEVEL fails to maintain the expected
```



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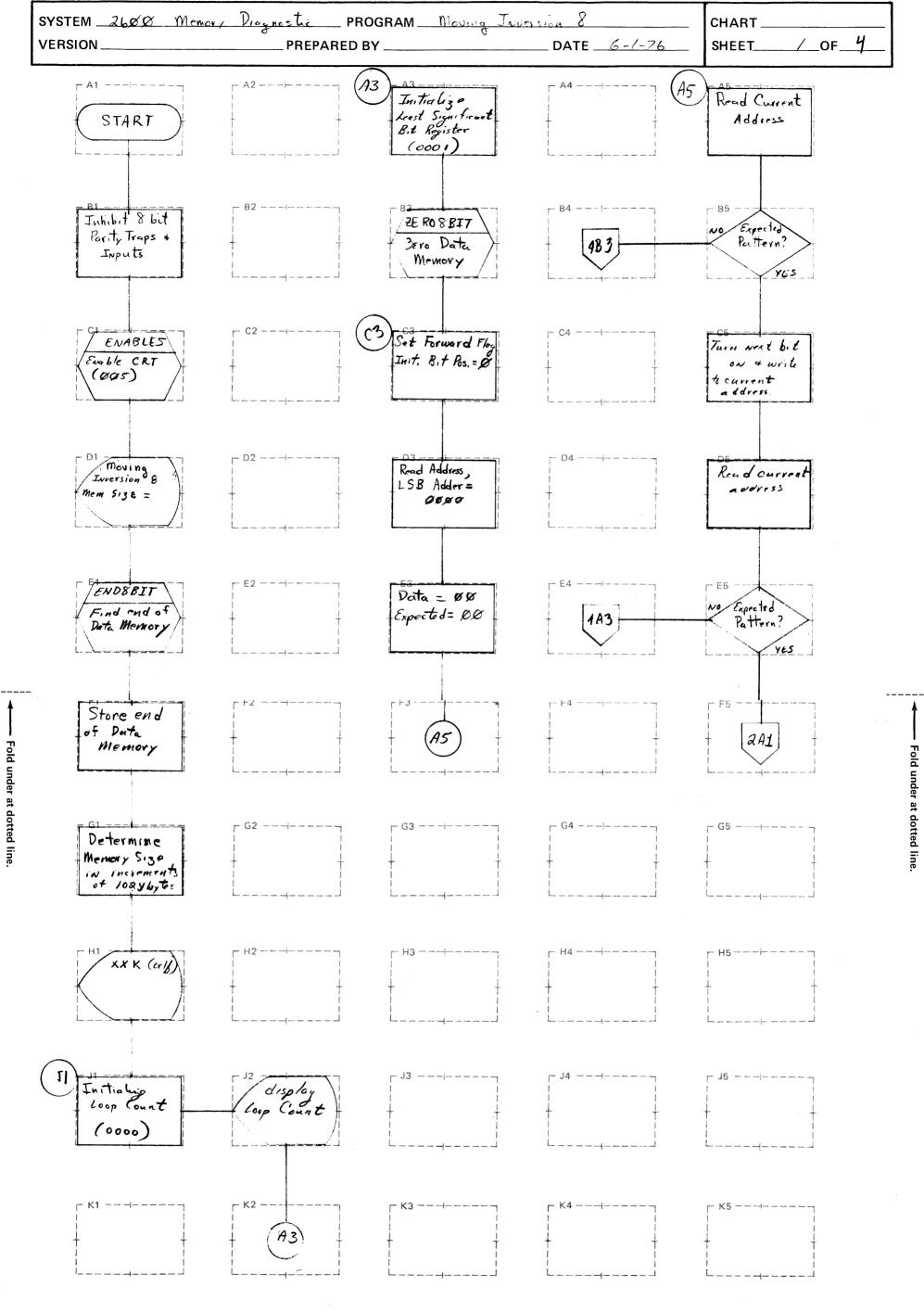
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<b>I</b> (	INVI	ERSI	ON 8	FILE = JSMOVI8 MOVING
		3 4 5	3 * 4 * 5 *	MOVI8  This diagnostic is coded from an article
		6 7 8	6 * 7 * 8 *	in the May 1976 issue of COMPUTER DESIGN entitled 'MOVING INVERSIONS TEST PATTERN IS THOROUGH, YET SPEEDY' by J. Henk de Jonge and Andre J. Smulders.
2		9 10 11	9 * 10 * 11 *	Description "In principle, the MOVI program inverts the
		12 13 14 15	12 * 13 * 14 * 15 *	data of each address sequentially,, thus creating an access time by the jump from one address to another which contains different information."
- ( ' '				

	INVERS	ION 8	<b>3</b>	FILE = JSMOVIA
	17 18 19	17 * 18 * 19 *	AUX	REGISTERS: 00 - 03, SL,F7-F0
	20 21 22 23 24 25	20 * 21 * 22 * 23 * 24 * 25 *	AUX AUX AUX AUX AUX	00 - END OF MEMORY 01 - LOOP COUNT 02 - CURRENT READ ADDRESS 03 - LEAST SIGNIFICANT BIT ADDRESS 04 - CURRENT OFFSET ADDRESS OF LSB ADDR
	26 27 28 29 30 31	26 * 27 * 28 * 29 * 30 * 31 *		SL - FORWARD/REVERSE SEQUENCE F7 - BIT POSITION F6 - EXPECTED DATA F5 - DATA FLAG F0 - WORK
	33 35	32 * 32 *		REMAINING FILE REGISTERS MAY BE USED BY VARIOUS BOOTSTRAP SUBROUTINES.
, .				
	•		·	

	VERS)	35	*					<b>=</b> J:	W
	36 37	36 37	*	MEMORY	BORAD L	AYDUT		•	
 	38	38	*		EVEN		C	)DD	_1
	39 40	40	* 40	00 101		80 P	01	80 1	! SFFF
	41 42		* * 60			80 P	01	80 1	-! P! 7FFF
	43 44		* OO	00 !O:		80 P	01		-! 
	45 46 47		* * 20 *	00 !0: !		80 P	O1	80 1	?! 3FFF
								-	
						,			

	<b>8</b>			FILE = JSMOVI
4 <del>&gt;</del> 50 51	* * e	CREEN D	ISPLAY AND ERRO	DR MESSAGES
52 53 54	# # *	MDV: # LI	ING INVERSION 8 LL	3 - MEM SIZE = XXK
55 56 57	*		WHERE XX - ME LLLL - LC	EMDRY SIZE IN K UNITS DOP COUNT
58 59	* E	RROR DIS	CUSSION	
60 61	*	1. E	RROR PC'S = XX	XX (EE/RR) XOR = YY
62 63	*		WHERE: XXXX =	FAILING ADDRESS
64 65 66	*		RR =	ACTUAL EXCLUSIVE OR
67 68 69	* *	LDCA PATT	I TON PAILS IO	RS WHEN THE CURRENT READ MAINTAIN THE EXPECTED
70 71 -	<b>\</b>	SYMBL	JSMDD02\$	
7. 75		B	* START	
76 77 78		8 8 8	* START *	
79 80		B B	*	
81 82		<u>B</u>	*	
83 84		B B	*	
85		В	*	
86 87		B B		
88		B	*	
89 90	#	B	*	
91		DGRAM EC	NUATES	
93 92	* EOMREG	EQU		
94	LOOPREG	EQU	00 01	END OF MEMORY REGISTER LOOP COUNTER
95	ADDRESS	EGU	05	ADDRESS REGISTER
<del>36</del> 97	LSBADREG '.SBADDER		03 04	LEAST SIGNIFICANT BIT ADDRESS
7				LSB ADDRESS DFFSET
i Ou-	* 511	ART DF D	IAGNOSTIC	
101	START	ORI ANDI	80,SH,SH OFD,SH,SH	INHIBIT 8 BIT PARITY TRAPS INHIBIT INPUTS
103	*	n 10 What is	<u> </u>	TINHTRIL INBULS



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