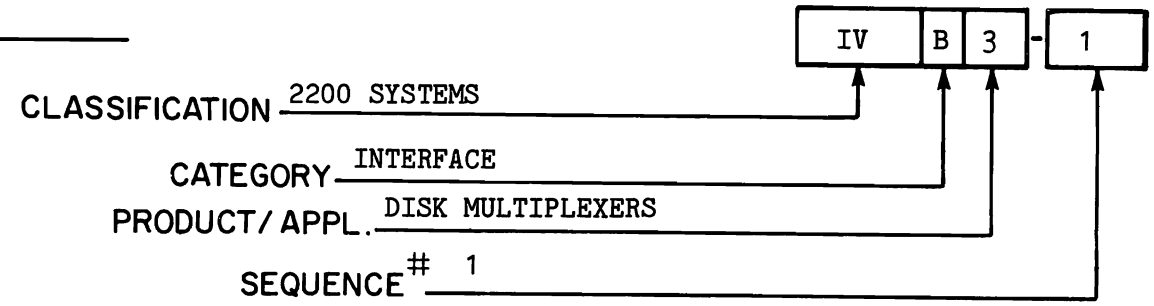
CUSTOMER ENGINEERING

PRODUCT SERVICE NOTICE

DATE: 9/22/80



TITLE:

MODEL 2280 DISK MULTIPLEXER

This PSN contains the following 2280 Disk Multiplexer information.

1. GENERAL DESCRIPTION
2. PHYSICAL CHARACTERISTICS
3. INSTALLATION
4. DIAGNOSTICS
5. TROUBLESHOOTING
6. HARDWARE THEORY OF OPERATION (MAJOR-FUNCTION LEVEL)

Following is a list of documentation categories referenced by this PSN. Documentation from these other categories is required for the performance of certain installation/maintenance tasks.

22C80 Disk Multiplexer Interface -- IV.B.1
2280 DPU-to-2280 DPU/MUX Conversion -- I.B.2
2280 DPU Power Supply Voltage Adjustments -- III.A.7
2280 Disk Diagnostic -- IV.C.1
2200VP BASIC-2 Language Reference Manual, WL# 700-4080 -- IV.C.2

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1. GENERAL DESCRIPTION

The Model 2280 Disk Multiplexer (hereinafter referred to as the 2280MUX) is optionally resident in the 2280 Disk Processing Unit (DPU) and permits two to fifteen 2200VP/LVP/MVP Central Processing Units to share one or two Model 2280 Disk Drives (Phoenix Drive or CDC 9448 Cartridge Module Drive--CMD). Unlike earlier disk multiplexers, which were of the "daisy-chain" type, the 2280MUX is a "star" type multiplexer. In a "star" configuration, the CPU's are individually connected directly to the multiplexer. (See FIGURE 1.)

The 2280MUX allocates disk time to multiple systems in a manner that enables all systems to have virtually concurrent access to the disk. The multiplexer sequentially polls all systems until one of the systems attempts to access the disk. At that point, the multiplexer momentarily ceases polling and passes control of the disk to the inquiring system, which is permitted to execute a single disk statement or command. The multiplexer does not monitor the amount of time required to execute each statement, nor does it limit the number of sectors transferred by a statement. A single statement may read or write only one sector, or may carry out multi-sector transfers. (For example, a MOVE or COPY statement might transfer the contents of an entire disk platter to a second platter; however, major file maintenance operations should be executed only by a system in Hog Mode--see following). When execution of the single disk operation is completed, sequential polling of on-line CPU's resumes from the last requesting CPU.

Some disk operations, such as the on-line updating of a shared common file, require that one system have a period of exclusive, uninterrupted access to the disk. For such operations, the $OPEN statement from the Wang BASIC-2 language should be used (ref: 2200VP BASIC-2 Language Reference Manual, WL# 700-4080, IV.C.2). In this mode of operation, one system temporarily monopolizes or "hogs" the disk, locking out all other systems. Critical file maintenance operations may then be carried out by the privileged system without interruption. After file maintenance has been completed, the $CLOSE statement should be used to release the disk, restoring all CPU's to equal disk-access priority.

2. PHYSICAL CHARACTERISTICS

The 2280MUX consists of the following:

-- A Multiplexer board (WL# 177-2280-X or WL# 210-7717) containing the polling and port- selection circuitry, which interfaces the 2280 Disk Processing Unit (DPU) and up to three CPU's.

-- Up to three Port Expander boards (WL# 177-2280-XE or WL# 210-7718), each of which interfaces up to four additional CPU's.

The 2280MUX circuit boards install directly into a Model 2280 Disk Processing Unit. (A special DPU motherboard (WL# 210-7716) is required. More detailed information follows.)

Each CPU connected to the 2280MUX must have a Model 22C80 I/O controller (WL# 177-2280-C or WL# 210-7715) to interface the 2280MUX.

NOTE:

Refer to documentation category IV.B.1 for information concerning the required 22C80 I/O controller.

For system interconnection, standard 12-foot (3.6-meter) I/O cables (WL# 220-0105-3 220-0138) are supplied with the multiplexer. Extension cables are available, allowing for a maximum distance between CPU and 2280MUX of 1,012 ft (306.7 m). Extension cable lengths and part numbers are as follows:

LENGTH (FEET)	LENGTH (METERS)	WL #
25	7.6	120-2280-01
50	15.2	120-2280-02
100	30.3	120-2280-03
250	75.8	120-2280-04
500	151.5	120-2280-05
750	227.3	120-2280-06
1000	303.0	120-2280-07

A 15-inch (37.5-cm) cable (WL# 220-0257) is also provided for connecting the Multiplexer board (WL# 210-7717) to the ALU/MUX board (WL# 210-7421-A) in the DPU.

FIGURE 1 below illustrates a typical four-system, dual-drive configuration. Two unused (not required) Port Expander boards are also shown in the figure.

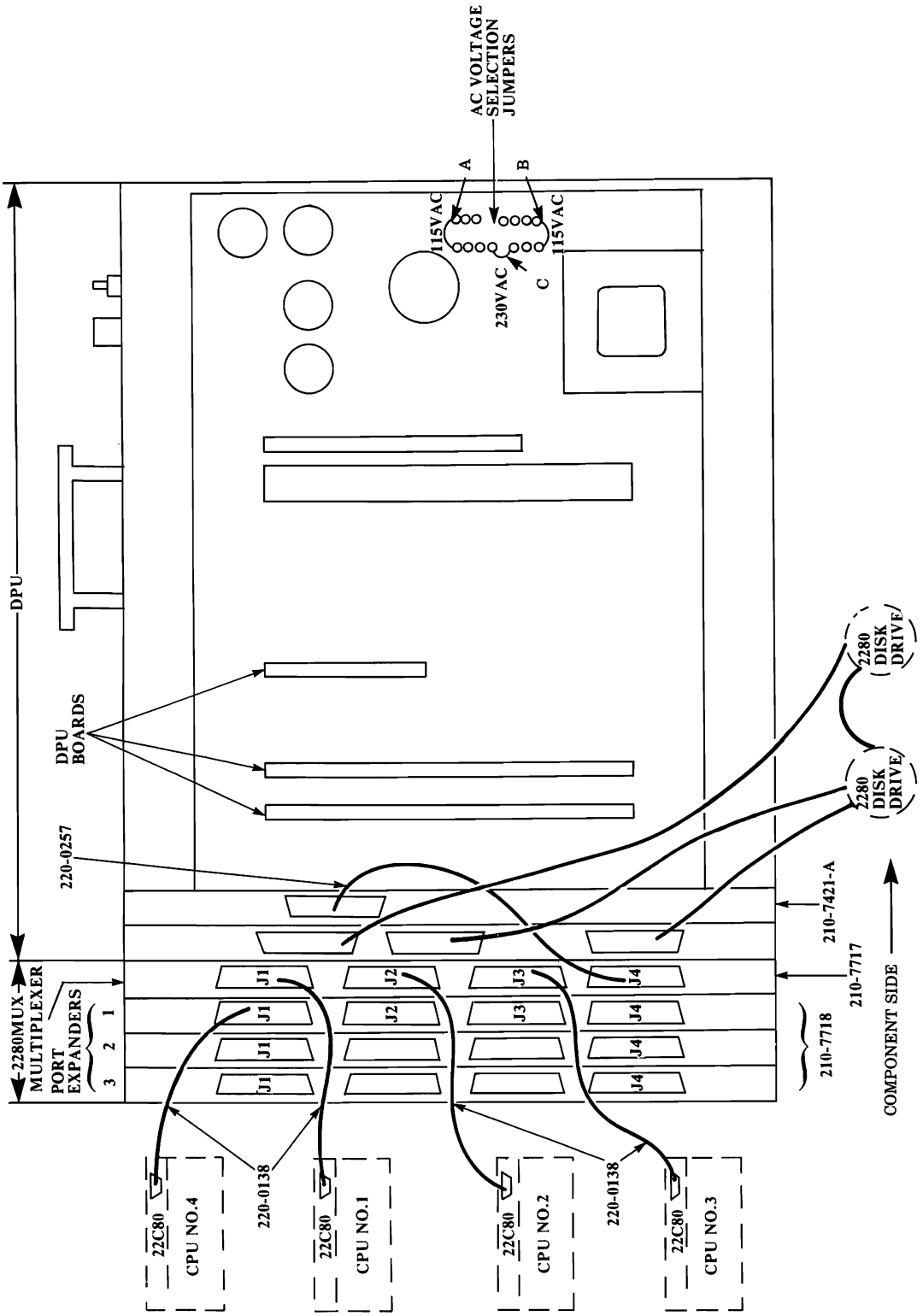


FIGURE 1 2280 DPU/MUX SYSTEM CONFIGURATION AND BOARD LAYOUT

3. INSTALLATION

NOTE:
Be sure to power-off the 2280 DPU/MUX before performing any installation procedure.

3.1 MOTHERBOARD REQUIREMENTS

The 2280MUX requires that a WL# 210-7716 motherboard be resident in the 2280 Disk Processing Unit (DPU). Model 2280 DPU's sold with the MUX have a WL# 210-7716 motherboard. All newly manufactured 2280 DPU's also have this motherboard installed, providing for easier installation of a MUX upgrade.

If an older-version 2280 DPU is to be upgraded to add multiplex capabilities, the entire 2280 DPU chassis must be replaced with the newer-version chassis (WL# 270-0688-60 for 60 Hz, or WL# 270-0688-50 for 50 Hz), containing a WL# 210-7716 motherboard.

Refer to documentation category I.B.2 for detailed conversion procedures, and then continue with Section 3.2 of this installation procedure.

3.2 MOTHERBOARD AC INPUT VOLTAGE SELECTION JUMPERS

Jumper wires are provided on the WL# 210-7716 motherboard for ac input voltage (115V or 230V) selection. Two jumpers are installed for 115VAC and one jumper for 230VAC. FIGURE 1 shows the positions of these jumpers. Be certain the jumper configuration is correct for the supplied ac voltage (see following chart).

VOLTAGE SELECTION JUMPERS

	115VAC	230VAC
JUMPER A	IN	OUT
JUMPER B	IN	OUT
JUMPER C	OUT	IN

3.3 MOTHERBOARD/PCB LAYOUT

The locations of the 2280MUX circuit boards in relation to the motherboard/chassis are shown in FIGURE 1. Ensure that all fingerboard connectors are clean prior to installing the boards in the DPU. (An ink eraser should be used to clean the pins if necessary.)

After installing the 2280MUX circuit boards, be certain to recheck and adjust, if necessary, DPU power supply voltages +5V and -12V. Refer to Wang Cartridge Module Disk Drive Field Level Maintenance Manual Addendum One, CE #03-0080-A (III.A.7), for 2280 DPU voltage adjustment procedures.

3.4 SYSTEM INTERCONNECTION

Refer to FIGURES 1, 2, 3, and the following table when interconnecting CPU's and 2280MUX.

TABLE 1 2280MUX SYSTEM CABLE CONNECTIONS

CABLE #	FROM	TO
220-0138	210-7717 Multiplexer--J1	CPU #1--22C80
220-0138	210-7717 Multiplexer--J2	CPU #2--22C80
220-0138	210-7717 Multiplexer--J3	CPU #3--22C80
220-0138	210-7718 Port Expander #1--J1	CPU #4--22C80
220-0138	210-7718 Port Expander #1--J2	CPU #5--22C80
220-0138	210-7718 Port Expander #1--J3	CPU #6--22C80
220-0138	210-7718 Port Expander #1--J4	CPU #7--22C80
220-0138	210-7718 Port Expander #2--J1	CPU #8--22C80
.		
.		
220-0138	210-7718 Port Expander #3--J4	CPU #15--22C80
220-0257	210-7717 Multiplexer--J4	210-7421-A (in DPU)

4. DIAGNOSTICS

Up to the date of this publication, diagnostics designed to test all 2280MUX functions had not been completed. It is possible to test a majority of the 2280MUX functions with the standard 2280 Disk Diagnostic (WL# 701-2555). This is accomplished by running the diagnostic at several (a predetermined number) CPU's at the same time, with each CPU addressing a different disk surface (one surface only) in the drive. The predetermined number of CPU's at which the diagnostic can be run is equal to the number of data surfaces present in the drive under test (that is, 2280-1: two surfaces; 2280-2: four surfaces; 2280-3: six surfaces).

Refer to documentation category IV.C.1 for detailed information concerning the standard 2280 Disk Diagnostic.

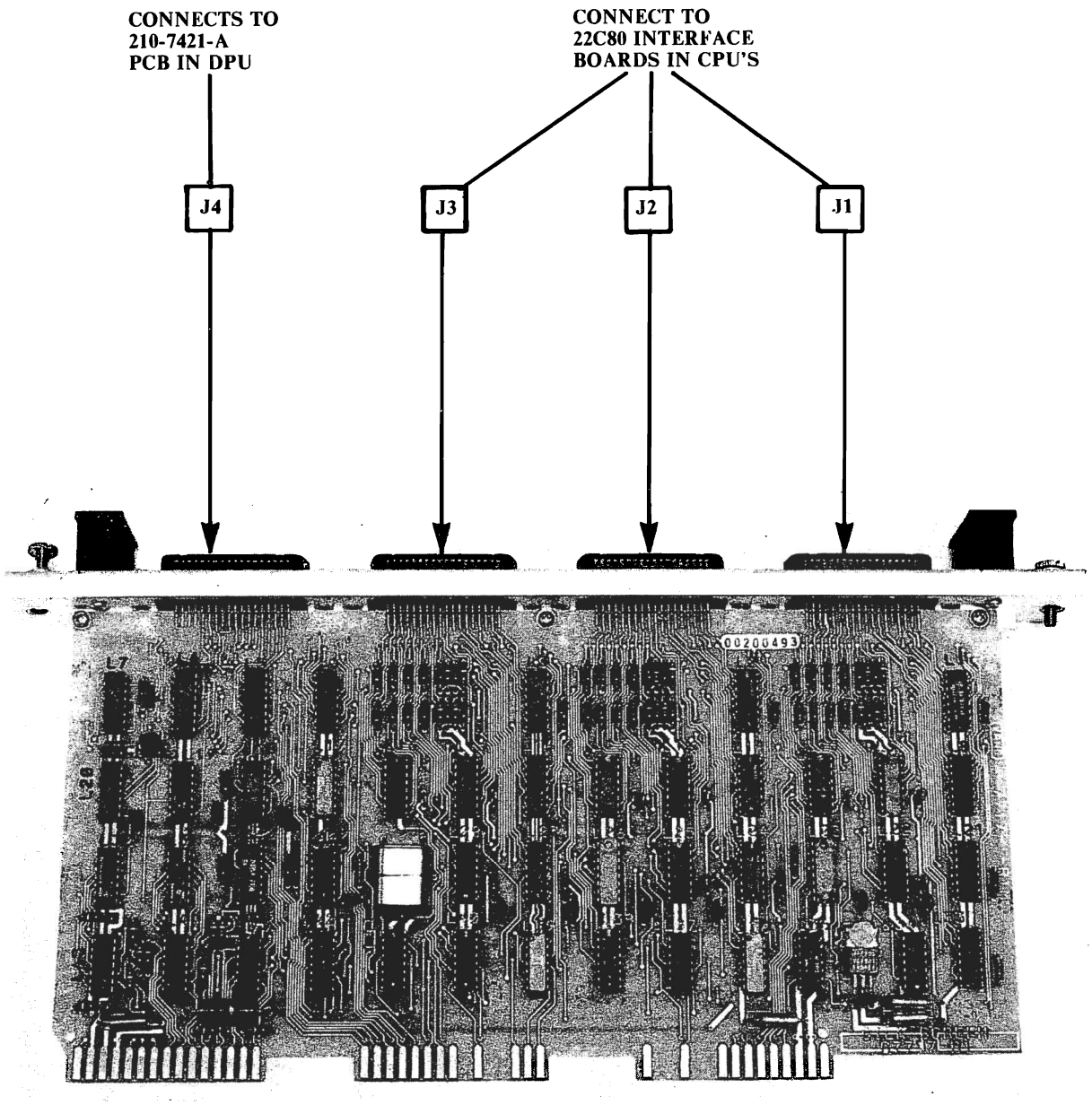


FIGURE 2 WL NO. 210-7717 MULTIPLEXER BOARD

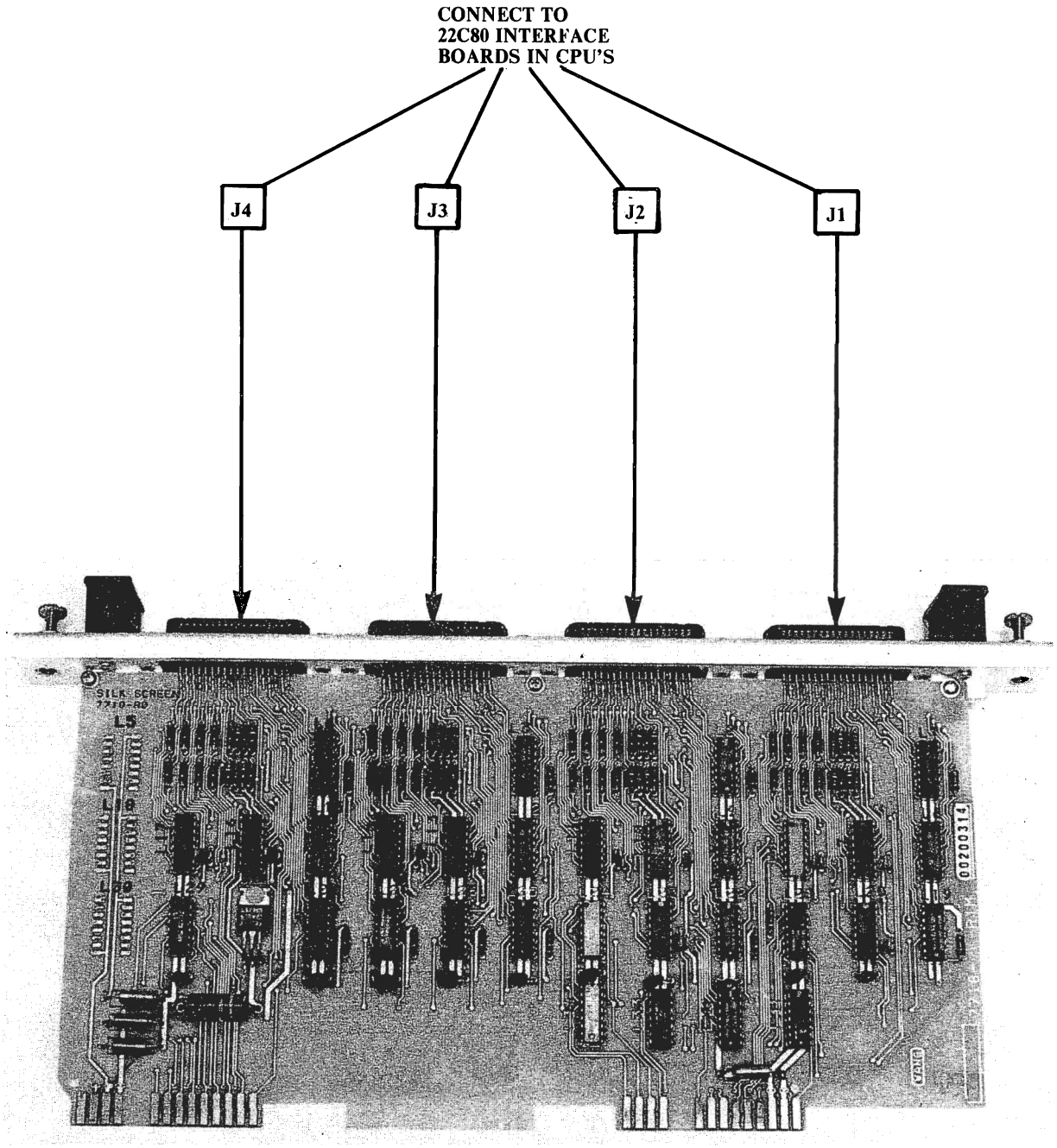


FIGURE 3 WL NO. 210-7718 PORT EXPANDER BOARD

5. TROUBLESHOOTING

If only one channel of a 2280MUX system fails (I/O error indication), it is possible to isolate the cause of the failure by interchanging the I/O cables at the Port Expander board or Multiplexer board (as applicable) in the 2280 DPU/MUX. If, after swapping CPU-to-MUX cables, the problem remains with the same 2280MUX channel, conclude that the Port Expander/Multiplexer is defective; if the problem moves with the suspected 2200 CPU to the different 2280MUX channel, conclude that the 2200 CPU is defective--the most likely cause being the 22C80 I/O controller.

If all channels fail, the 2280 DPU, the DPU/MUX power supply, the 2280MUX multiplexer board, the disk cables, or the 2280 disk itself may be defective.

6. HARDWARE THEORY OF OPERATION (MAJOR-FUNCTION LEVEL)

Port Expander Board (WL #210-7718) (ref: FIGURE 4 and MNEMONICS)

Port Selector--

Decodes the port-select signals ($\overline{S0\text{-}1}$), received from the Multiplexer board, into port-select signals $\overline{P_{1-4}}$. These signals enable one of four CPU I/O ports on the Port Expander board.

Reset Mux--

Selects the appropriate Reset pulse (RESET1-4), received from the CPU's, for output to the Multiplexer board as $\overline{ICAPM}$. The Reset pulse is used to initialize the DPU, the MUX, and the disk drive.

Request Latch--

Selects the appropriate Request signal (REQ_{1-4}), received from the CPU's, for output to the Multiplexer board as RQ_{1-4}. The Request line informs the DPU that a CPU requires disk access.

Input Bus Mux--

Receives the read data (IB_{1-8}) that is to be sent to the CPU. During the first half of the Input Data Strobe (IDS), the low order bits (IB_{1-4}) are selected through the Input Bus Mux as Input Data bits ID1-ID4. During the second half of the IDS, the high order bits (IB_{5-8}) are selected through the multiplexer. The Input Data bits are sent to the CPU's, via the 22C80 I/O controller.

Level Converters (Line Receivers/Drivers)--

Convert differential voltage levels (Emitter Coupled Logic--ECL--levels) received from the CPU's (22C80) to the TTL levels required by the Multiplexer board. Convert TTL voltage levels received from the Multiplexer board to the differential driving levels required by the CPU's (22C80). Use of ECL in this application allows each CPU disk I/O logic to operate at optimum speed even with the greater distance from CPU to multiplexer, as compared to the driver/receiver distances possible with TTL.

PORT EXPANDER SIGNAL MNEMONICS

$\overline{ACK_{1-4}}$ (Acknowledge):

Acknowledgement of CPU request for disk use -- from MUX (210-7717)

ACK (Acknowledge):

Acknowledgement of CPU request for disk use -- to CPU's (22C80)

CLK (Clock):

Clocks Request Latch -- from MUX (210-7717)

CPB (Central Processor Busy):

CPU ready/busy status -- from CPU's (22C80)

$\overline{CPB}$ (Central Processor Busy):

CPU ready/busy status -- to MUX (210-7717)

DN3 (Disk Number 3):

Indicates access to second drive is required -- from CPU's (22C80)

$\overline{\text{DN3}}$ (Disk Number 3):

Indicates access to second drive is required -- to MUX (210-7717)

DOD1-DOD4 (Data Out to Disk):

Write data to be sent to disk -- to MUX (210-7717)

DRB (Disk Ready/Busy):

Disk ready/busy status -- to CPU's (22C80)

DS (Data Select):

Selects IB_{1-4} or IB_{5-8} for output -- from MUX (210-7717)

IB_{1-8} (Input Bus):

Read data to be sent to CPU's -- from MUX (210-7717)

$\overline{\text{ICAPM}}$ (Input Calculator Prime):

Resets DPU and disk -- to MUX (210-7717)

ID1-ID4 (Input Data):

Read data to be sent to CPU's -- to CPU's (22C80)

IDS (Input Data Strobe):

Strobes read data from disk to CPU's -- to CPU's (22C80)

IOB1 (Input/Output Bit 1):

Parity bit for write data to be sent to disk -- from CPU's (22C80)

$\overline{\text{IOB1}}$ (Input/Output Bit 1):

Parity bit for write data to be sent to disk -- to MUX (210-7717)

OBS (Output Bus Strobe):

Strobes write data from CPU's to disk -- from CPU's (22C80)

$\overline{\text{OBS}}$ (Output Bus Strobe):

Strobes write data from CPU's to disk -- to MUX (210-7717)

OD1-OD4 (Output Data):

Write data to be sent to disk -- from CPU's (22C80)

$\overline{P_{1-4}}$ (Port):

Select appropriate CPU port circuitry -- internal

RB (Ready/Busy):

Disk ready/busy status -- from MUX (210-7717)

REQ_{1-4} (Request):

Request by CPU for disk use -- from CPU's (22C80)

$\overline{RESET}_{1-4}$:

Reset DPU and disk -- from CPU's (22C80)

RQ_{1-4} (Request):

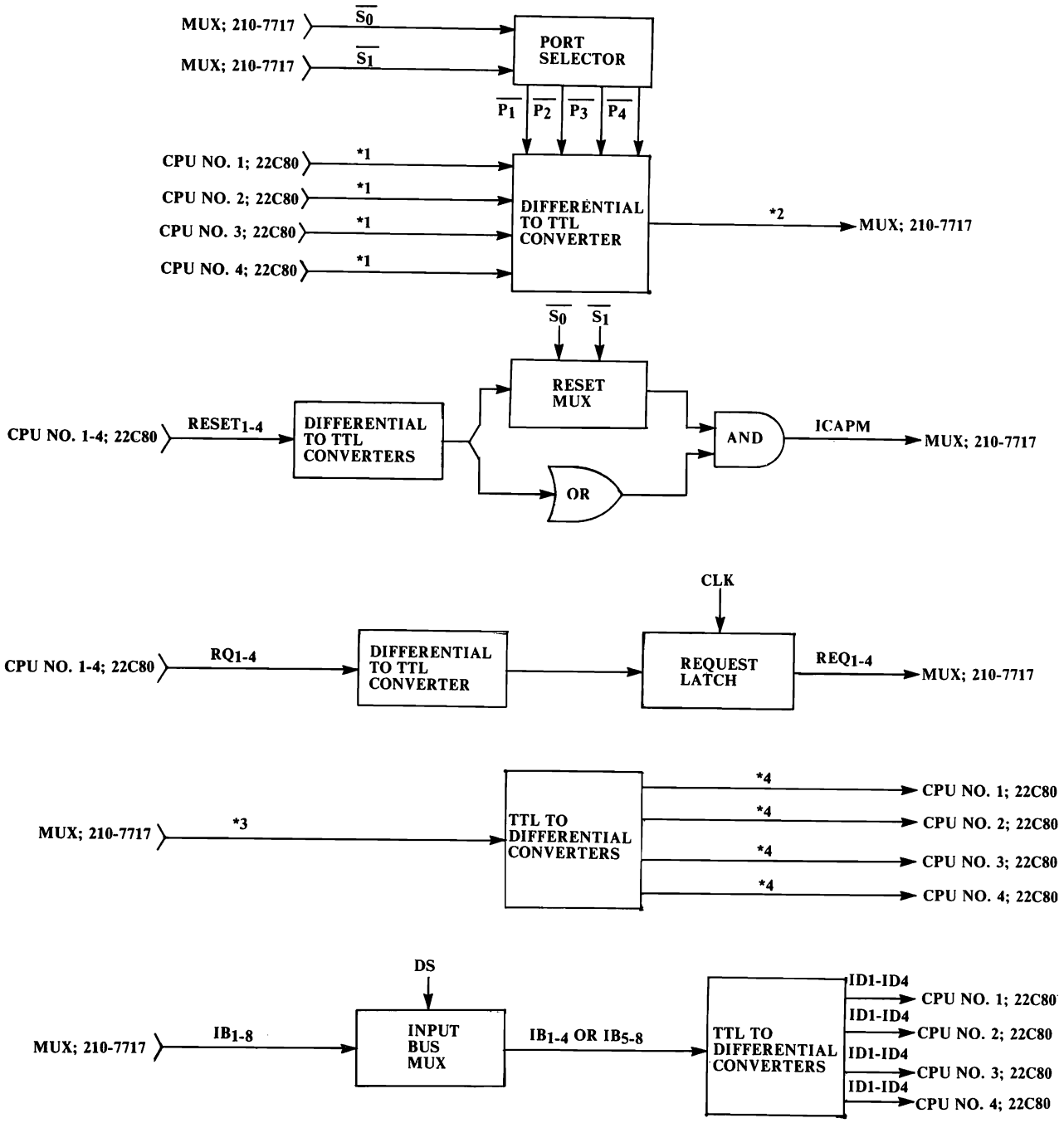
Request by CPU for disk use -- to MUX (210-7717)

$\overline{S_{0-1}}$ (Select):

Decoded into port select signals -- from MUX (210-7717)

$\overline{STR}$ (Strobe):

Strobes read data from disk to CPU's -- from MUX (210-7717)



*1 – OD1-OD4, IOB1, DN3, CPB, OBS
*2 – DOD1-DOD4, $\overline{IOB1}$, $\overline{DN3}$, $\overline{CPB}$, $\overline{OBS}$
*3 – RB, $\overline{STR}$, $\overline{ACK}_{1-4}$
*4 – DRB, IDS, ACK

FIGURE 4 PORT EXPANDER BLOCK DIAGRAM

Multiplexer Board (WL #210-7717) (ref: FIGURE 5 and MNEMONICS)

Output Data Latch--

Receives the write data (DOD1-DOD4) that is to be sent to (written on) the disk. During the first half of the Output Bus Strobe ($\overline{OBS}$), the data-out bits are clocked through the Output Data Latch as KS0-KS3. During the second half of OBS, the data-out bits are clocked through the latch as KS4-KS7. The KS bits are sent to the disk via the DPU.

Reset Mux--

Selects the appropriate (desired) Reset pulse (RESET1-RESET3) received from the CPU's for output to the DPU as $\overline{ICAPM}$. The Reset pulse is used to initialize the DPU and disk drive.

Request Latch--

Selects the appropriate (desired) Request signal (REQ1-REQ3) received from the CPU's. The Request line informs the DPU that a CPU requires disk access.

Polling Circuit--

Scans the CPU request lines ($RQ1\text{-}4_{1\text{-}4}$) to determine whether disk access is desired. When a request is received, the multiplexer sends an acknowledge signal ($\overline{ACK1\text{-}4_{1\text{-}4}}$) to the requesting CPU, and the polling sequence is momentarily halted until that CPU completes its disk operation. Polling resumes with the next sequential channel. RESET initializes the polling circuit to a count of one (channel #1 of the WL# 210-7717 Multiplexer board).

Clock--

Increments the CPU polling circuit.

Decode Control Circuit--

Monitors the acknowledge signals ($\overline{ACK1\text{-}4_{1\text{-}4}}$), and decodes these signals

into the appropriate Board Select (BS1-BS4), Port Select (P1-P3), and Select (S0-S1) signals.

Port Selector--

Decodes the port-select signals ($\overline{S0}$-$\overline{S1}$) into port-select signals $\overline{P1}$-$\overline{P3}$. These signals enable the port circuitry for the CPU requiring disk access.

CPU Ready/Busy Latch--

Provides the DPU with the CPU ready/busy status.

Input Bus Strobe Latch--

Receives the Input Bus Strobe from the DPU, and retransmits the strobe to each CPU at the appropriate time.

Input Bus Mux--

Receives the read data (IB1-IB8) that is to be sent to the CPU. During the first half of the Input Bus Strobe ($\overline{IBS}$), the low order bits (IB1-IB4) are selected through the Input Bus Mux as Input Data bits ID1-ID4. During the second half of the IBS, the high order bits (IB5-IB8) are selected through the multiplexer. The Input Data bits are sent to the CPU's via the 22C80 I/O controller.

Level Converters (Line Receivers/Drivers)--

Convert differential voltage levels (Emitter Coupled Logic--ECL--levels) received from the CPU's (22C80) to the TTL levels required by the Multiplexer board. Convert TTL voltage levels received from the Multiplexer board to the differential driving levels required by the CPU's (22C80). Use of ECL in this application allows each CPU disk I/O logic to operate at optimum speed even with the greater distance from CPU to multiplexer, as compared to the driver/receiver distances possible with TTL.

MULTIPLEXER SIGNAL MNEMONICS

$\overline{ACK1}_{1-3}$ (Acknowledge):

Acknowledgement of CPU request for disk use -- internal

$\overline{ACK2\text{-}4}_{1-4}$ (Acknowledge):

Acknowledgement of CPU request for disk use -- to Port Expanders (210-7718)

ACK (Acknowledge):

Acknowledgement of CPU request for disk use -- to CPU's (22C80)

$\overline{BS2}$-$\overline{BS4}$ (Board Select):

Selects the appropriate Port Expander -- to Port Expanders (210-7718)

CLK (Clock):

Clocks Request Latch -- internal

CPB (Central Processor Busy):

CPU ready/busy status -- from CPU's (22C80)

$\overline{CPB}$ (Central Processor Busy):

CPU ready/busy status -- to DPU (210-7421-A)

DN3 (Disk Number 3):

Indicates access to second drive is required -- from CPU's (22C80)

$\overline{DN3}$ (Disk Number 3):

Indicates access to second drive is required -- to DPU (210-7421-A)

DOD1-DOD4 (Data Out to Disk):

Write data to be sent to disk -- internal

DRB (Disk Ready/Busy):

Disk ready/busy status -- to CPU's (22C80)

DS (Data Select):

Selects IB1-IB4 or IB5-IB8 for output -- internal

$\overline{GISO}$:

Strobes write data from CPU's to disk -- to DPU (210-7421-A)

GKBD:

CPU ready/busy status -- to DPU (210-7421-A)

$\overline{\text{IBS}}$ (Input Bus Strobe):

Strobes read data from disk to CPU's -- from DPU (210-7421-A)

IB1-IB8 (Input Bus):

Read data to be sent to CPU's -- from DPU (210-7421-A)

$\overline{\text{ICAPM}}$ (Input Calculator Prime):

Resets DPU and disk -- to DPU (210-7421-A)

ID1-ID4 (Input Data):

Read data to be sent to CPU's -- to CPU's (22C80)

IDS (Input Data Strobe):

Strobes read data from disk to CPU's -- to CPU's (22C80)

IOB1 (Input/Output Bit 1):

Parity bit for write data to be sent to disk -- from CPU's (22C80)

$\overline{\text{IOB1}}$ (Input/Output Bit 1):

Parity bit for write data to be sent to disk -- to DPU (210-7421-A)

KS0-KS7:

Write data to be sent to disk -- to DPU (210-7421-A)

$\overline{\text{OBS}}$ (Output Bus Strobe):

Strobes write data from CPU's to disk -- from Port Expanders (210-7718)

OD1-OD4 (Output Data):

Write data to be sent to disk -- from CPU's (22C80)

ODS (Output Data Strobe):

Strobes write data from CPU's to disk -- from CPU's (22C80)

$\overline{\text{P1}}$-$\overline{\text{P3}}$ (Port):

Select appropriate CPU port circuitry -- internal

RB (Ready/Busy):

Disk ready/busy status -- from DPU (210-7421-A)

REQ1-REQ3 (Request):

Request by CPU for disk use -- from CPU's (22C80)

RESET1-RESET3:

Reset DPU and disk -- from CPU's (22C80)

$RQ1_{1-3}$ (Request):

Request by CPU for disk use -- internal

$RQ2\text{-}4_{1-4}$ (Request):

Request by CPU for disk use -- from Port Expanders (210-7718)

S0-S1 (Select):

Decoded into port select signals -- internal

$\overline{STR}$ (Strobe):

Strobes read data from disk to CPU's -- to Port Expanders (210-7718)

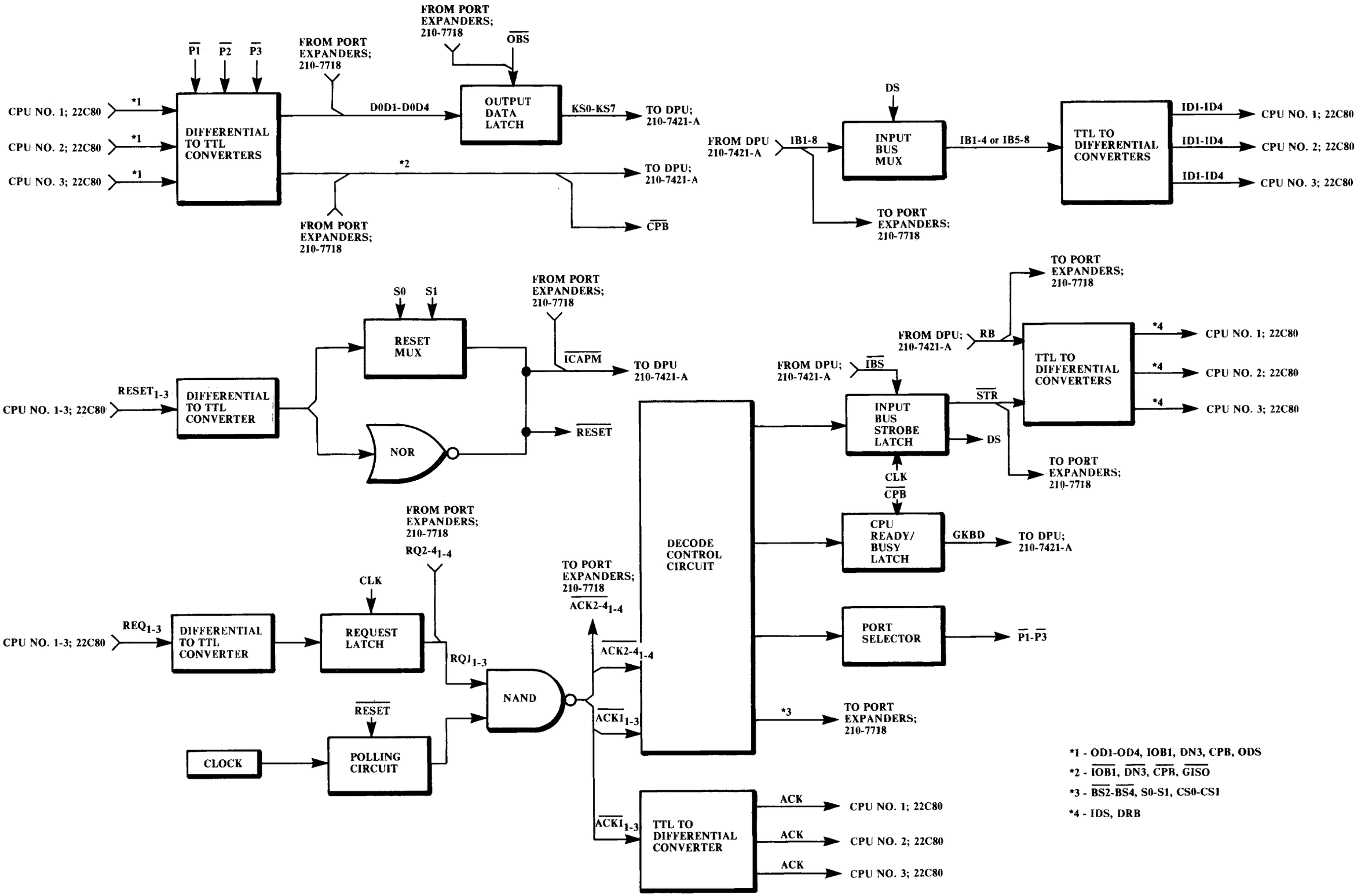
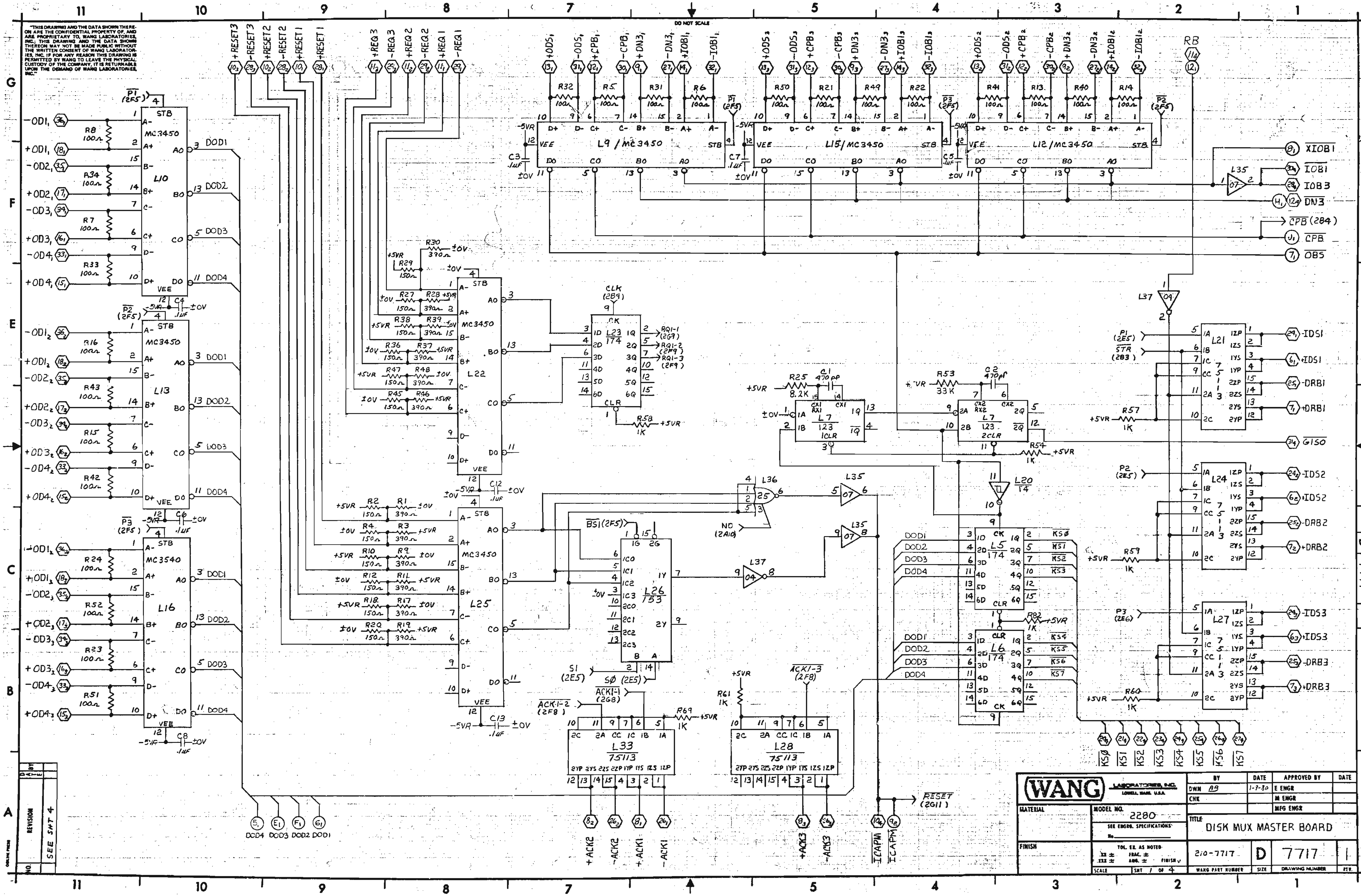


FIGURE 5 WL. NO. 210-7717 MULTIPLEXER BLOCK DIAGRAM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L13 MC3450
L16 MC3540
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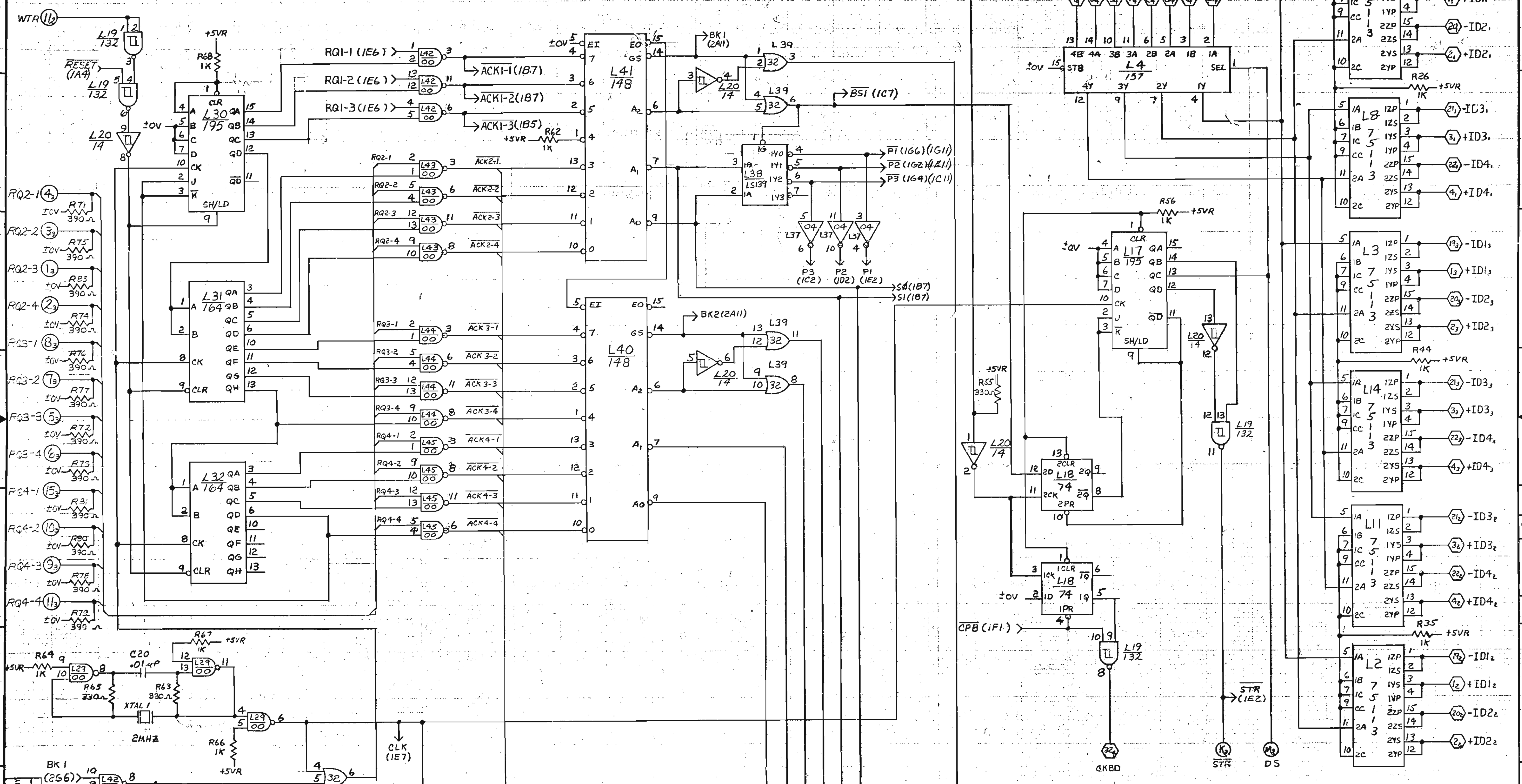
L25 MC3450
L9 / MC3450
L15 / MC3450
L12 / MC3450
L23 174
L26 153
L5 174
L6 174
L7 123
L33 75113
L28 75113
L21
L24
L27
L35
L36
L37
L20
XIOB1
IOB1
IOB3
DN3
CPB (2B4)
CPB
OBS
GISO
-IDS1
+IDS1
-DRB1
+DRB1
-IDS2
+IDS2
-DRB2
+DRB2
-IDS3
+IDS3
-DRB3
+DRB3
KS0 KS1 KS2 KS3 KS4 KS5 KS6 KS7
RESET (2G11)
DOD4 DOD3 DOD2 DOD1
+ACK2 -ACK2 +ACK1 -ACK1 +ACK3 -ACK3
ICAPM ICAPM
REVISION
SEE SHT 4
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
MODEL NO. 2280
SEE ENGRG. SPECIFICATIONS
DWN AB 1-7-80
E ENGR
M ENGR
MFG ENGR
TITLE DISK MUX MASTER BOARD
210-7717
D 7717
SHT 1 OF 4

DO NOT SCALE



WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY / DATE
MATERIAL	MODEL NO. 2280	DWN A.B	1-9-80	E ENGR
	SEE ENGRG. SPECIFICATIONS No.	CHK		M ENGR
				MFG ENGR
		TITLE DISK MUX MASTER BOARD		
FINISH	TOL. EX. AS NOTED .XX ± FRAC. ± .XXX ± ANG. ± FINISH ✓	210-7717 (WANG PART NUMBER)	D (SIZE)	7717 (DRAWING NUMBER) REV. 1
	SCALE / SHT 2 OF 4			

DO NOT SCALE

J4 J3 J2 J1

L7 L6 L5 L4 L3 L2 L1

L20 L19 L18 L17 L16 L15 L14 L13 L12 L11 L10 L9 L8

L32 L31 L30 L29 L28 L27 L26 L25 L24 L23 L22 L21

L45 L44 L43 L42 L41 L40 L39 L38 L37 L36 L35 Q1 L34 L33

XTAL1

R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R38 R39 R40 R41 R42 R43 R44 R45 R46 R47 R48 R49 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R60 R61 R62 R63 R64 R65 R67 R68 R69 R70 R71 R72 R73 R74 R75 R76 R77 R78 R79 R80 R81

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 + C21 - + C22 - + C23 - + C24 -

7717 R1

7717-R1

S3 A3 S2 A2 S1 A1

D 7717

REVISION	BY	DATE
SEE SHEET 4		

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	BY	DATE	APPROVED BY	DATE
DWN	AB	3/19/80	E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO. 2280

SEE ENGRG. SPECIFICATIONS

No.

TITLE DISK MUX MASTER BOARD

FINISH

TOL. EX. AS NOTED
.XX ± FRAC. ±
.XXX ± ANG. ±
FINISH √

SCALE SHT 3 OF 4

210-7717 | D | 7717 | 1

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.

DO NOT SCALE

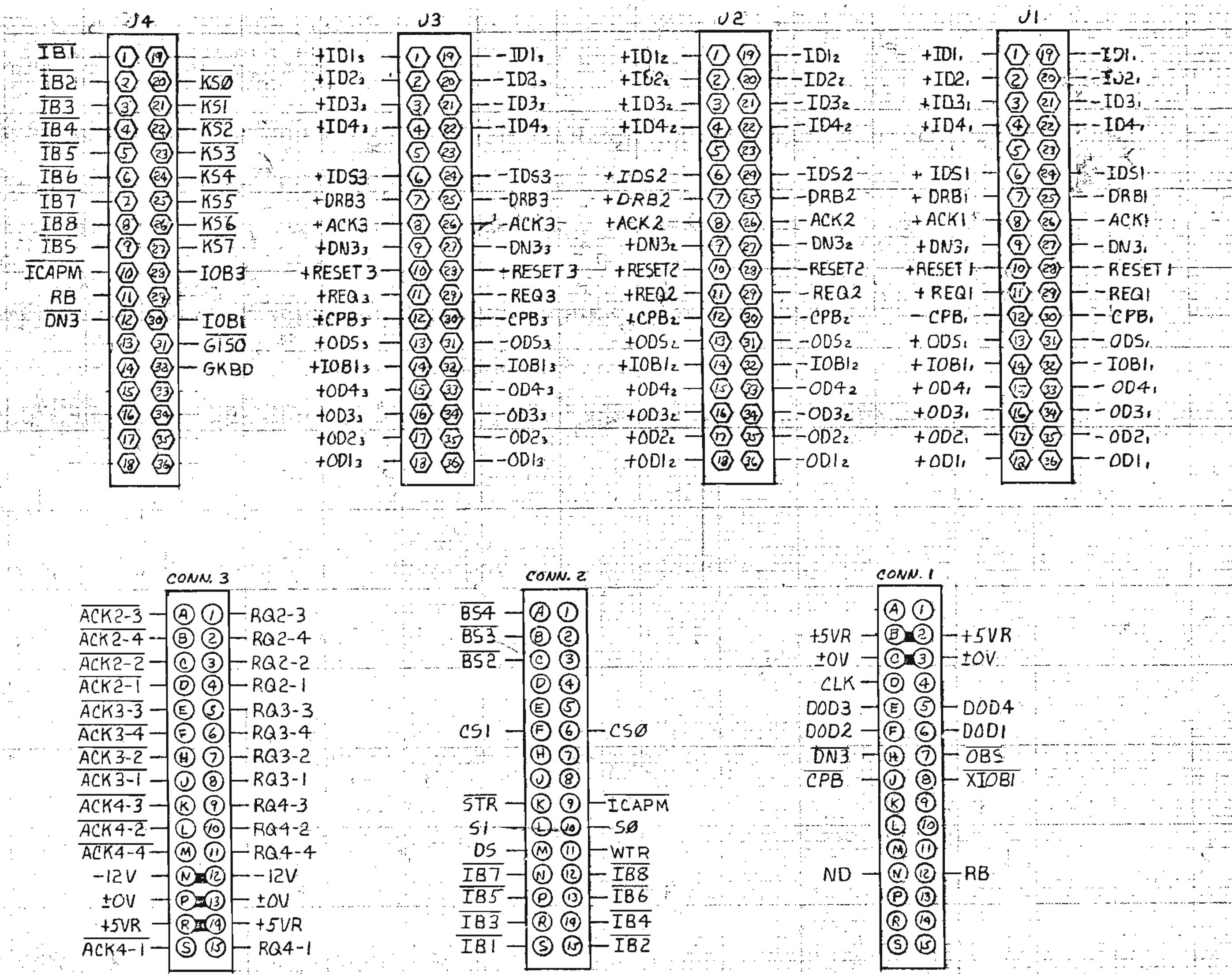
I.C. LOCATION	W.L. PART NO.	TYPE
L1,2,3,8,11,14, 21,24,27,28,33	376-0256	75113
L4	376-0082	74157
L5,6,23	376-0098	74174
L7	376-0080	74123
L9,10,12,13,15, 16,22,25	376-0275	MC3450
L17,30	376-0097	74195
L18	376-0006	7474
L29,42-45	376-0002	7400
L37	376-0010	7404
L26	376-0048	74153
L31,32	376-0102	74164
L34,39	376-0093	7432
L35	376-0056	7407
L36	376-0092	7425
L38	376-0226	74LS139
L40,41	376-0171	74148
L19	376-0266	74132
L20	376-0139	7414

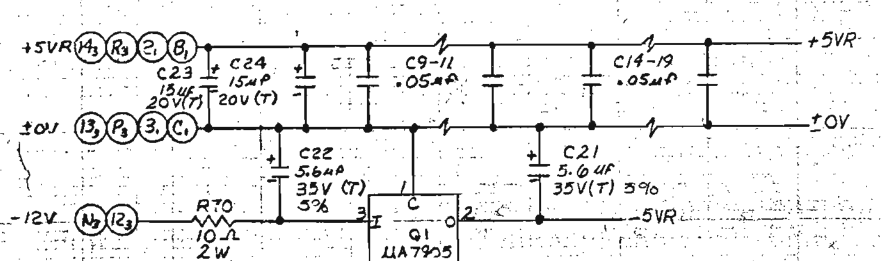
IC TYPE	LOCATION	SPARES
7400	L29	1
7407	L35	3
7425	L36	1
7432	L34	3
74LS139	L38	1

COMPONENT	TYPE	W.L. PART NO.
R1,3,9,11,17, 19,28,30,37, 39,46,48, 71-81,83	390Ω 1/4W,10%	330-2039
R2,4,10,12,18, 20,27,29,36, 38,45,47	150Ω 1/4W, 10%	330-2015
R5-8,13-16, 21-24,31-34, 40-43,49-52	100Ω 1/4W,10%	330-2010
R25	8.2K 1/4W,10%	330-3082
R26,35,44,54 56-62,64, 66-69,82	1K 1/4W, 10%	330-3010
R53	33K 1/4W,10%	330-4033
R55,63,65	330Ω 1/4W,10%	330-2033
R70	10Ω 2W, 10%	337-1010
C1,2	470pF 500V	300-1470
C3-8,12,13,	.1µF 50V	300-1930
C9-11,14-19	.05µF 12V	300-1900
C20	.01µF 25V	300-1903
C21,22	5.6µF 35V (T) 5%	300-4025
C23,24	15µF 20V (T)	300-4022
XTAL1	2 MHZ	321-0010
Q1	µA7905	374-0002
J1-4	36 PIN CONN.	350-1044

MNEMONIC	COORD.
ACK2-1, ACK4-4	2A8
ACK2+, ACK2-	1A7
ACK1+, ACK1-	1A6
ACK3+, ACK3-	1A5
BS2	2A5
BS3	2A6
BS4	2A6
CLK	2A8
CS0	2A6
CS1	2A6
CPB	1F1
+CPB1, -CPB1	1G7
+CPB2, -CPB2	1G3
+CPB3, -CPB3	1G5
DN3	1F1
+DN31, -DN31	1G6
+DN32, -DN32	1G3
+DN33, -DN33	1G5
DOD1 - DOD4	1A9
DRB1+, DRB1-	1D1
DRB2+, DRB2-	1C1
DRB3+, DRB3-	1B1
DS	2A2
GISO	1D1
GKBD	2A4
IBS	2G4
IB1 - IB8	2G3
ICAPM	1A4
-ID11 — -ID41	2G1
+ID11 — +ID41	2G1
-ID12 — -ID42	2B1
+ID12 — +ID42	2B1
-ID13 — -ID43	2E1
+ID13 — +ID43	2E1
+IOBI1, -IOBI1	1G6
+IOBI2, -IOBI2	1G3
+IOBI3, -IOBI3	1G4
IOB1	1F1
IOB3	1F1

MNEMONIC	COORD.
IDS1-, IDS1+	1B1
IDS2-, IDS2+	1D1
IDS3-, IDS3+	1C1
KSØ — KS7	1B2
ND	2A10
OBS	1F1
-OD11 — -OD41	1F11
+OD11 — +OD41	1F11
-OD12 — -OD42	1E11
+OD12 — +OD42	1E11
-OD13 — -OD43	1C11
+OD13 — +OD43	1C11
+ODS1, -ODS1	1G7
+ODS2, -ODS2	1G4
+ODS3, -ODS3	1G5
RB	1G2
-RESET1 — -RESET3	1G9
+RESET1 — +RESET3	1G9
-REQ1 — -REQ3	1G8
+REQ1 — +REQ3	1G8
RQ2-1 — RQ4-4	2E11
SØ	2A5
S1	2A5
STR	1B3
WTR	2G11
XIOB1	1F1





E-REV
0

REV	REVISION	APP'D
0	ORIGINATED PER CWR # E898	A.B 5-19-80
1	REVISED PER ECN # 15196	APP'D: 7-10-80

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

BY	DATE	APPROVED BY	DATE
DWN A.B	1-9-80	E ENGR R.S.	7-10-80
CHK R.S.	7-10-80	M ENGR	
		MFG ENGR	

MATERIAL | FINISH

MODEL NO. 2280

SEE ENGRG. SPECIFICATIONS No.

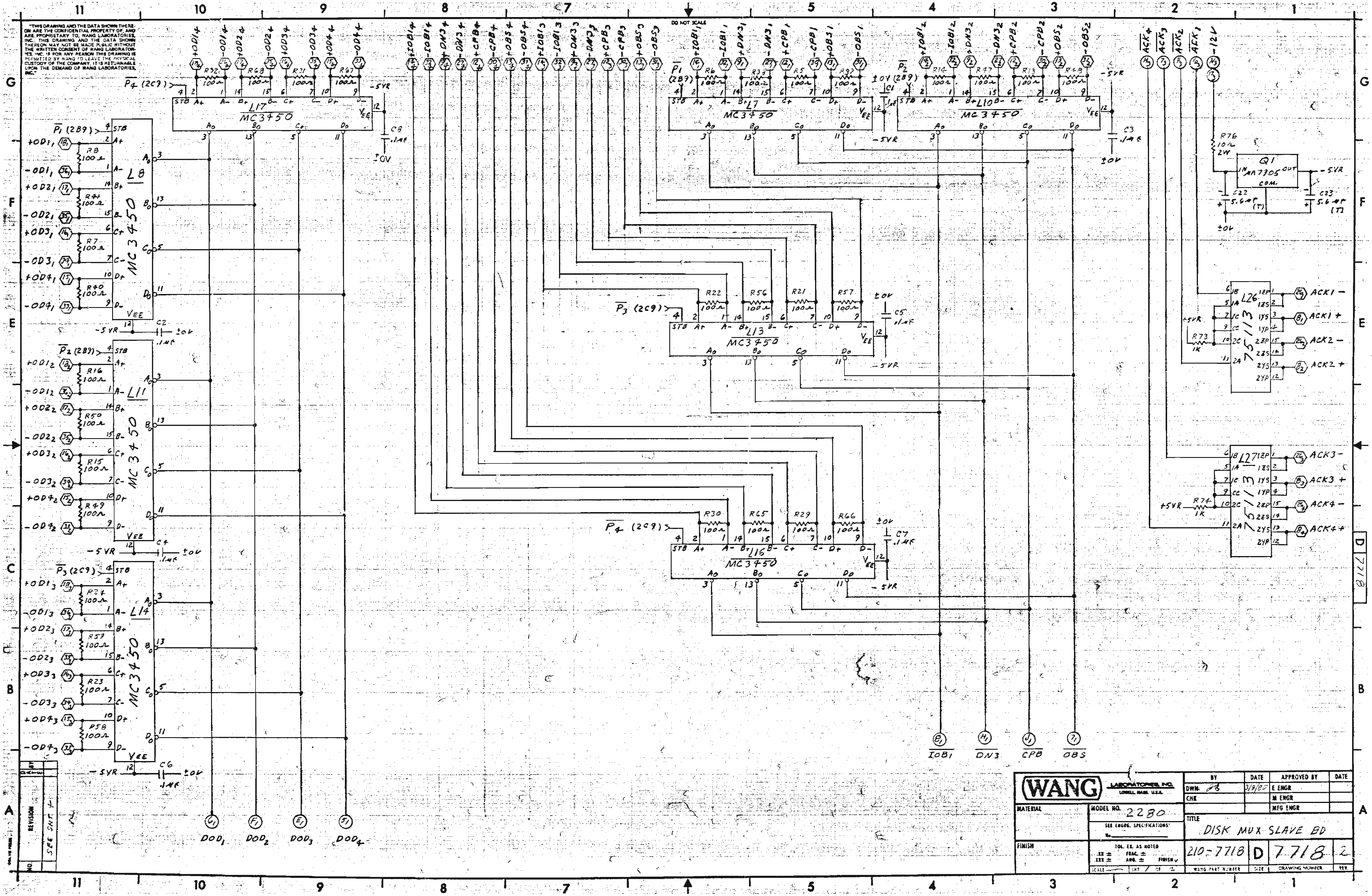
TOL. EX. AS NOTED .XX ± FRAC. ± .XXX ± ANG. ± FINISH ✓

SCALE | SHT 4 OF 4

TITLE DISK MUX MASTER BOARD

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
210-7717	D	7717	1

D 7717



DO NOT SCALE

S_0 (2C14) S_1 (2C11)

$\overline{BS}$ (2B11)

IB_7 IB_8 IB_3 IB_7 IB_2 IB_6 IB_1 IB_5 DS

+RESET1 -RESET1 +RESET2 -RESET2 +RESET3 -RESET3 +RESET4 -RESET4

+REQ1 -REQ1 +REQ2 -REQ2 +REQ3 -REQ3 +REQ4 -REQ4

CLK

ND

S_1 (2G8) S_0 (2G8) $\overline{BS}$ (2F7)

RB $\overline{STR}$

$\overline{P_4}$ (1G11)(1C7) $\overline{P_3}$ (1C11)(1E7) $\overline{P_2}$ (1E11)(1G4) $\overline{P_1}$ (1B11)(1G6)

IBS1- IBS1+ DRB1- DRB1+ IBS2- IBS2+ DRB2- DRB2+ IBS3- IBS3+ DRB3- DRB3+ IBS4- IBS4+ DRB4- DRB4+

RQ_4 RQ_3 RQ_2 RQ_1 $\overline{ICAPM}$

	BY	DATE	APPROVED BY	DATE
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	DWN	2/3/8	E ENGR	
	CHK		M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO. 2280

SEE ENGRG. SPECIFICATIONS No.

FINISH

TOL. EX. AS NOTED: XX ± FRAC. ± XXX ± ANG. ± FINISH √

SCALE SHT 2 OF 2

TITLE: DISK MUX SLAVE BD

210-7718 | D | 7718 | 2

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

REVISION | BY | DATE | APPROVED

SEE SHT 1