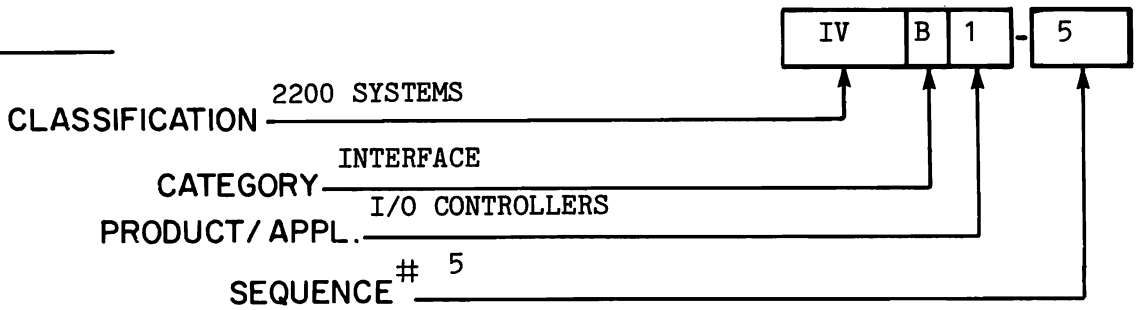
CUSTOMER ENGINEERING

PRODUCT SERVICE NOTICE

DATE: 9/22/80



TITLE:

MODEL 22C80 DISK MULTIPLEXER INTERFACE CONTROLLER (WL# 177-2280C)

This PSN contains the following 2280 Disk Multiplexer Interface Controller information.

1. GENERAL DESCRIPTION
2. SWITCH SETTINGS
3. INSTALLATION
4. SYSTEM INTERCONNECTION
5. DIAGNOSTICS
6. TROUBLESHOOTING
7. HARDWARE THEORY OF OPERATION (MAJOR-FUNCTION LEVEL)

Following is a list of documentation categories referenced by this PSN. Documentation from these other categories is required for the performance of certain installation/maintenance tasks.

Device Address Switch Settings -- IV.B.1-3
CPU Power Supply Voltage Adjustments -- IV.A.3
2280MUX System Interconnection -- IV.B.3
2280 Disk Diagnostic -- IV.C.1

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1. GENERAL DESCRIPTION

The Model 22C80 I/O controller (WL# 177-2280C or WL# 210-7715) provides the input/output interface between a 2200VP/LVP/MVP Central Processing Unit and a 2280 Disk Multiplexer (2280MUX).

2. SWITCH SETTINGS

See FIGURE 1 for information concerning the setting of device address switch SW1. The device addresses normally used for the 2280 Disk Drive are HEX 10 (primary address), HEX 20 (secondary address), or HEX 30 (secondary address). Refer to PSN IV.B.1-3 for more information concerning the setting of device address switches.

NOTE:

The HEX values given in FIGURE 1 are correct only for boards at Revision 2 and above. For R0 and R1 boards (limited distribution) the HEX values are as follows.

SWITCH #	HEX VALUE
1	01
2	80
3	20
4	10
5	08
6	04
7	02
8	NOT USED

3. INSTALLATION

The 22C80 can be installed in any available I/O slot in the 2200VP/LVP/MVP CPU. Be certain to power-off the CPU before installing the controller. Prior to inserting the 22C80 in a CPU, ensure that all switches on that board are set correctly (ref: Section 2). Also check to see that the fingerboard connectors are clean.

After installing the 22C80 in a unit, be certain to recheck and adjust, if necessary, CPU power supply voltages +5V (I/O) and -12V. Refer to documentation category IV.A.3 for the appropriate CPU voltage adjustment procedures.

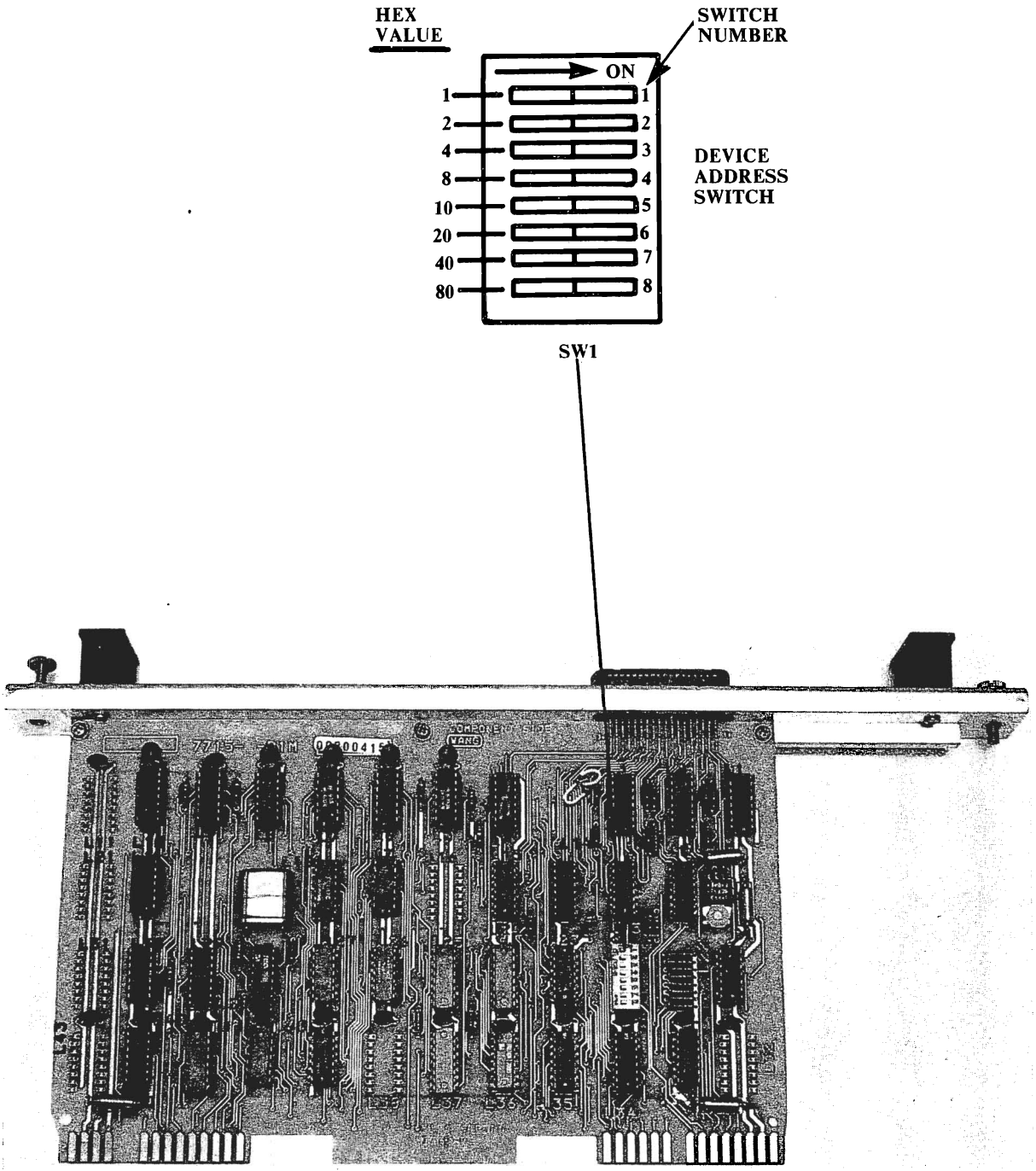
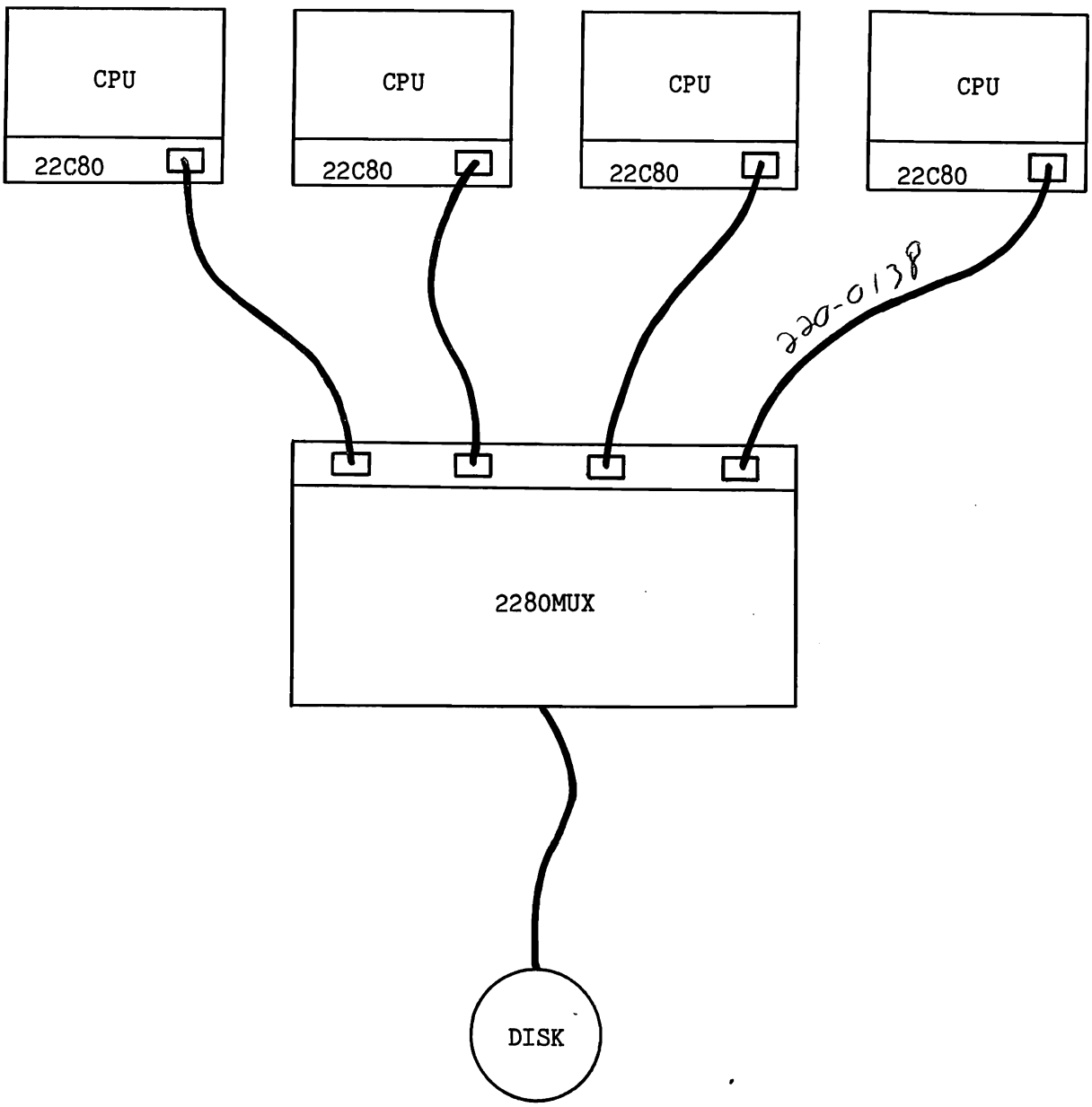


FIGURE 1 WL NO. 210-7715 22C80 INTERFACE BOARD

4. SYSTEM INTERCONNECTION

The I/O cables (WL# 220-0138) attached to jacks J1-J3 on the 2280MUX Multiplexer board (WL# 210-7717), and to jacks J1-J4 on the 2280MUX Port Expander boards (WL# 210-7718) connect to the 22C80 controller in each CPU of the multiplex system (see "Star" configuration below). Refer to documentation category IV.B.3 for more information concerning 2280MUX system interconnection.



5. DIAGNOSTICS

Up to the date of this publication, diagnostics designed to test all 2280MUX functions, as well as the associated 22C80 controllers, had not been completed. It is possible to test a majority of the 2280MUX and 22C80 functions with the standard 2280 Disk Diagnostic (WL# 701-2555). This is accomplished by running the diagnostic at several (a predetermined number) CPU's at the same time, with each CPU addressing a different disk surface (one surface only) in the drive. The predetermined number of CPU's at which the diagnostic can be run is equal to the number of data surfaces present in the drive under test (that is, 2280-1: two surfaces; 2280-2: four surfaces; 2280-3: six surfaces). Refer to documentation category IV.C.1 for detailed information concerning the standard 2280 Disk Diagnostic.

6. TROUBLESHOOTING

If only one channel of a 2280MUX system fails (I/O error indication), it is possible to isolate the cause of the failure by interchanging the I/O cables at the Port Expander board or Multiplexer board (as applicable) in the 2280 DPU/MUX. If, after swapping CPU-to-MUX cables, the problem remains with the same 2280MUX channel, conclude that the Port Expander/Multiplexer is defective; if the problem moves with the suspected 2200 CPU to the different 2280MUX channel, conclude that the 2200 CPU is defective--the most likely cause being the 22C80 I/O controller. If all channels fail, the 2280 DPU, the DPU/MUX power supply, the 2280MUX multiplexer board, the disk cables, or the 2280 disk itself may be defective.

7. HARDWARE THEORY OF OPERATION (MAJOR-FUNCTION LEVEL)

Address Bus and Control Circuitry (ref: FIGURE 2 and MNEMONICS)

Device Address Switch--

Represents the device address of the 2280 Disk Drive. This address is chosen by the customer and set by the Customer Engineer. The outputs of the switch are inputs to the Address Compare Circuit.

Address Compare Circuit--

Verifies the device address received from the CPU via the Address Bus ($\overline{AB1}$-$\overline{AB8}$) against the address represented by the Device Address Switch. The output of the compare circuit is input to the Select Latch. The output also enables operation of the DN3 Latch.

Select Latch--

Produces a Select ($\overline{SEL}$) signal if the device address received from the CPU and the address represented by the Device Address Switch setting are identical. This Select signal in turn generates a Request ($\overline{REQ}$) signal, which is sent to the 2280 Disk Multiplexer (2280MUX) indicating the CPU requires disk access. The Select signal also enables operation of the Control Decoder, and the OBS Latch.

DN3 Latch--

Monitors CPU Address Bus bit 7 (HEX 40) to determine whether access to the second 2280 Disk Drive in a daisy-chain configuration is requested. If the second drive is specified, a DN3 signal is sent to the 2280MUX indicating such.

Control Decoder--

Decodes control data received from the CPU via the Output Bus ($\overline{OB1}$, and $\overline{OB8}$) into the desired command as follows:

	LOGIC LEVEL			
OB1	"0"	"1"	"0"	"1"
OB8	"0"	"0"	"1"	"1"
COMMAND	Clear Parity Error	Hog Disk	Reset Disk	Release Disk

Hog Latch--

When a "Hog" command is decoded (see Control Decoder), the Hog Latch produces a Request ($\overline{REQ}$) signal which is sent to the 2280MUX indicating the CPU requires exclusive use of the disk.

When a "Release Disk" command is decoded, the Hog Latch terminates the Request signal.

Disk Ready/Busy Circuit--

Monitors the Ready/Busy signal received from the disk ($\overline{\text{DRBY}}$), and relays that status to the CPU.

OBS Latch--

Generates an Output Data Strobe ($\overline{\text{ODS}}$) which strobes the Output Data to the 2280MUX.

Shift Register--

Produces the timing pulses required for controlling the transfer of data between the CPU and the 2280MUX.

Level Converters (Line Receivers/Drivers)--

Convert TTL voltage levels to the differential voltage levels (Emitter Coupled Logic--ECL--levels) required by the 2280MUX Port Expander board. Use of ECL in this application allows each CPU disk I/O logic to operate at optimum speed even with the greater distance from CPU to multiplexer, as compared to the driver/receiver distances possible with TTL.

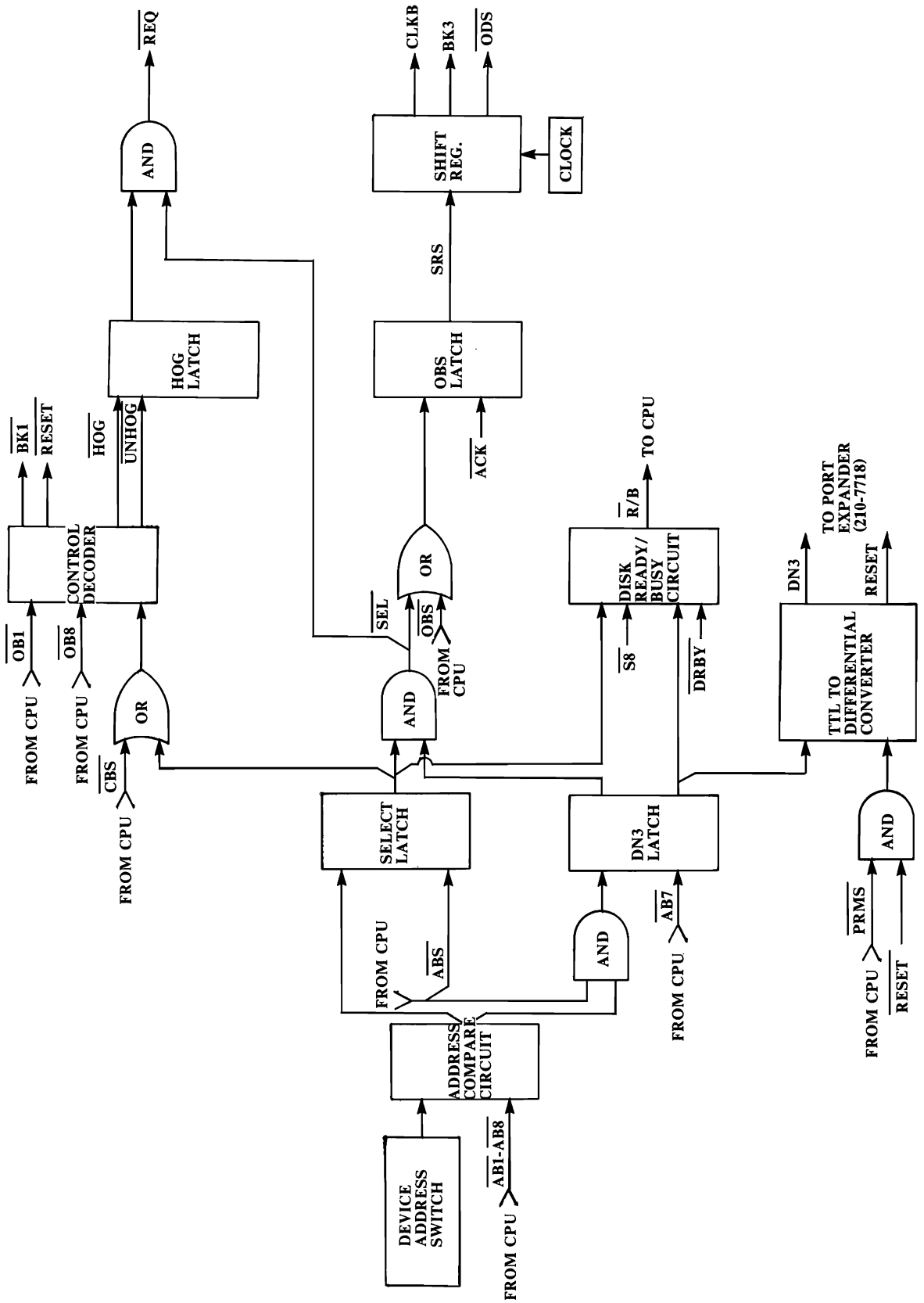


FIGURE 2 22C80 BLOCK DIAGRAM (ADDRESS BUS AND CONTROL CIRCUITRY)

Input Bus Circuitry (ref: FIGURE 3 and MNEMONICS)

Input Data Demultiplex Latches (Data)--

Receives the read data that is to be sent to the CPU from the 2280MUX Port Expander board. On the leading edge of the Input Data Strobe ($\overline{IDS}$), the low order Input Data bits ($\overline{ID1}$-$\overline{ID4}$) are selected through the demultiplexer, and are then sent to the Parity Checker and the Input Bus Mux. On the trailing edge of $\overline{IDS}$, the high order bits ($\overline{ID5}$-$\overline{ID8}$) are selected through the demultiplexer.

Input Data Demultiplex Latches (Disk Status)--

Receives the disk status from the 2280MUX Port Expander board. On the leading edge of the Status Request Strobe ($\overline{SRB}$), the low order Input Data bits ($\overline{ID1}$-$\overline{ID4}$) are selected through the demultiplexer as S1-S4, and the are sent to the Input Bus Mux for transmission to the CPU. On the trailing edge of $\overline{SRB}$, the high order bits ($\overline{ID5}$-$\overline{ID8}$) are selected through the demultiplexer as $\overline{S5}$-$\overline{S8}$.

Input Bus Mux--

Selects either disk status or data as Input Bus bits $\overline{IB1}$-$\overline{IB8}$, and transmits the information to the CPU.

Parity Checker--

Verifies the parity bit, which is received along with the Input Data for integrity. If the parity bit is incorrect the Parity Error Latch is set.

Parity Error Latch--

Indicates a parity error occurring during transfer of data between the 2280MUX and the 22C80 Interface.

Level Converters (Line Receivers/Drivers)--

Convert differential voltage levels (Emitter Coupled Logic--ECL--levels) received from the 2280MUX Port Expander board to the TTL levels required by the 22C80 Interface board. Use of ECL in this application allows each CPU disk I/O logic to operate at optimum speed even with the greater distance from CPU to multiplexer, as compared to the driver/receiver distances possible with TTL.

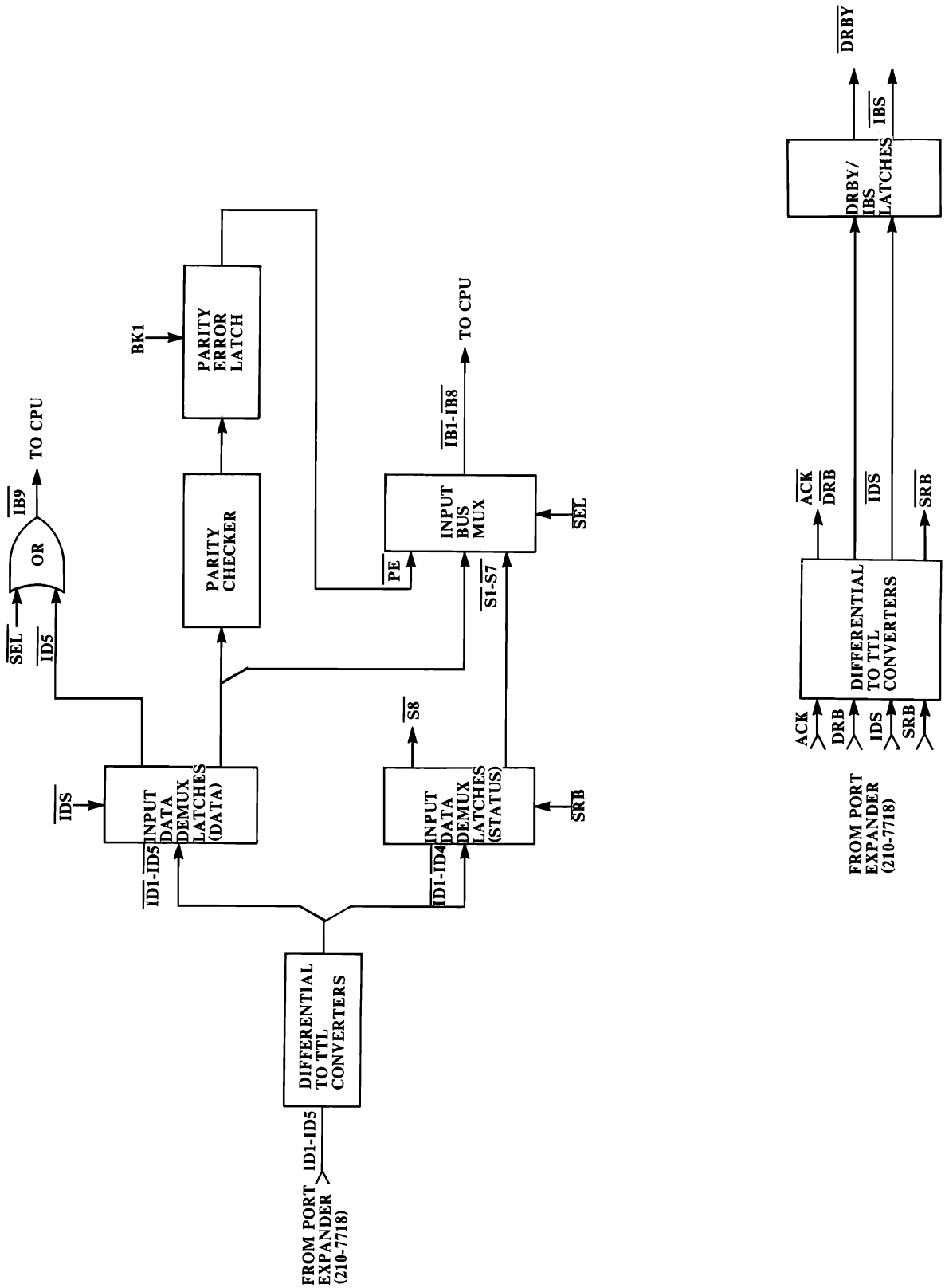


FIGURE 3 22C80 BLOCK DIAGRAM (INPUT BUS CIRCUITRY)

Output Bus Circuitry (ref: FIGURE 4 and MNEMONICS)

Output Bus Mux--

Receives the write data that is to be sent to the disk from the CPU Output Bus ($\overline{OB1}$-$\overline{OB8}$). During the first half of the Output Bus Strobe ($\overline{OBS}$), the low order bits ($\overline{OB1}$-$\overline{OB4}$) are selected through the Output Bus Mux as Output Data bits $\overline{OD1}$-$\overline{OD4}$. During the second half of the $\overline{OBS}$, the high order bits ($\overline{OB5}$-$\overline{OB8}$) are selected through the multiplexer. The Output Data bits are sent to the 2280MUX for transmission to the disk drive.

Parity Generator--

Accepts the write data that is to be sent to the disk from the CPU Output Bus ($\overline{OB1}$-$\overline{OB8}$), and generates a parity bit ($\overline{OD5}$) which is sent to the 2280MUX along with the Output Data.

Level Converters (Line Receivers/Drivers)--

Convert TTL voltage levels to the differential voltage levels (Emitter Coupled Logic--ECL--levels) required by the 2280MUX Port Expander board. Use of ECL in this application allows each CPU disk I/O logic to operate at optimum speed even with the greater distance from CPU to multiplexer, as compared to the driver/receiver distances possible with TTL.

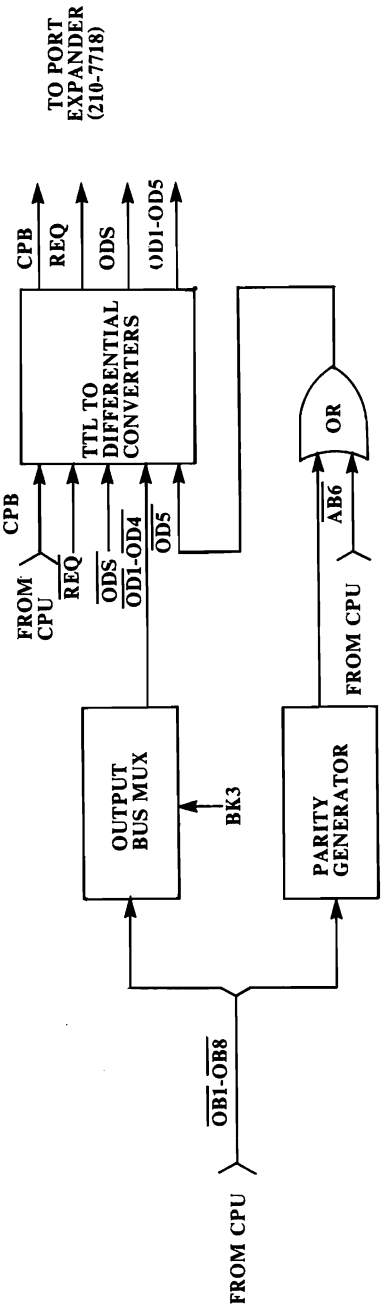


FIGURE 4 22C80 BLOCK DIAGRAM (OUTPUT BUS CIRCUITRY)

SIGNAL MNEMONICS

$\overline{AB1}$-$\overline{AB8}$ (Address Bus):

Address data for I/O controller selection -- from CPU

$\overline{AB7}$ (Address Bus):

Indicates access to second drive is required -- from CPU

$\overline{ABS}$ (Address Bus Strobe):

Strobes address data to I/O controller

ACK (Acknowledge):

Acknowledge of CPU request for disk use -- from Port Expander (210-7718)

$\overline{ACK}$ (Acknowledge):

Acknowledgement of CPU request for disk use -- internal

$\overline{BK1}$:

Clears Parity Error Latch -- internal

BK3:

Selects either low or high order data as Output Data -- internal

$\overline{CBS}$ (Control Bus Strobe):

Strobes control data to I/O controller -- from CPU

CLKB (Clock B):

Selects $\overline{AB6}$ as $\overline{OD5}$ -- internal

$\overline{CPB}$ (Central Processor Busy):

CPU ready/busy status -- from CPU

CPB (Central Processor Busy):

CPU ready/busy status -- internal

DN3 (Disk Number 3):

Indicates access to second drive is required -- internal

DRB (Disk Ready/Busy):

Disk ready/busy status -- from Port Expander (210-7718)

$\overline{\text{DRB}}$ (Disk Ready/Busy):

Disk ready/busy status -- internal

$\overline{\text{DRBY}}$ (Disk Ready/Busy):

Disk ready/busy status -- internal

$\overline{\text{HOG}}$:

Initiates exclusive use of disk -- internal

$\overline{\text{IB1}}$-$\overline{\text{IB8}}$ (Input Bus):

Read data to be sent to CPU -- to CPU

$\overline{\text{IB9}}$ (Input Bus):

ENDI bit -- to CPU

$\overline{\text{IBS}}$ (Input Bus Strobe):

Strobes write data from disk to CPU -- to CPU

ID1-ID5 (Input Data):

Read data to be sent to CPU --from Port Expander (210-7718)

$\overline{\text{ID1}}$-$\overline{\text{ID4}}$ (Input Data):

Status to be sent to CPU -- internal

$\overline{\text{ID1}}$-$\overline{\text{ID5}}$ (Input Data):

Read data to be sent to CPU -- internal

$\overline{\text{ID5}}$ (Input Data):

Generates ENDI bit -- internal

IDS (Input Data Strobe):

Strobes read data from disk to CPU -- from Port Expander (210-7718)

$\overline{\text{IDS}}$ (Input Data Strobe):

Strobes read data from disk to CPU -- internal

$\overline{\text{OB1}}$-$\overline{\text{OB8}}$ (Output Bus):

Write data to be sent to disk -- from CPU

$\overline{\text{OB1}}$ (Output Bus):

Decoded into control signals -- from CPU

$\overline{\text{OB8}}$ (Output Bus):

Decoded into control signals -- from CPU

$\overline{\text{OBS}}$ (Output Bus Strobe):

Strobes write data from CPU to disk -- from CPU

$\overline{\text{OD1}}$-$\overline{\text{OD4}}$ (Output Data):

Write data to be sent to disk -- internal

$\overline{\text{OD5}}$ (Output Data):

Parity bit for write data to be sent to disk -- internal

OD1-OD5 (Output Data):

Write data to be sent to disk -- to Port Expander (210-7718)

$\overline{\text{ODS}}$ (Output Data Strobe):

Strobes write data from CPU to disk -- internal

ODS (Output Data Strobe):

Strobes write data from CPU to disk -- to Port Expander (210-7718)

$\overline{\text{PE}}$ (Parity Error):

Parity error indication -- internal

$\overline{\text{PRMS}}$ (Prime Signal):

Resets DPU and disk -- from CPU

$\overline{\text{R}}$/B (Ready/Busy):

Disk ready/busy status -- to CPU

$\overline{\text{REQ}}$ (Request):

Request by CPU for disk use -- internal

REQ (Request):

Request by CPU for disk use -- to Port Expander (210-7718)

$\overline{\text{RESET}}$:

Resets DPU and disk -- internal

RESET:

Resets DPU and disk -- to Port Expander (210-7718)

$\overline{S1}$-$\overline{S7}$ (Status):

Status to be sent to CPU -- internal

$\overline{S8}$ (Status):

Determines disk ready/busy status -- internal

$\overline{SEL}$ (Selected):

Indicates I/O controller selected -- internal

SRB (Status Request Bit):

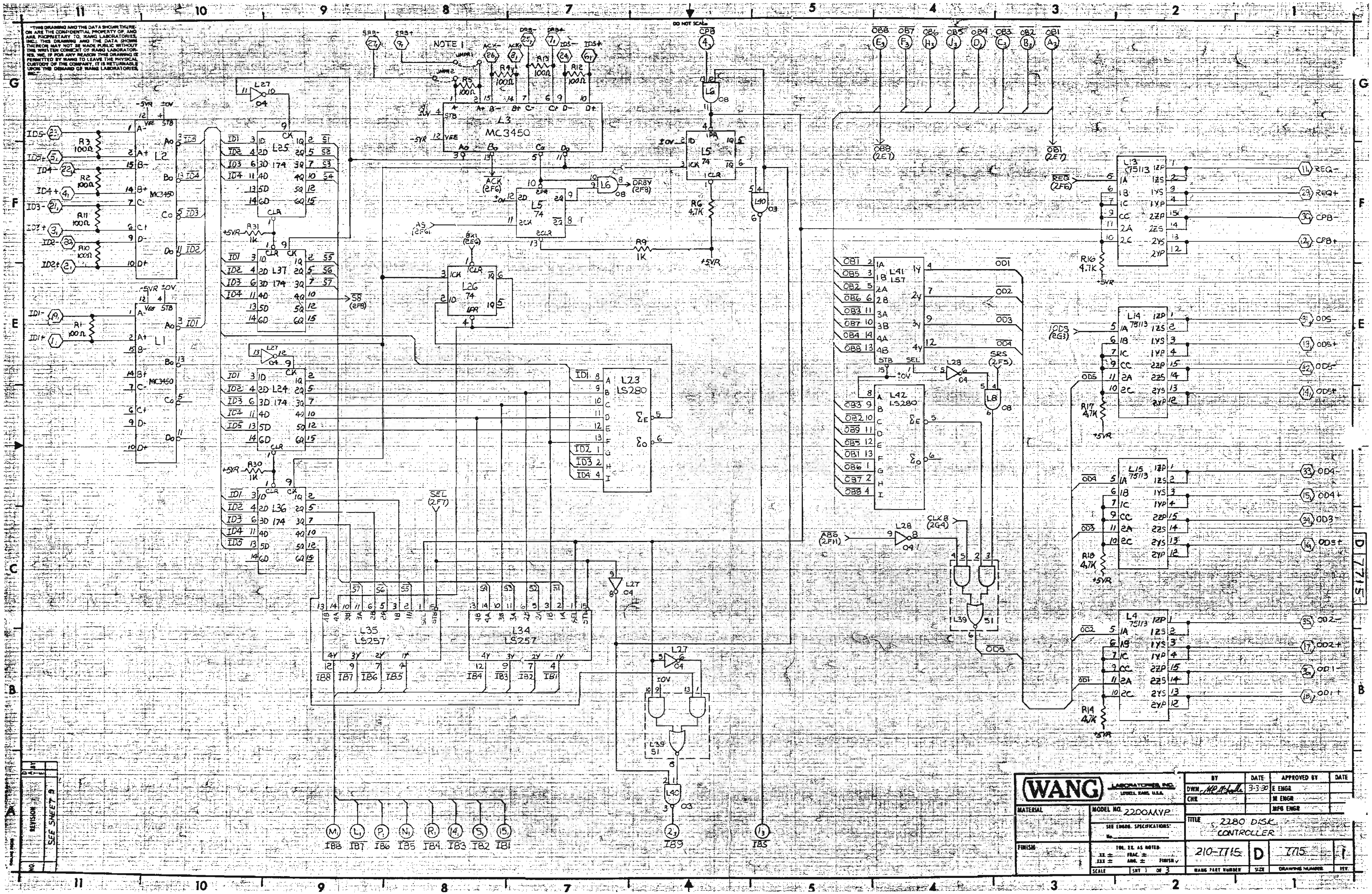
Strobes disk status to the 22C80 -- from Port Expander (210-7718)

$\overline{SRB}$ (Status Request Bit):

Strobes disk status to the 22C80 -- internal

$\overline{UNHOG}$:

Terminates exclusive use of disk -- internal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L2 MC3450
L1 MC3450
L3 MC3450
L25 174
L37 174
L24 174
L36 174
L5 74
L26 74
L6
L23 LS280
L35 LS257
L34 LS257
L27
L39 51
L40 03
L41 LS7
L42 LS280
L28
L8
L13 75113
L14 75113
L15 75113
L4 75113
REQ-
REQ+
CPB-
CPB+
OD5-
OD5+
OD4-
OD4+
OD3-
OD3+
OD2-
OD2+
OD1-
OD1+
IB8
IB7
IB6
IB5
IB4
IB3
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IBS
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WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
BY
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APPROVED BY
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E ENGR
CHK
M ENGR
MFG ENGR
MATERIAL
MODEL NO. 2200MVP
SEE ENGRG. SPECIFICATIONS
TITLE 2280 DISK CONTROLLER
FINISH
TOL. EX. AS NOTED
210-7715
D
7715
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SCALE
SHT 1 OF 3
WANG PART NUMBER
SIZE
DRAWING NUMBER
REV.

DO NOT SCALE

NOTE:
1. ONLY ONE PAIR OF JUMPERS (JMPR 1 & 2 OR JMPR 3 & 4) USED AT ONE TIME.

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY	DATE
MATERIAL	DWN AC/KB		E ENGR	
MODEL NO. 2200MVP	CHK		PE ENGR	
SEE ENGRG. SPECIFICATIONS			MFG ENGR	
FINISH	TITLE 2280 DISK CONTROLLER			
TOL. EX. AS NOTED: XX ± FRAC ± XXX ± ANG. ± FINISH √	210-7715	D	7715	1
SCALE	SHT 2 OF 3	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.

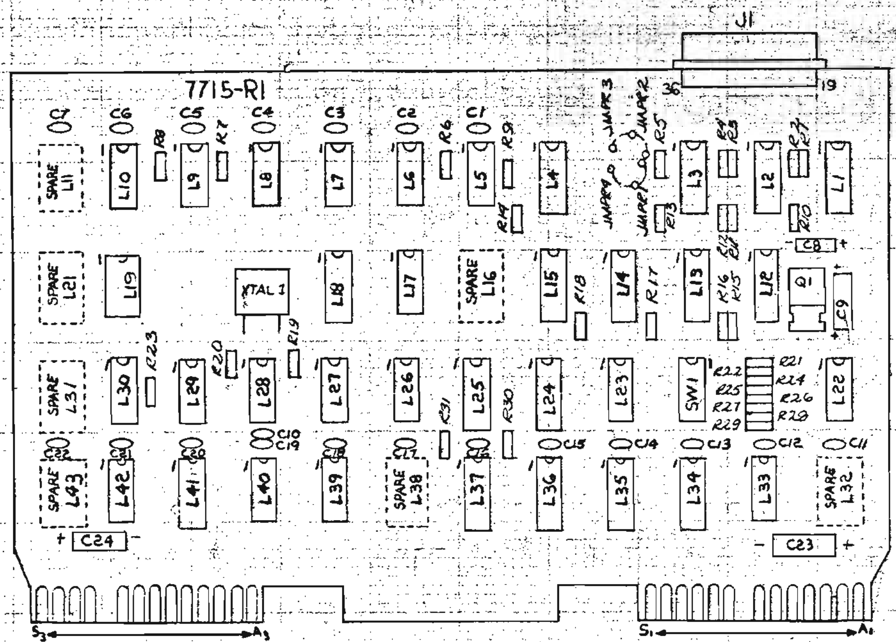
NO.	REVISION	DATE	APPROVED
	SEE SHEET 3		

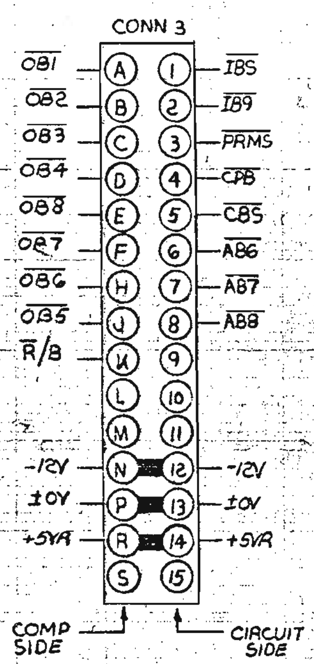
DO NOT SCALE

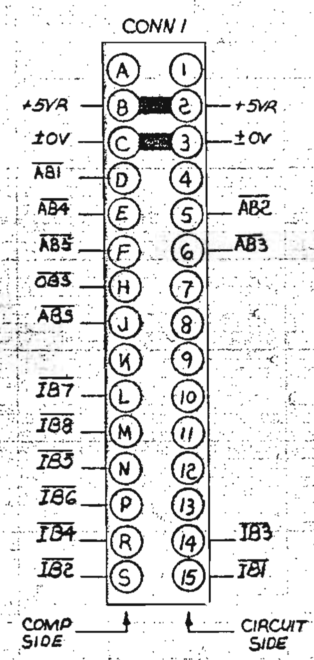
COMPONENT	TYPE	W.L. PART NO.
R1-5, 10-13	100Ω 1/4W 10%	330-2010
R6-8, 14-18, 23	4.7K 1/4W 10%	330-3047
R19, 20	330Ω 1/4W 10%	330-2033
R9, 21, 22, 24-31	1K 1/4W 10%	330-3010
C1-7, 11-22	.05 µf 12V	300-1900
C8	5.6µf 35V (T)	300-4025
C9, 23, 24	15µf 20V (T)	300-4022
C10	.01 µf 25V	300-1903
Q1	µA7905	374-0002
XTAL 1	20 MHZ	321-0010
SW1	SPST 8POS	325-1503
U1	CONN 36 POS	350-1044

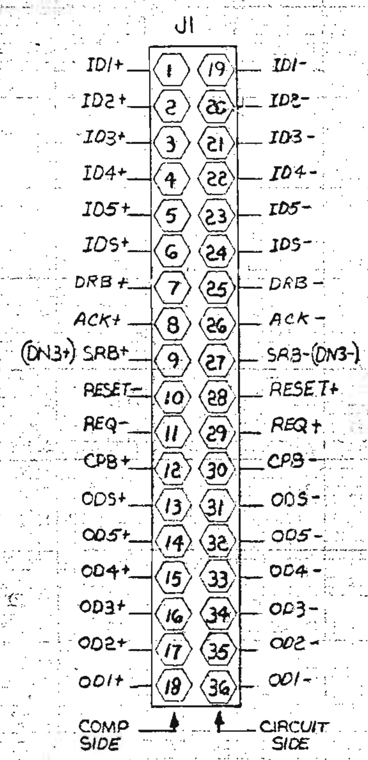
LOCATION	TYPE	W.L. PART NO.
L1, 2, 3	MC3450	376-0275
L4, 12, 13, 14, 15	75113	376-0256
L5, 9, 26, 30	7474	376-0006
L6, 8, 17	7408	376-0081
L7	7402	376-0016
L10	7432	376-0093
L19	7400	376-0002
L18	9321	376-0096
L22, 33	74LS266	376-0148
L23, 42	74LS280	376-0242
L24, 25, 36, 37	74174	376-0098
L27, 28	7404	376-0010
L29	74195	376-0097
L34, 35	74LS257	376-0204
L39	7451	376-0012
L40	7403	376-0028
L41	74157	376-0082
L11, 16, 21, 31, 32, L38, 43	SPARE	

TYPE	LOCATION	SPARES
7400	L19	3
7402	L7	1
7408	L6	2
	L17	1
7432	L10	3
7474	L30	1
74LS266	L22	1
9321	L18	1



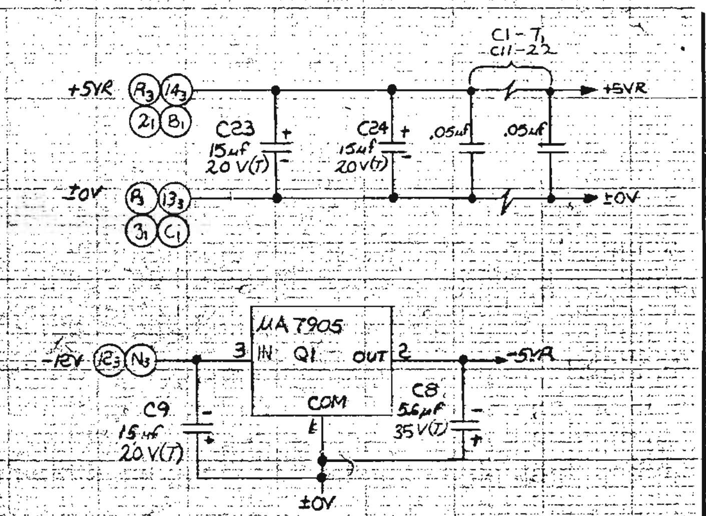






MNEMONIC	COORD
ABS	2G9
AB1	2G9
AB2 - AB8	2E11
AB7	2G9
ACK+, ACK-	1G7
CBS	2D11
CPB	1G6
CPB+, CPB-	1F1
DN3+, DN3-	2E1
DRB+, DRB-	1G7
IBS	1A5
IB1 - IB8	1A8
IB9	1A8
ID1+ ID1-	1E11
ID2+, ID2-	1E11
ID3+, ID3-	1F11
ID4+, ID4-	1F11

MNEMONIC	COORD
ID5+, ID5-	1F11
IDS+, IDS-	1G7
OBS	2G7
ODS+, ODS-	1E1
OB1 - OB8	1G4
OD1+, OD1-	1B1
OD2+, OD2-	1B1
OD3+, OD3-	1C1
OD4+, OD4-	1D1
OD5+, OD5-	1E1
PRMS	2E11
R/B	2F1
RESET+, RESET-	2E1
REQ+, REQ-	1F1
SRB+, SRB-	1G8



E-REV

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	DWN	3-3-80	E ENGR	
	CHK		M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO. 2200MVP

SEE ENGRG. SPECIFICATIONS No.

TITLE 2280 DISK CONROLLER

FINISH

TOL. EX. AS NOTED: .XX ± .XXX ± FRAC. ± ANG. ± FINISH

SCALE SHT 3 OF 3

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
210-7715	D	7715	1