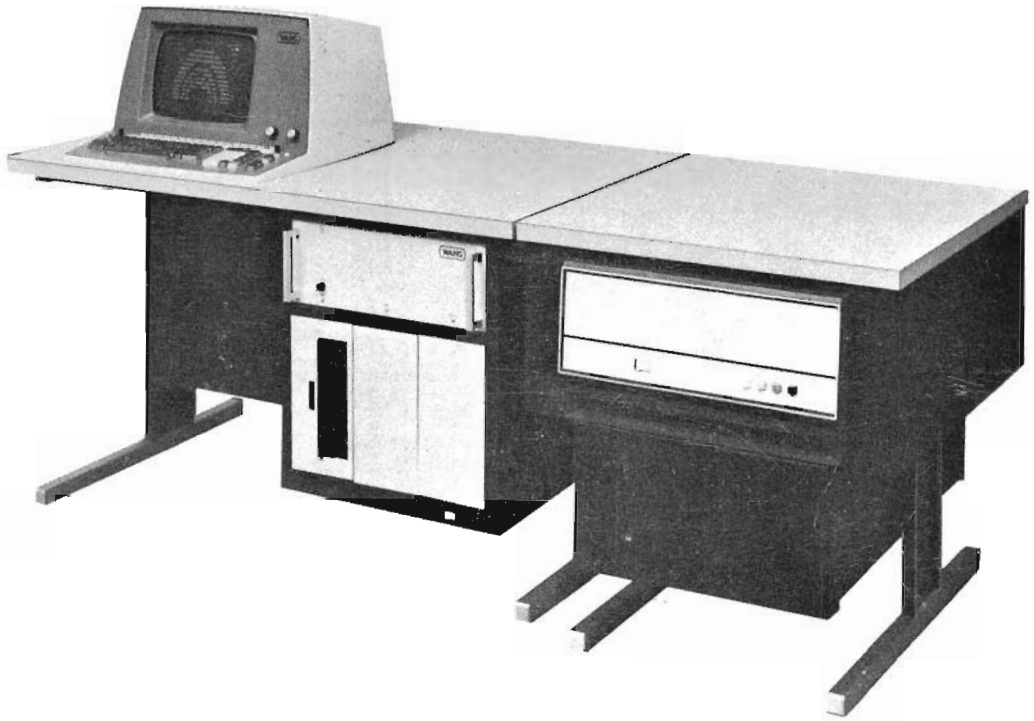
03-0071-1

Customer Engineering Division



Model 2200MVP

Maintenance Manual

WANG

CUSTOMER ENGINEERING

PUBLICATION UPDATE BULLETIN

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This PUB. provides updated information to the appropriate sections of the 2200 MVP Computer System Product Maintenance Manual.

INSTRUCTIONS:

Remove and insert attached pages and/or microfiche as follows:

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WANG

4103

2200 COMPUTER

Model: MVP

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Customer Engineering
Product Maintenance Manual

729-0584-A

PREFACE

This documentation package for the 2200MVP Computer consists of five separate publications including a basic Product Maintenance Manual (PMM), along with a Service Newsletter (SN) and three Product Service Notices (PSN's) inserted at the end of the PMM. The five publications are as follows:

1. PMM 729-0584: This version of the 2200MVP Computer PMM contains a new Illustrated Parts Breakdown (IPB) for the 2200MVP-A to replace the original Bill of Materials (BOM) in Appendix E

2. SN 729-0586: 2200VP/MVP Fan Replacement With Large I/O Controllers

3. PSN 729-0813: Model 2236MXD (WL# 177-3236-1) MUX/Controller

4. PSN 729-0814: Model 22C32 (WL# 212-3012) Triple Controller

5. PSN 729-1020: Installation of Option "C" Into 2200 MVP System

The scope of this documentation package reflects the type of maintenance philosophy selected for this product (swap unit, printed circuit assembly, chip level or any combination thereof). It's purpose is to provide the Wang-trained Customer Engineer (CE) with instructions to operate, troubleshoot and repair the 2200MVP Computer.

Second Edition (January 1984)

This edition of the 2200MVP PMM obsoletes document numbers 729-0584, 729-0586, 729-0813, 729-0814, and 729-1020. The material in this document may only be used for the purpose stated in the Preface. Updates and/or changes to this document will be published as PSN's or subsequent editions.

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Customer Engineering Division

Model 2200MVP

Maintenance Manual

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PREFACE

THIS PUBLICATION REPLACES SERVICE BULLETIN #83
AND THE MODEL 2200MVP MAINTENANCE MANUAL #03-0071

This manual should be considered a source document for all 2200MVP system-level maintenance information. The 2200MVP CPU, the 2236D Terminal, and the 2236MXD I/O Controller are supported directly by this text; the text also supports--by indirect reference--every peripheral device belonging to the system.

Detailed information relating to system peripherals--installation procedures, specialized diagnostic tests, preventive maintenance procedures, adjustments, and troubleshooting procedures--can be found in the maintenance manuals that support each peripheral.

A list of 2200MVP system documentation, categorized by product, follows:

THE MVP SYSTEM (Overview Documentation):

2200 MVP Brochure; WL# 700-4587
2200 MVP Technical Information; WL# 700-4656
2200 MVP Introductory Manual; WL# 700-4693
2200 VP/MVP BASIC-2 Lang. Reference Manual; WL# 700-4080, 4080-1, 4080-2
WCS 40/2200MVP Preliminary Service Bulletin #83 (Replaced by 03-0071)
2200MVP Maintenance Manual; CE Div. #03-0071 (Replaced by 03-0071-1)
2200MVP Maintenance Manual; CE Div. #03-0071-1

THE MVP CPU

2200MVP Maintenance Manual; CE Div. #03-0071
Module Repair Guide #'s 4.1A, 4.2A, 4.3A, 4.4A, 4.5
2236D/2236D Data Sheet; WL# 700-4807
Module Repair Guide #3.2

SYSTEM INTERACTIVE TERMINAL (2236D)

2236D/2236MXD Data Sheet; WL# 700-4807
Model 2236D Interactive Terminal User Manual; WL# 700-4405
Service Bulletins #73, 79, 80, 80A
Module Repair Guide #'s 3 & 3.1
ISN #'s 121, 141A, 141B, 149, 173, & 179
SNL #90
CEA #31

OTHER SYSTEM PERIPHERALS

DISKS:

2260 (all versions)
SNL #'s 86.1 (key document)
2260 B Data Sheet; WL# 700-3483
2260C Fixed/Removable Disk Drive Data Sheet
2260B/C Disk Drive Ref. Addenda; WL #700-3159-1,2
2260BC & C Disk Drive Ref. Addendum; WL# 700-4081-2
2200VP/MVP Disk Drive Addendum; WL #700-4081
Service Bulletin #'s 43, 43.1, 43.2, 43.2A, 72, & 86A
Mass Storage Device Manual; CE Div. #03-0026
Field-Level Maint. Guide: Diablo Series 40 Drives; CE Div. #03-0057
Diablo Series 40 Disk Drive Maintenance Manual
Diablo Series 40 Disk Drive Parts Catalog
Diablo 429 Power Supply Maintenance Manual
Diablo 44B Disk Drive Maintenance Manual
Diablo 44B Disk Drive Parts Catalog
CDC 10 Meg 'Hawk' Maintenance Manual (CE/OEM)
CDC 10 Meg 'Hawk' Training Manual CE Div #03-0059
CDC Microcircuits Manual (OEM)
Wang 'Hawk' Manual #03-0072
ISN #'s 10, 17, 45, 65, 75.1, 81, 114, 114, 116, 116A, 125, 136, 142, 156, 161A, 164, 170, 171, 174, & 184
SNL #'s 1, 5, 47, 51, 58, 87, 131, & 132

2270A
2270A IBM 3740-Compat. Diskette System Data Sheet; WL #700-4152
Service Bulletin #82
ISN #'s 85, 87, 91, 122, 129A, 154, 154.1
SNL #'s 32, 65, 123

2280 (all versions)
2280 Fixed/Removable Disk Drive Data Sheet; WL #700-4843
CDC (Phoenix) Cartridge Module Drive Prelim. Hardware Maint. Manual
FLMG: Phoenix Disk Drives; CE Div. Publication (still in prep. stage)

PRINTERS & PLOTTERS:

2201L
2201L Output Writer Data Sheet; WL #700-4377
2201L Output Writer User Manual; WL #700-4403
ISN #s 50, 111, 152, 159
SNL #s 3, 4, 29, 35, 92

2221W
2221W Line Printer Data Sheet; WL #700-3620
2221W Line Printer User Manual; WL #700-4403
Model 72 Matrix Printer (2221W) Manual; CE Div. #03-0027
Matrix Printer FLMG #03-0060
ISN #s 83, 96, 102, 108.1, & 176
SNL #s 4, 21, 26, 30, 36, 41, 48, 52, & 100
CEA #s 7 & 32

2231W-1, 2, 3, & 6
- 2231W Line Printer Data Sheet; WL #700-3821
- 2231W Line Printer User Manual; WL #700-3877
- 2231W-3 Data Sheet; WL #700-4375
- 2231W-3 User Manual; WL #700-4457
- 2231W-6 Data Sheet; WL #700-4677
- 2231W-6 User Manual; WL #700-5070
- Model 61/62 Matrix Printer (2231W) Manual; CE Div. #03-0077
- Matrix Printer FLMG #03-0060
- Service Bulletin #76
- ISN #s 118 & 163
- SNL #s 54, 61, 81, 83, & 100
- CEA #18

2232B
- 2232B Flatbed Plotter Data Sheet; WL 700-3194
- 2232B User Manual; WL# 700-3371
- Service Bulletin #s 44, 44.1
- SNL #s 92 & 92A

2251
- 2251 (Victor) Printer Data Sheet; WL# 700-4028
- 2251 (Victor) Printer User Manual; WL# 700-4042
- 2251 User Manual Addendum; WL# 700-4417
- ISN # 146

2261W
- 2261W Data Sheet; WL #700-4144
- 2261W Line Printer User Manual; WL #700-4271
- 2261W Line Printer User Manual Addendum; WL #700-4423
- Matrix Printer FLMG #03-0060
- Model 77 Quad Head (2261W) Printer Manual; CE Div. #03-0061
- ISN #s 157, 167, & 176
- SNL #s 102, 111, & 119

2263-1,2
- 2263 Line Printer Data Sheet; WL #700-4149
- 2263 Line Printer User Manual; WL #700-4251
- Chaintrain - Logic & Troubleshooting Manual (OEM)
- Chaintrain - Maintenance Instructions Manual (OEM)
- Chaintrain - Operation Instructions Manual (OEM)
- Chaintrain - Principles of Operation Manual (OEM)
- Chaintrain - Illustrated Parts Breakdowns (OEM)
- ISN #s 162, 168, & 169
- SNL #98

2271
- 2271 Output Writer Data Sheet; WL #700-4147
- 2271 Output Writer User Manual; WL #700-4276

2272
- 2272 Digital Drum Plotter Data Sheet; WL #700-3826
- 2200 Plotter Utilities Manual; WL #700-3838
- 2200 Plotter Utilities Manual Addendum; WL #700-3838-1
- 2272 Digital Plotter Prelim. Maint. Manual; CE Div. Publication
- Module Repair Guide #8

2281
2281 Daisy Printer Data Sheet; WL #700-4146
Service Bulletin #74
Diablo HY-TYPE II Maintenance Manual
Diablo HY-TYPE II Illustrated Parts Catalog
Module Repair Guide #'s 7 & 9
SNL #s 74, 97, & 128

2281P
2281P Data Sheet; WL# 700-4473
Service Bulletin # 74.1
SNL #s 128 & 133

2282
2282 Graphic CRT Plotter Data Sheet; WL# 700-4378
Service Bulletin #s 84 & 84A

MULTIPLEXERS

2211M Printer Multiplexer
Data Sheet; WL# 700-5224

2221M Printer Multiplexer
Data Sheet; WL# 700-4367

2230MXA/B Disk Multiplexer
Data Sheet; WL# 700-3740
Service Bulletin # 54.1
SNL # 110A, B, & C
CEA # 30

TELECOMMUNICATIONS:

Telecom. Self-Teaching Manual; CE Div. Publication #03-0078
Product Service Telecommunications Guide; CE Publication
Service Bulletin #77
Asynchronous I Manual (Marketing Publication); WL #700-4718
Telecom. Marketing Guide; WL #700-4412
Telecom. Sales Guide; WL #700-4703
Telecommunications Support Utilities User Manual; WL #700-4086
Telecom. Support Utilities User Manual Addendum; WL #700-4086-1
Teletype Emulator Data Sheet; WL #700-4704
Burroughs Emulator Data Sheet; WL #700-4705
2741 Emulator Data Sheet; WL #700-4706
HASP Multileaving Data Sheet; WL #700-4707
3741 Software Utilities Data Sheet; WL #700-4708
2780/3780 Software Utilities Data Sheet; WL #700-4709

2227B & 2227N
2227B Buffered Async. Telecommunications Data Sheet; WL #700-3830
2227B Buffered Async. Telecommunications User Manual; WL #700-4114
Service Bulletin #77

2228B & 2228N
2228B Bisynchronous Telecom. Data Sheet; WL #700-4143
Service Bulletin #77

TAPE

2209A

2209A 9-Track Tape Drive Data Sheet; WL #700-4261
2209A 9-Track Tape Drive User Manual; WL #700-4358
2209A 9-Track Tape Drive Utilities Manual; WL #700-4325
Kennedy Mod. 9100 Vacuum Column Tape Transport Manual
Kennedy Mod. 9219 Formatter Manual (OEM)
Service Bulletin #87
SNL #s 99, 104 & 107

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SECTION 1
SYSTEM-LEVEL GENERAL INFORMATION

1.1 INTRODUCTION

The Wang 2200 MVP is an interactive, multi-user, multi-task, disk-based computer system, utilizing fixed-partition user memory. The MVP Central Processor supports up to eight terminals and sixteen jobs (tasks) concurrently, and is programmable in Wang BASIC-2. The 2200MVP also supports a wide range of peripheral devices, such as printers, plotters, disk drives, tape drives, and telecommunications-interface devices.

The ablility of the 2200 MVP to handle multiple concurrent tasks is made possible through the use of simultaneous foreground (real-time, interactive) and background (batch, non-interactive) processing.

The total MVP system features the following hardware elements:

* A CENTRAL PROCESSING UNIT: One 2200MVP Central Processing Unit with 16K to 256K bytes of User Memory. If a system has extensive I/O requirements, a 2200MVP-A Central Processor Chassis is required.

* WORKSTATIONS: One to eight 2236D system display/keyboard consoles.

* DISK DRIVES: At least one disk drive (the "system disk") must be attached to the system. Disk drive units that may be attached to the system are the Wang 2270A-1D, 2270A-2D, 2270A-3D, all models of the 2260 disk drive, and all models of the 2280 (CDC Phoenix) disk drive.

* PRINTERS: At least one printer must be attached to the system. Printers that may be attached to the system are the 2221W, 2231W-1, 2231W-2, 2251, 2261W, 2263-1, 2263-2, 2271, and the 2281W.

* PLOTTERS: The 2272 Digital Drum Plotter, the 2232B Flatbed Plotter, and the 2282 Graphic CRT Plotter are presently the only Wang plotting devices that function with the MVP system.

* TAPE DEVICES: The 2209AV 9-track (Kennedy) tape drive (plus formatter unit) can be attached to the MVP system.

* TELECOMMUNICATION DEVICES: The 2227B and 2228B telecommunications controllers provide asynchronous (27B) and synchronous (28B) telecom-link capability for the MVP. Both controllers are supported by emulator software (Teletype Emulator, Burroughs Emulator, 2741 Emulator, HASP Multileaving Emulator, 3741 Emulator, 2780 Emulator, and 3780 Emulator.)

* TELETYPE-COMPATIBLE DEVICE CONTROLLERS: The 2227B Asynchronous Telecommunications controller (with Teletype emulator software) is used in conjunction with any RS-232-C/Teletype-compatible device.

* MULTIPLEXERS: The 2211M and 2221M Printer Multiplexers are supported by the 2200MVP system. The system also supports Disk Multiplexer 2230MXA/B.

See Figure 1-1 for an illustration of a typical 2200MVP System configuration. See Figures 1-2, -3, -4, and -5 for specific system cabling requirements.

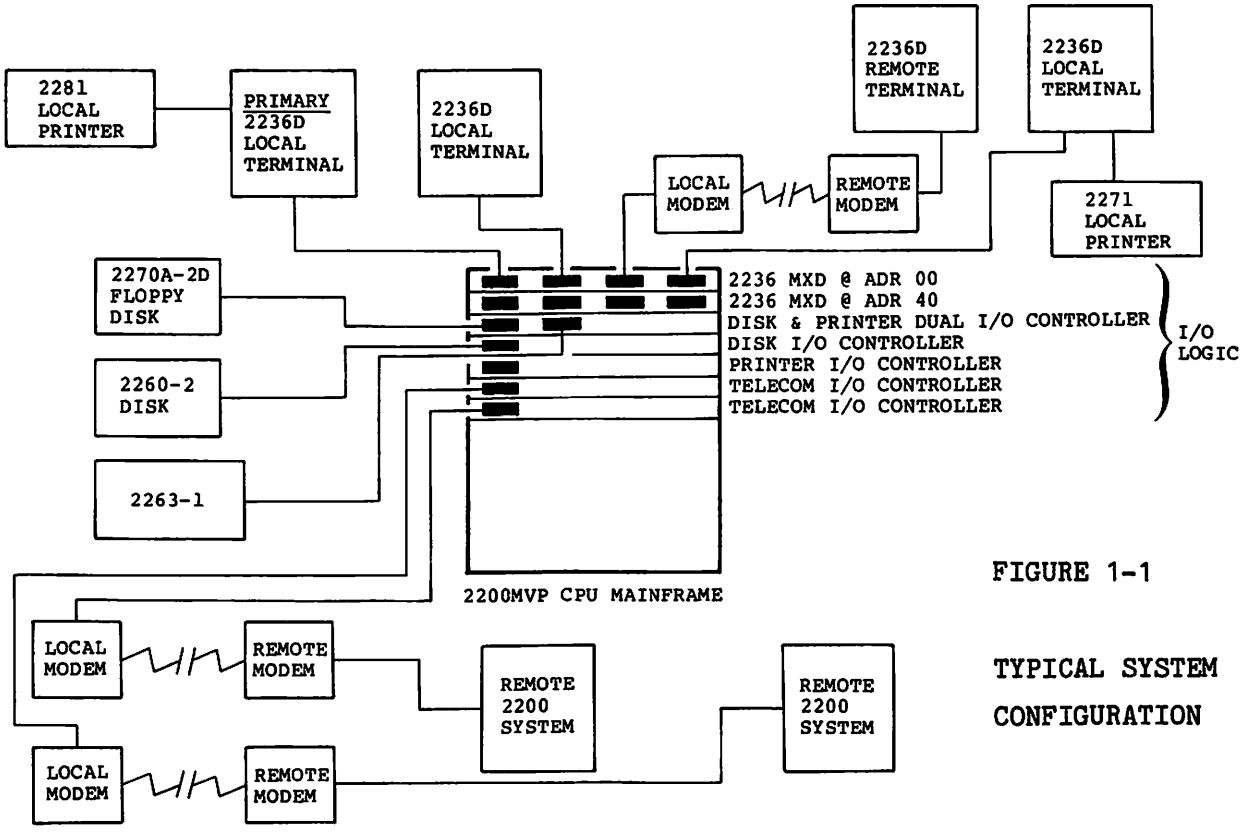


FIGURE 1-1

TYPICAL SYSTEM CONFIGURATION

FIGURE 1-2

PRINTER INTERFACE CABLES

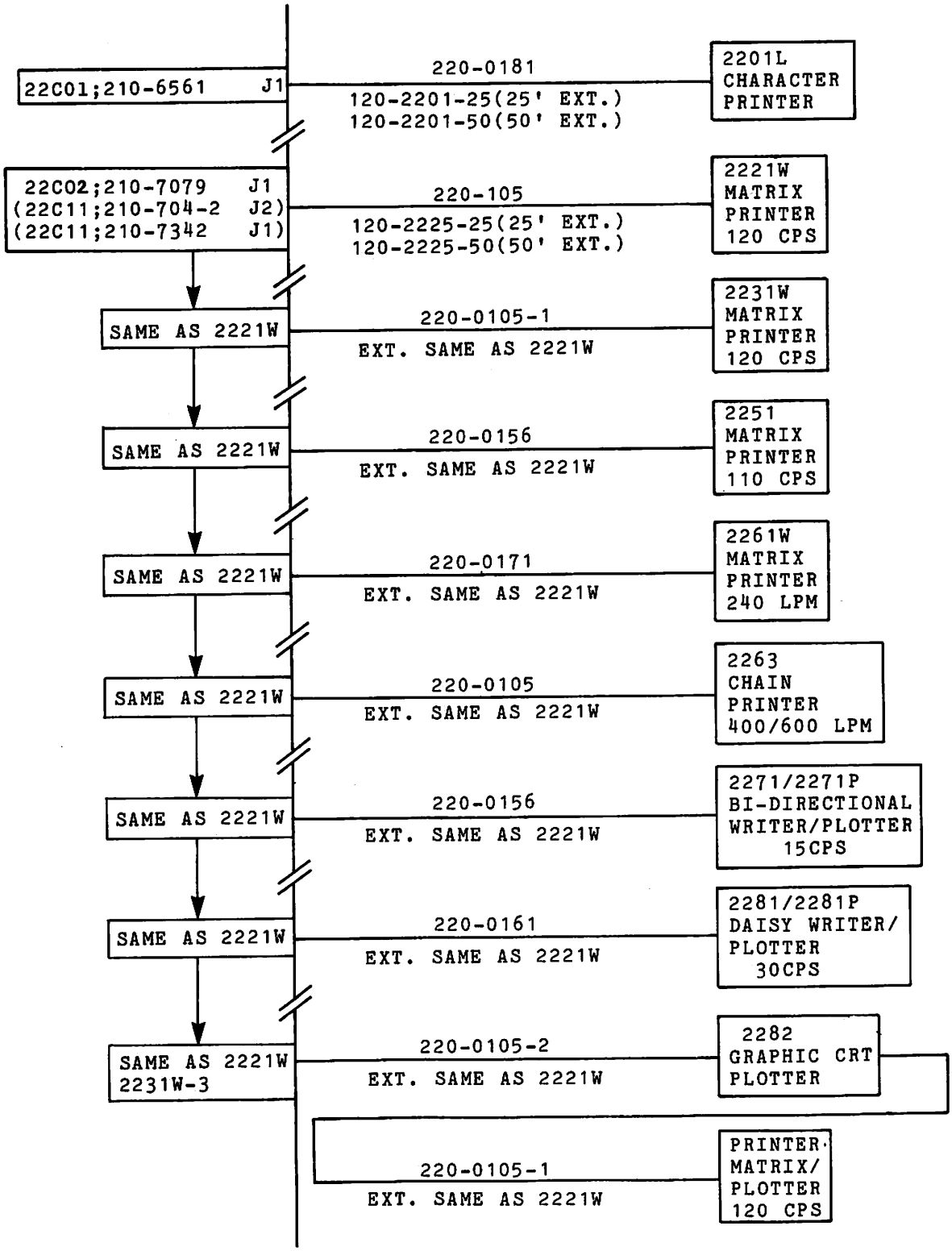


FIGURE 1-3

DISK INTEFACE CABLES

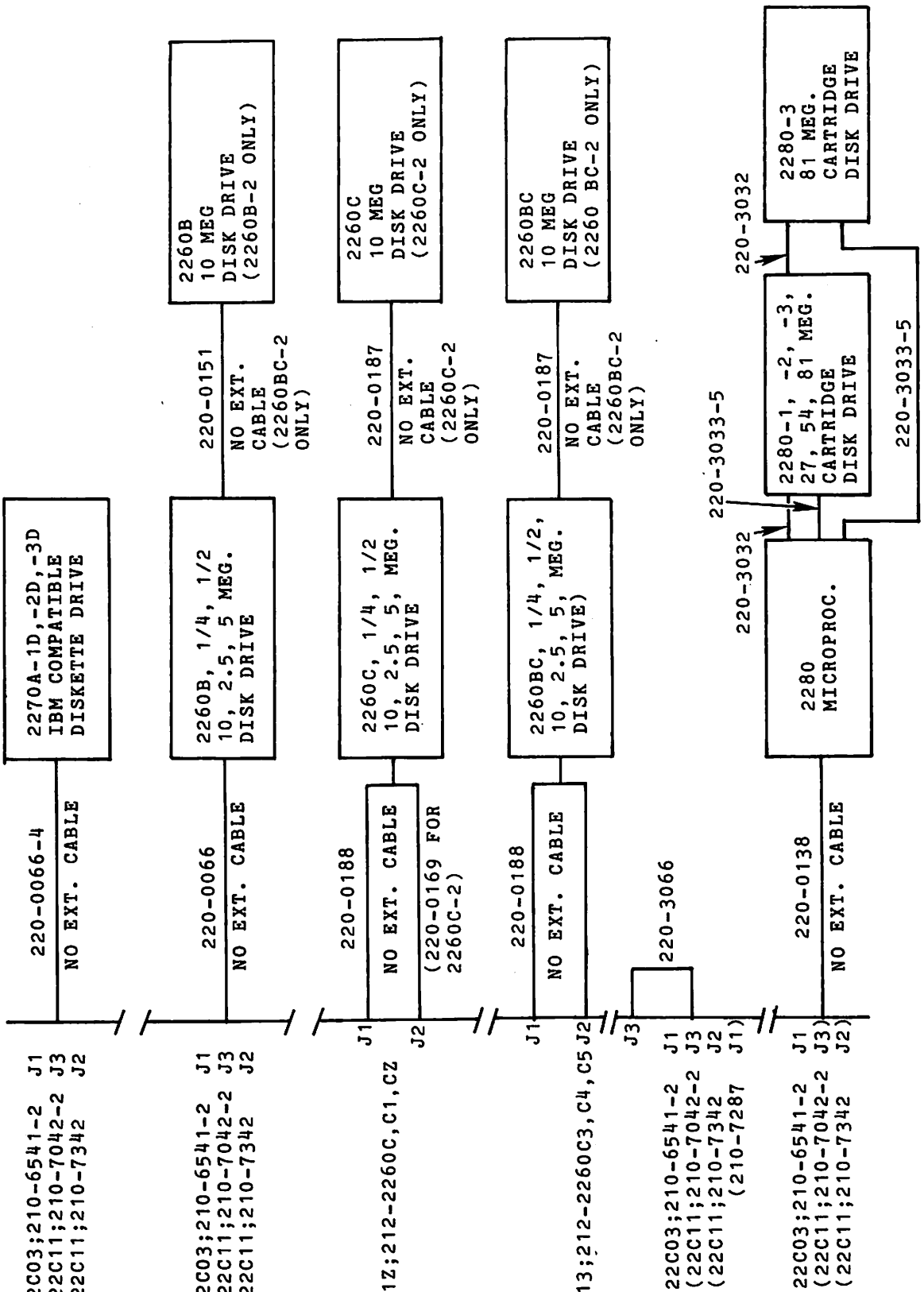


FIGURE 1-4

TELECOMMUNICATIONS, TAPE, PLOTTER, AND TERMINAL INTERFACE CABLES

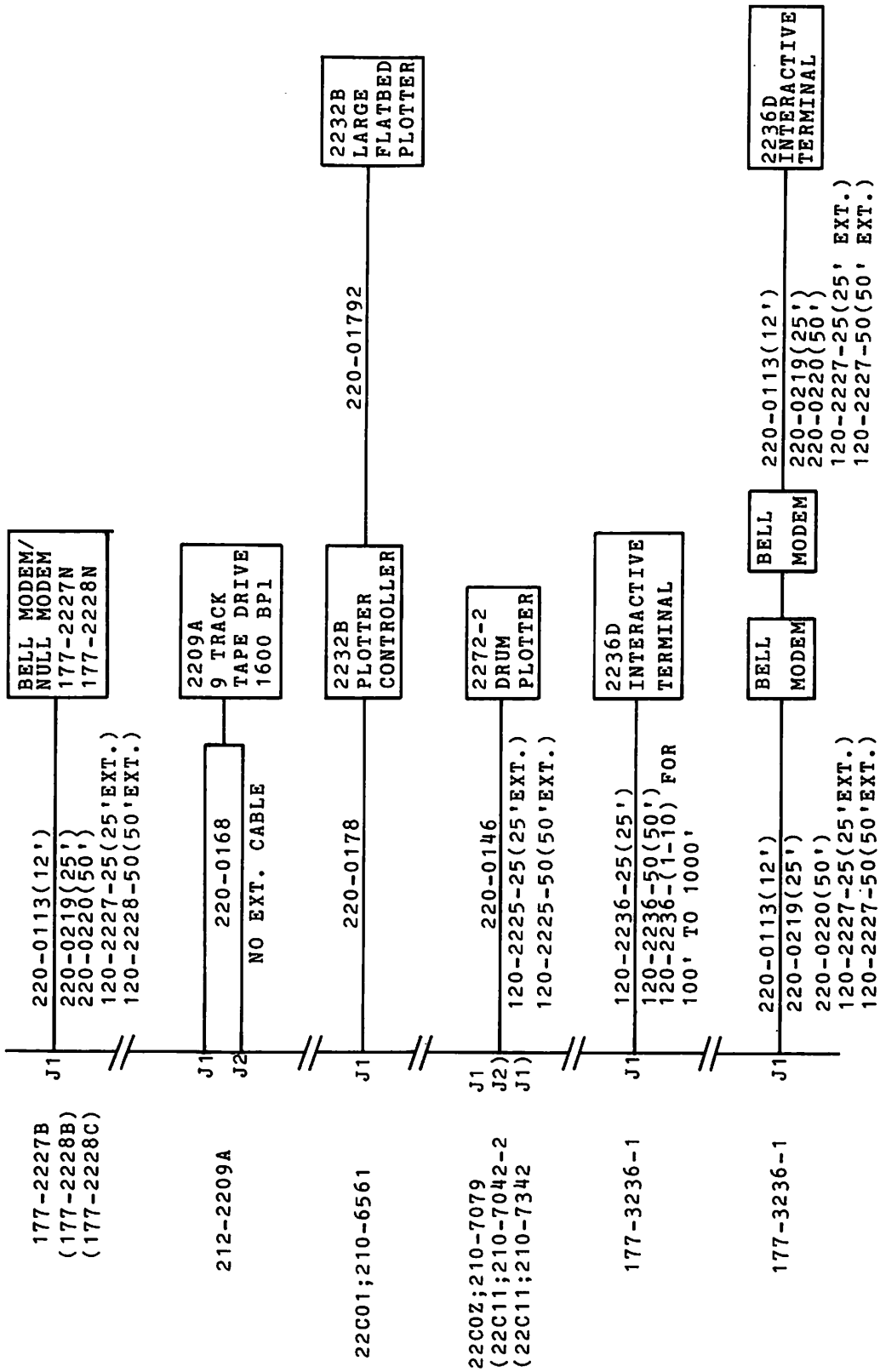
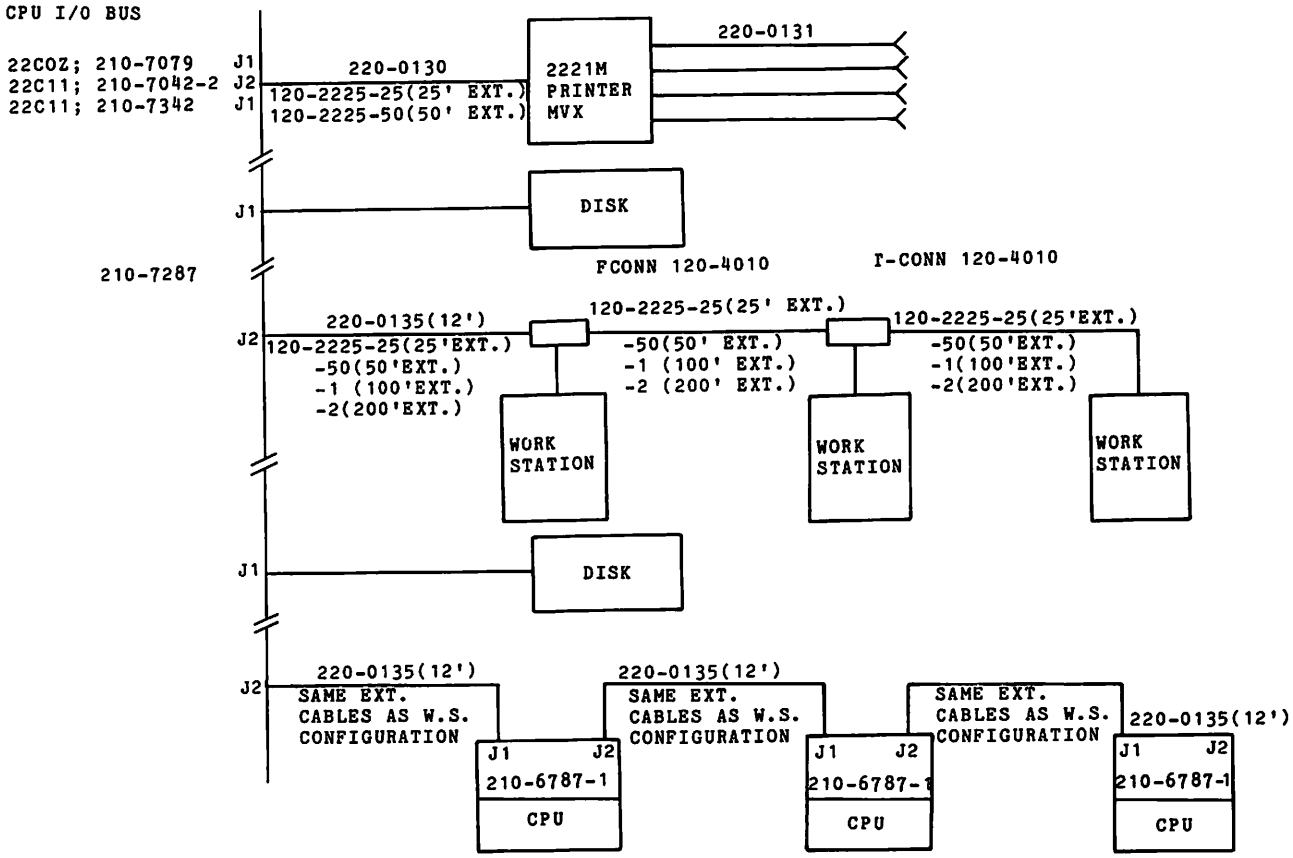


FIGURE 1-5

MULTIPLEXER INTERFACE CABLES



1.2 THE MVP CENTRAL PROCESSOR UNIT

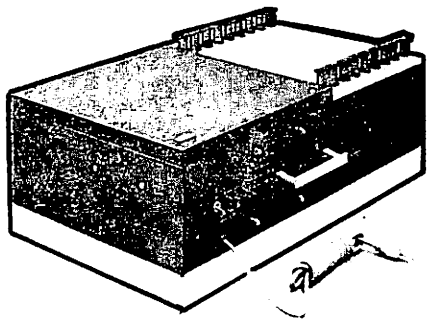


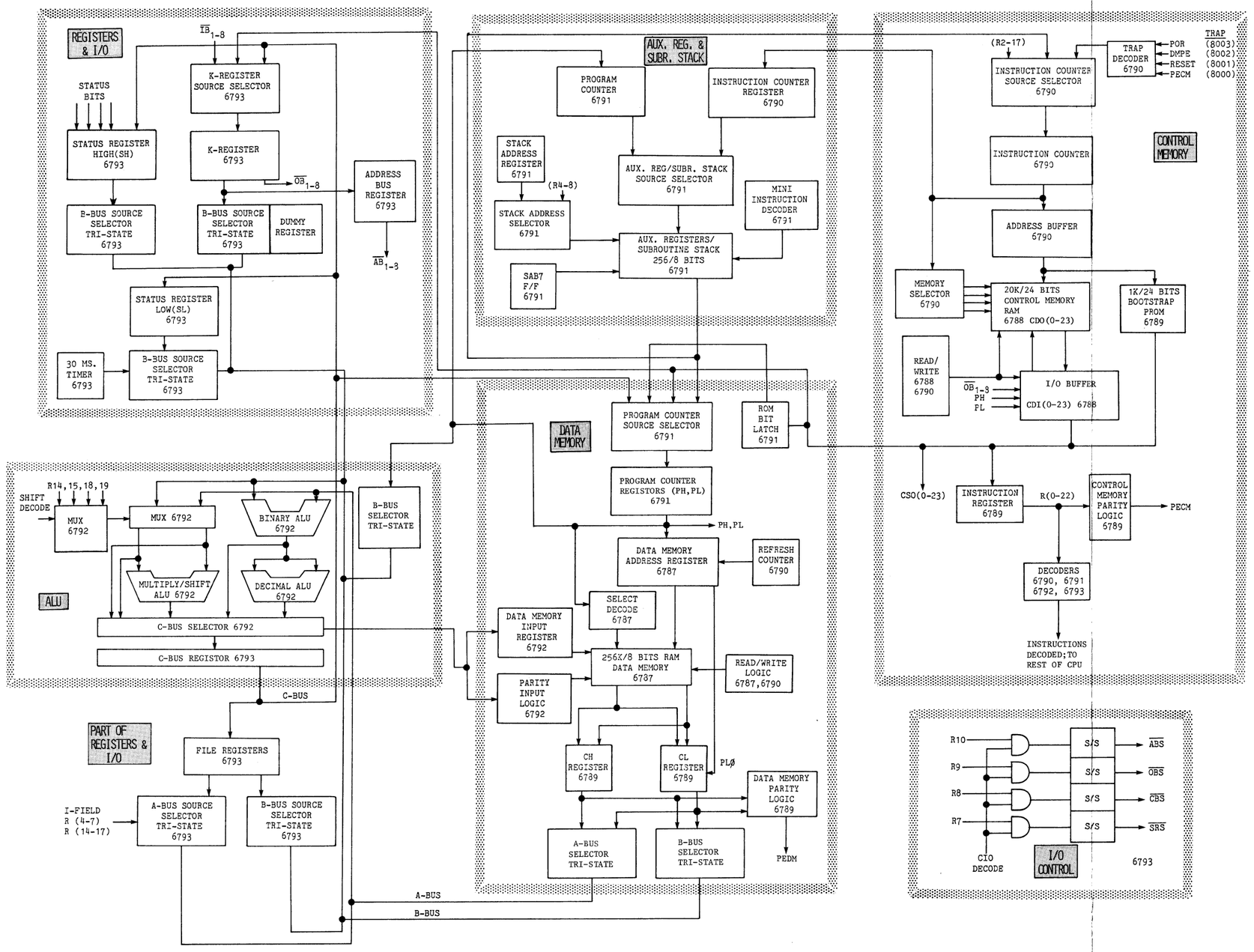
FIGURE 1-6

THE
2200MVP CPU

FIGURE 1-7

2200MVP CPU
BLOCK-LEVEL FUNCTION DIAGRAM

The MVP Central Processor contains a Bootstrap PROM (1K x 24 Bits), a three-section ALU (there is a binary section, a decimal section, and a multiply section in the MVP ALU), System Control logic, Memory-Control logic, a Control Memory (20K x 24bits), a Data ("User") Memory (from 16K to 256K x 8 bits), an I/O interface, and a Power Supply.



1.2.2 CONTROL MEMORY

The MVP Operating System occupies 20 Kilobytes of Control Memory microcode storage space. Control memory is used exclusively by the MVP Operating system and the BASIC-2 interpreter, and it cannot be accessed by a user or by user programs.

1.2.3 USER MEMORY

Explanation and description of the 2200MVP User Memory is combined in Section 5 of this publication.

1.2.4 DIFFERENCES BETWEEN THE 2200VP AND THE 2200MVP PROCESSOR

The MVP CPU is identical to the single-user 2200VP/2600 CPU, with two exceptions:

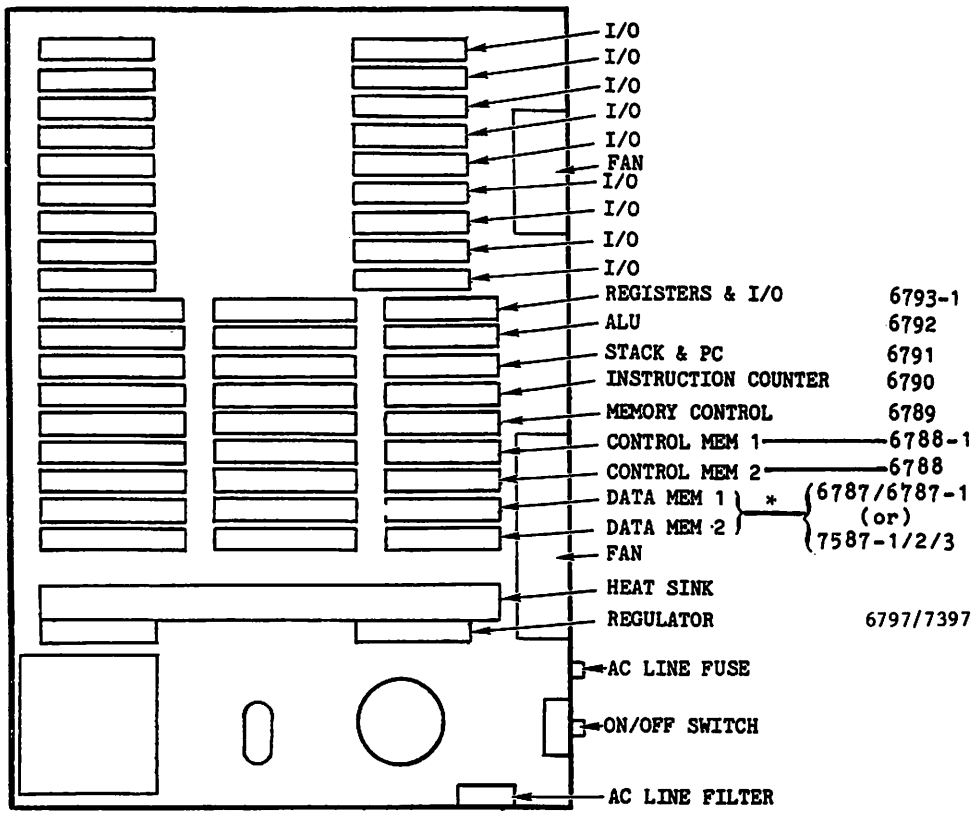
First, in order to load the more extensive MVP Operating System into the CPU, more Control Memory hardware was added to the VP's first 6788 Control Memory module. The first MVP Control Memory module, designated 6788-1, has an additional 4K of RAM for a total of 12 Kilobytes. Total system Control Memory (two Control Memory modules) is 20 Kilobytes.

The second change was made in the Registers and I/O module, 6793. A 6793-1 module was created with additional/modified hardware which allows multi-user capabilities.

1.2.5 INTERNAL LAYOUT OF THE 2200MVP MAINFRAME

Figures 1-8, 1-9, 1-10, and 1-11 show 2200 MVP chassis layout and RAM-loading options for Data (User) Memory and Control Memory.

FIGURE 1-8 2200MVP CPU LAYOUT



CAUTION: WHEN CHANGING CONTROL MEMORY OR DATA MEMORY BOARDS, MAKE SURE THAT CPU POWER IS OFF AND FAN HAS STOPPED.

6787 DATA (USER) MEMORY BOARD LOADING

DATA MEM BOARD SLOT	MEM SIZE 16K	16K INCREMENTS 32K	48K	64K
DATA MEMORY 1	6787	6787-1	6787-1	6787-1
DATA MEMORY 2	OPEN	OPEN	6787	6787-1

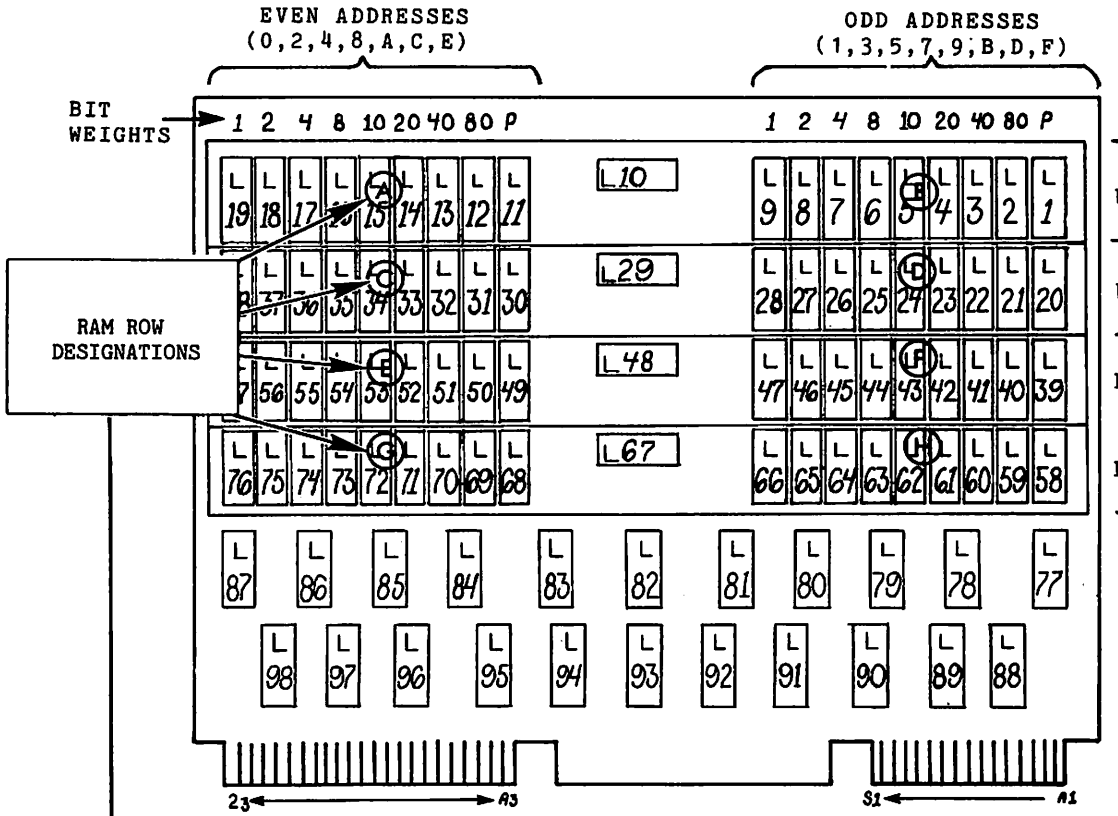
BANK #1
(SEE FIGURE 1-9 FOR DETAIL)

7587 DATA (USER) MEMORY BOARD LOADING

DATA MEM BOARD SLOT	MEM SIZE 64K	32K INCREMENTS 96K	128K	64K INCREMENTS 192K	256K
DATA MEMORY 1	7587-1	7587-2	7587-3	7587-3	7587-3
DATA MEMORY 2	OPEN	OPEN	OPEN	7587-1	7587-3

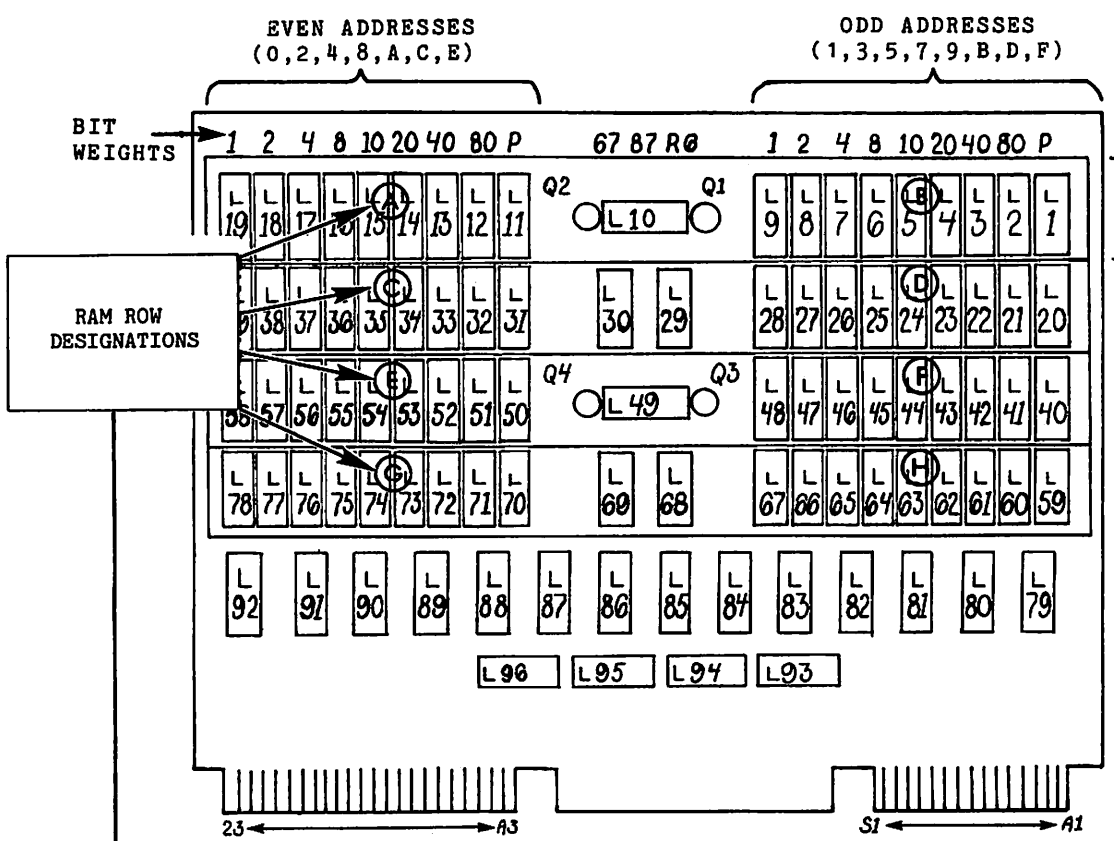
BANK #1 (SEE FIGURE 1-9 FOR DETAIL)
BANK #2 (SEE FIGURE 1-10 FOR DETAIL)
BANK #3
BANK #4

FIGURE 1-9 DATA MEMORY (6787) RAM LOADING



	WHEN LOADED IN DATA MEM. BOARD SLOT#2	WHEN LOADED IN DATA MEM. BOARD SLOT#1
LOCATIONS:	8000-FFFF (BANK #2)	8000-FFFF (BANK #4)
LOCATIONS:	0000-7FFF (BANK #2)	0000-7FFF (BANK #4)
LOCATIONS:	8000-FFFF (BANK #1)	8000-FFFF (BANK #3)
LOCATIONS:	0000-7FFF (BANK #1)	0000-7FFF (BANK #3)

BOARD NOMEN-CLATURE	ROWS LOADED WITH RAM ICs A	B	C	D	E	F	G	H	RAM SIZE:
6787					X	X	X	X	16K
6787-1	X	X	X	X	X	X	X	X	32K



HEX ADDRESS LOCATIONS & BANK NUMBERS

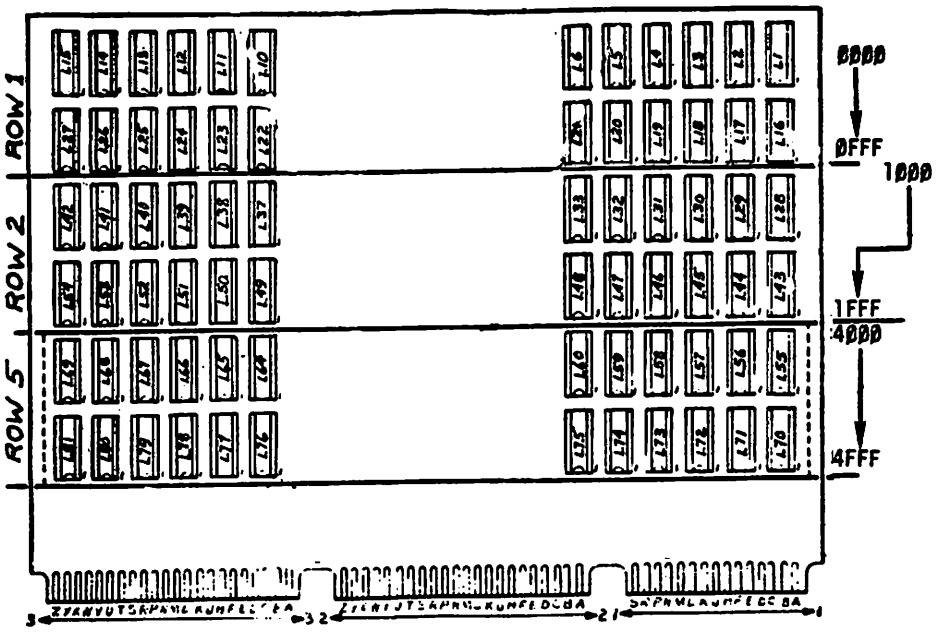
	WHEN LOADED IN DATA MEM. BOARD SLOT#1	WHEN LOADED IN DATA MEM. BOARD SLOT#2
LOCATIONS:	4000-5FFF (BANK #1)	COOO-DFFF (BANK #1)
LOCATIONS:	6000-7FFF (BANK #1)	EOOO-FFFF (BANK #1)
LOCATIONS:	0000-1FFF (BANK #1)	8000-9FFF BANK #1)
LOCATIONS:	2000-3FFF (BANK #1)	A000-BFFF (BANK #1)

BOARD NOMEN-CLATURE	ROWS LOADED WITH RAM ICs A	B	C	D	E	F	G	H	RAM SIZE
7587-1					X	X	X	X	64K
7587-2			X	X	X	X	X	X	96K
7587-3	X	X	X	X	X	X	X	X	128K

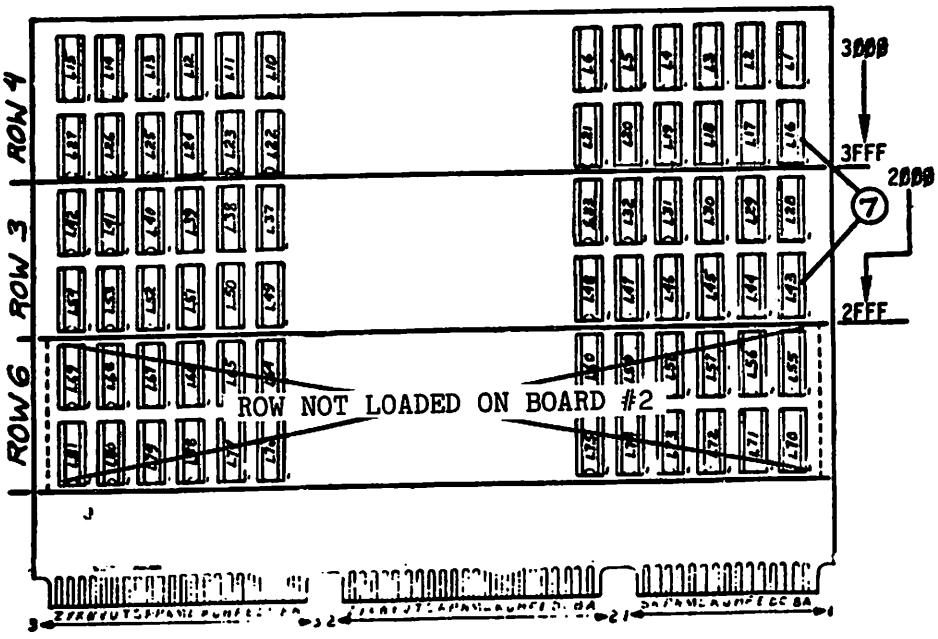
FIGURE 1-10 DATA MEMORY (7587) RAM LOADING

FIGURE 1-11

CONTROL MEMORY (6788) RAM LOADING



BOARD #1
6788-1



BOARD #2
6788

1.2.6 2200 MVP/MVP-A CPU SPECIFICATIONS

Subroutine Stacking:

96 levels

Precision:

13 digits standard (variable)

Maximum Data Rate:

100,000 bytes/sec

Memory Size:

16K bytes (standard). Expandable to a maximum of 256K bytes in 64K increments.

I/O Provisions:

9 I/O Ports

Operating Temperature:

50°F to 90°F (65°F to 75°F recommended)

Operating Humidity:

20% to 80% Relative humidity, non-condensing
(35% R.H. to 65% R.H. recommended)

Power Requirements:

Voltage 115 VAC ± 10%, 50 or 60 Hz ± 1 Hz
230 VAC ± 10%, 50 or 60 Hz ± 1 Hz

Power (MVP) 230 Watts (782 BTU/hr.)
(MVP-A) Specs. not available
@ date of printing

MVP Fuses 3 AMP @ 115V
1.5 AMP @ 230V

MVP-A Fuses Specs. not available
@ date of printing

Dimensions:

Height . . . . . 12.1 in. (30.7 cm)
Width . . . . . 14.5 in. (36.8 cm)
Depth . . . . . 21 in. (53.3 cm)

Shipping Weight

MVP 47 lb (21 kg)
MVP-A Specs. not available
@ date of printing

1.3 2236D INTERACTIVE TERMINAL

FIGURE 1-12

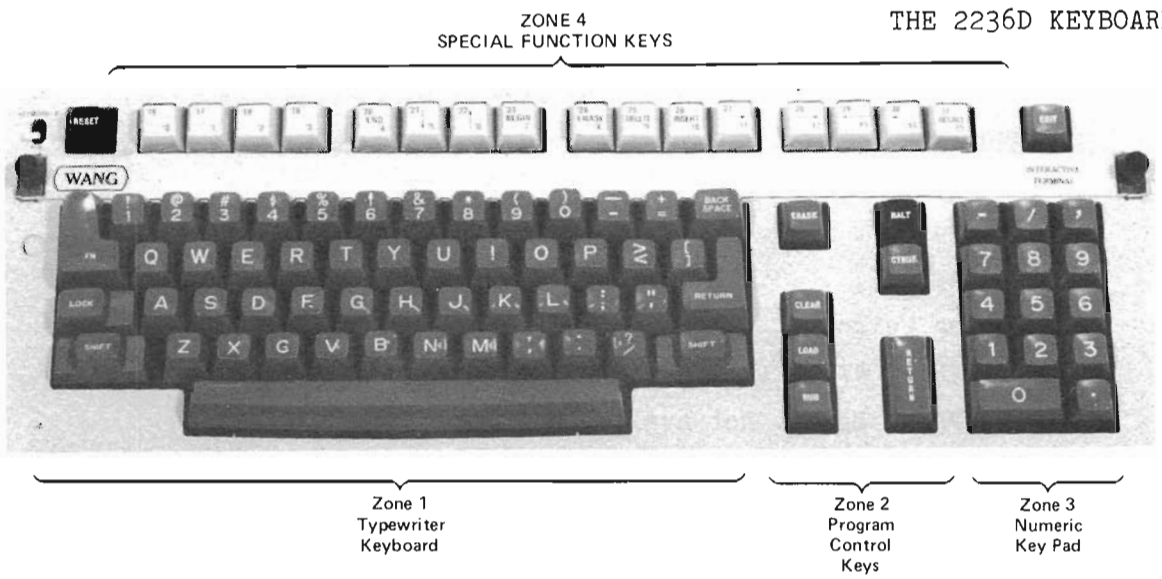
THE 2236D INTERACTIVE TERMINAL

1.3.1 GENERAL

The 12-inch (diagonal screen measure) display and typewriter-like keyboard are the principle devices of communication (interaction) between the user and the system. Up to 1,920 upper/lower case characters can be displayed in 24 lines (80 characters per line) with full cursor control. A programmable audio alarm is provided which indicates the occurrence of certain errors and other machine conditions. Screen brightness and contrast are adjustable from the front panel of the terminal. A character underscore feature is incorporated for the purpose of highlighting portions of display.

1.3.2 THE KEYBOARD

FIGURE 1-13
THE 2236D KEYBOARD



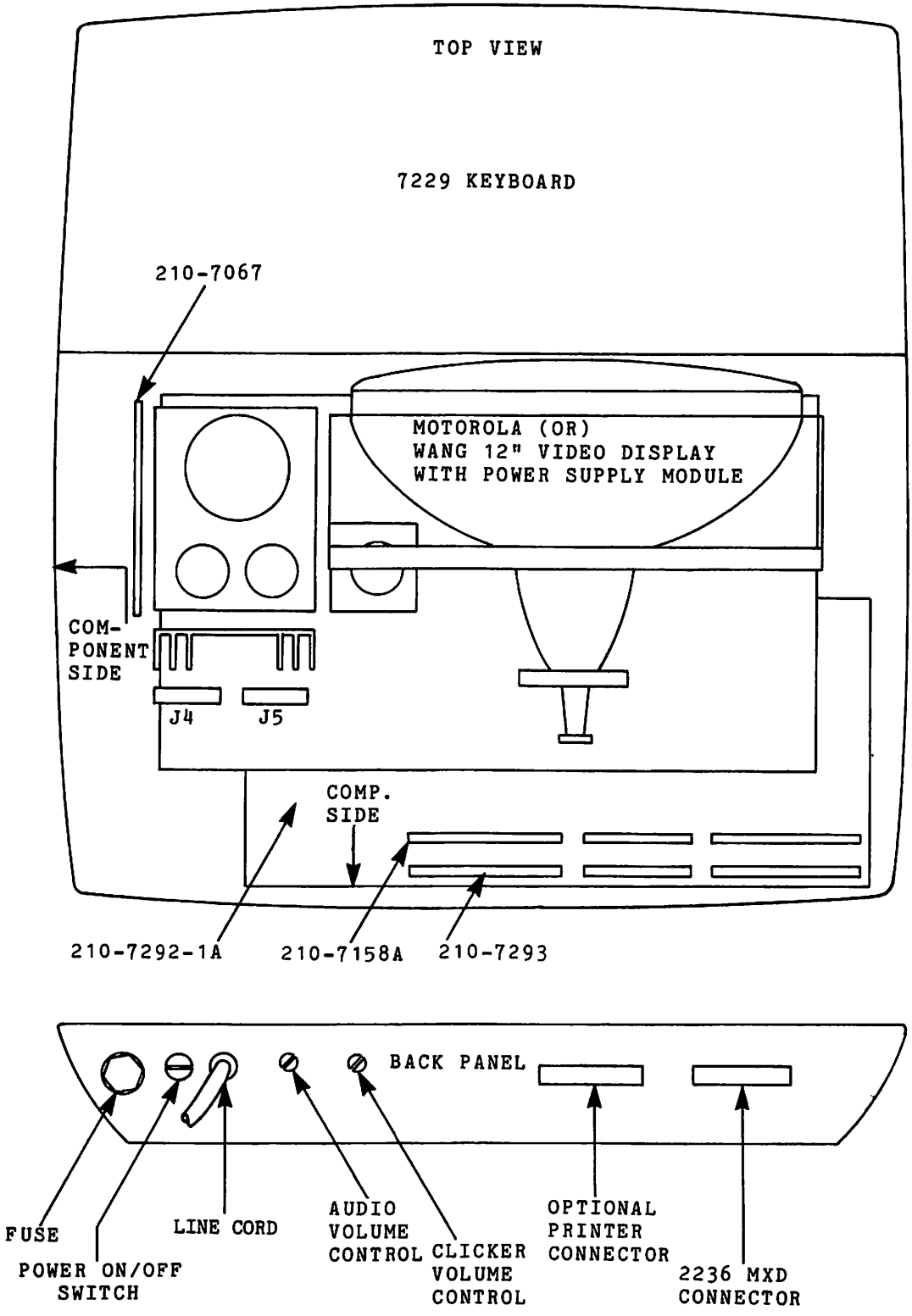
This unit has a standard typewriter character key arrangement, several program control keys, and a 10-key numeric keypad. The keyboard permits an operator to enter data, write programs, perform calculations, and issue special commands to the central processor. An internal "clicker" device provides audio verification when a key is activated. Other elements of keyboard hardware prevent errors caused by pressing more than one key at a time, and errors of inadvertent multiple key entry ("keybounce").

The keyboard has two modes of operation, selected by means of a toggle switch labeled "A/A" and "A/a" at the upper left corner of the keyboard. In the A/A mode, alphabetic characters are produced in uppercase, whether "shifted" or "unshifted". "Shifted" numerics produce symbols and special characters. In the A/a mode, the keyboard produces standard U/L-case typewriter characters. Whenever the Shift key is depressed, the Shift indicator lamp illuminates. In addition to the standard typewriter-like keyboard and numeric pad, the Model 2236 contains a system-commands key area, and 32 user-definable special functions keys. The special function keys also access Edit-mode functions for changing data or lines of program text. (Note: Keyboard operations are detailed in the 2236D Reference Manual: WL# 700-4405 and the 2200 MVP BASIC-2 Reference Manual: WL# 700-4080.)

The RESET button, located to the right of the Mode switch, immediately stops program execution, listing, and I/O operations. RESET also clears the CRT, homes the cursor, signals READY and returns control to the console user (Console Input Mode). RESET is a "last resort" means of terminating program execution and generally should not be used to that end.

1.3.3 INTERNAL LAYOUT OF THE 2236D INTERACTIVE TERMINAL

FIGURE 1-14 2236D INTERNAL LAYOUT



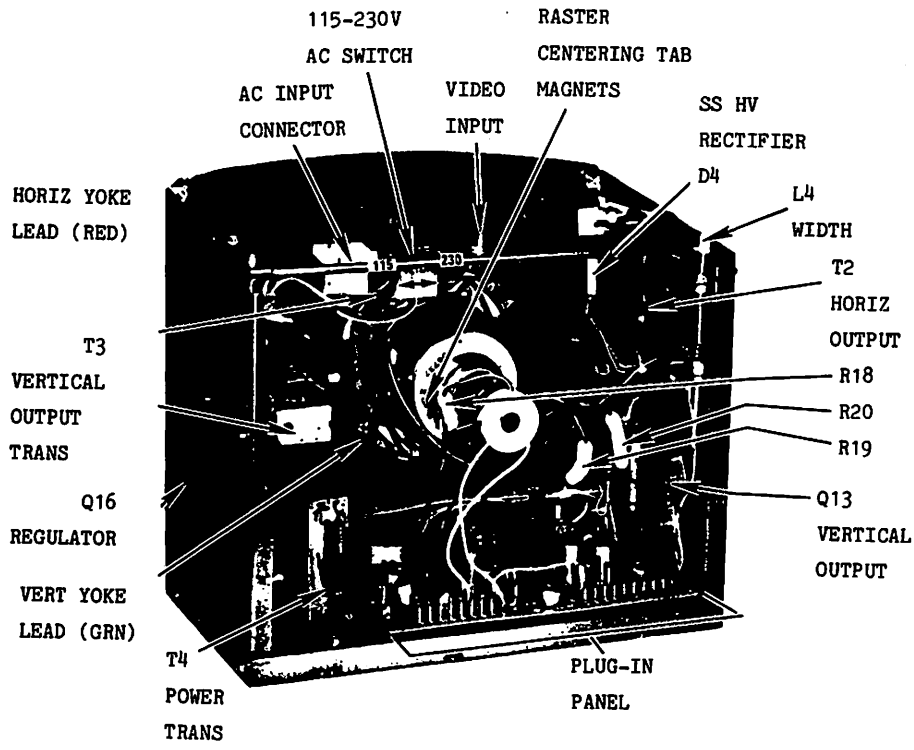


FIGURE 1-15 THE MOTOROLA DISPLAY UNIT

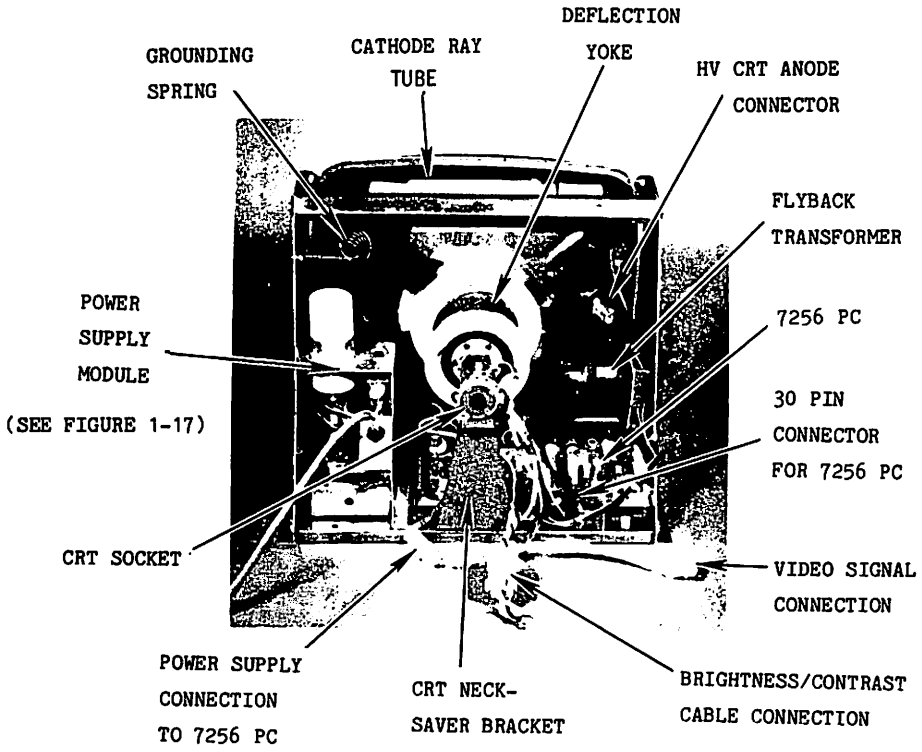
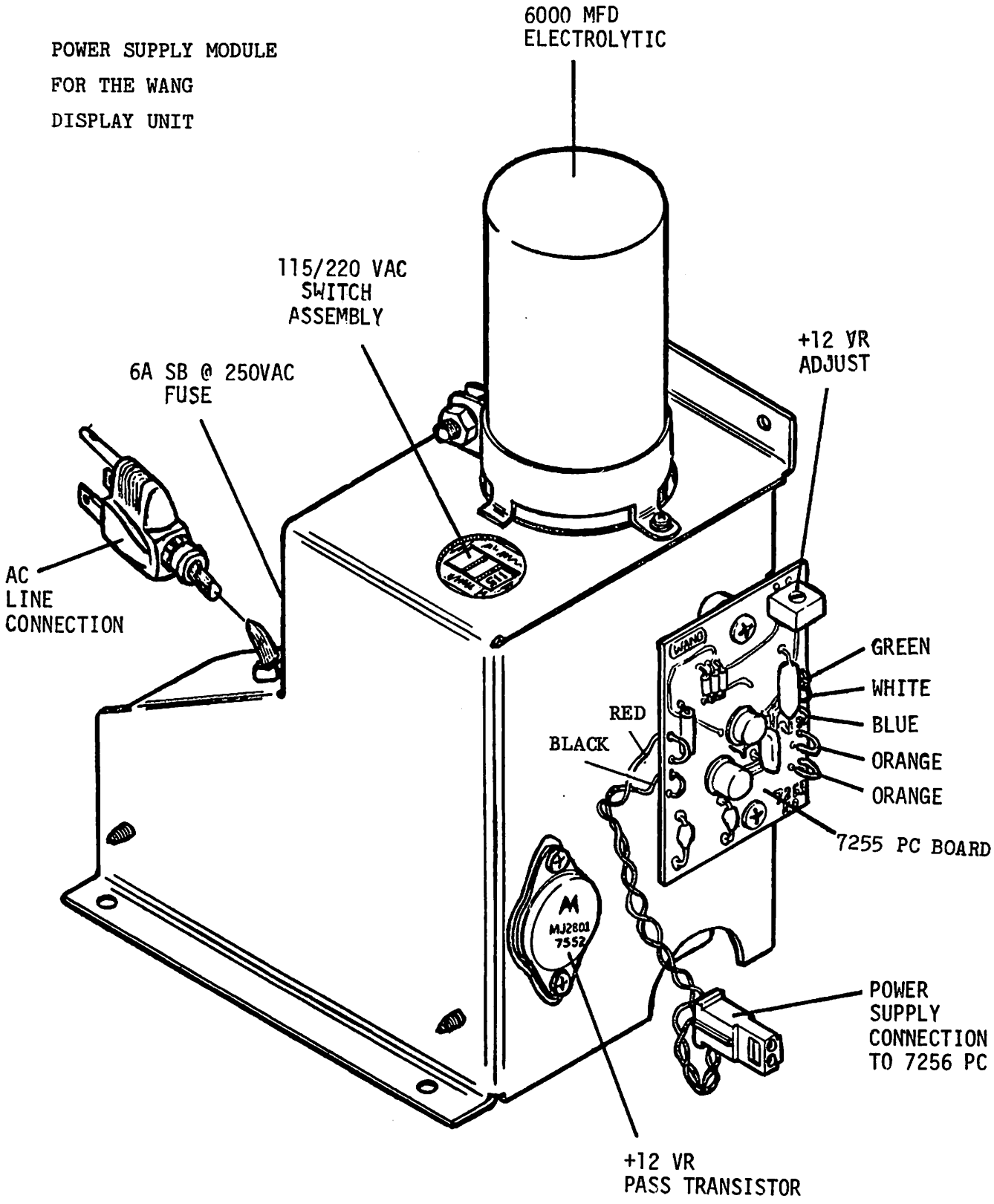


FIGURE 1-16 THE WANG DISPLAY UNIT

FIGURE 1-17

POWER SUPPLY MODULE
FOR THE WANG
DISPLAY UNIT



1.3.4 2236D INTERACTIVE TERMINAL SPECIFICATIONS

Size:	Height	13 1/2 in. (34.3 cm)
	Depth	20 1/2 in. (52 cm)
	Width	19 3/4 in. (50.2 cm)

Weight: 51 lb (23.1 kg)

CRT Screen:	Display Size	12 in. diagonal (30.4 cm)
	Capacity	24 lines, 80 characters/line
	Character size	
	Height	0.16 in. (0.41 cm)
	Width	0.09 in. (0.23 cm)
	Character Set	112 diaplayable "graphic" characters, with or without underline, including upper- and lowercase letters.

Keyboard: Typewriter Keyboard cable of generating 88 different ASCII graphic characters including upper and lowercase letters. A convenient Numeric Keypad, several Program Control Keys, a general function (FN) key, and 16 Special Function Keys are also included.

Power Requirements: 115 or 230 VAC $\pm$ 10%
50 or 60 Hz $\pm$ 1/2 Hz
40 Watts

Fuses: 2 amp @ 115V/60 Hz
1 amp @ 230V/50 Hz

Operating Environment: 50°F to 90°F (10°C to 32°C)
20% to 80% relative humidity, allowable
35% to 65% relative humidity, recommended

Cable: One 8-foot (2.4m) cord is provided for the connection of the terminal to an AC outlet. One 25-foot (7.6m) direct-connection Terminal-to -I/O Controller) cable is provided with each Model 2236D, unless an optional direct connection cable is ordered for that terminal. All direct connection cables have male plugs at each end and thus are not extendable. Cables are optionally available in lengths of 25 feet (7.6m), 50 ft. (15.2m), 100 ft. (30.5m), and thereafter in increments of 100 ft. (30.48m) up to 1000 ft. (304.8m). Direct-connection cable is shielded.

Modem cables are optionally available in lengths of 12 feet (3.7m), with additional extensions of 25 ft. (7.6m) and 50 ft. (15.2m); however, the combined cable distance from Wang equipment to its modem is 50 ft. (15.2m) maximum according to EIA standards.

Operating Environment: Same as 2200MVP CPU.

Communication Modes: Full-Duplex Asynchonous Wang mode for Model 2236D Interactive Terminals.
Full-Duplex Asynchronous Teletype mode for non-Wang, RS-232-C compatible, Teleype-equivalent terminals.

Transmission Rates: 300, 600, 1200, 2400, 4800, 9600, or 19,200 baud.

Asynchronous Communication
Character Format Options:

Parity: odd, even, or none.
Number of Data Bits: 5, 6, 7, or 8.
Number of Stop Bits: 1, 1.5, or 2.
One Start bit (standard).

Non-Wang Terminal Requirements:	An RS-232-C-compatible, Teletype-equivalent terminal must have a 25-pin RS-232-C compatible plug, must communicate at one of the Multiplex Controller transmission rates, and must use one of the Multiplex Controller's software-selectable asynchronous communication character formats. A non-Wang terminal may use the same cable as an Interactive Terminal.

1.4 THE CPU I/O CONTROLLERS

The CPU has nine I/O ports. Each peripheral device is connected to a controller board which plugs into one CPU I/O Port. Some controllers incorporate "front end" intelligence (firmware) which allows the controller to perform I/O processing independently while the CPU simultaneously does applications and Operating System processing.

The following I/O controllers are used in the 2200MVP System:

PERIPHERAL MODEL # AND DESCRIPTION:	CPU I/O CONTROLLER: MODEL # AND DESCRIPTION	CONTROLLER: COMPLETED ASSEMBLY #	CONTROLLER: COMPOSITE ASSEMBLY #'s
2201L Character Printer	22C02 Printer Cntrlr. 22C11 Printer/Disk Controller	WL#210-7079 WL#210-7042-2* WL#210-7342**	Not Applicable Not Applicable
2209AV Nine-Track Tape (1600 BPI-PE)	2209A Controller	WL#212-2209-A	WL#210-7141 (MB) WL#210-7142-A (DB)
2221W Matrix Line Printer (132 col/200 CPS)	22C02 Printer Cntrlr 22C11 Printer/Disk Controller	WL#210-7079 WL#210-7042-2* WL#210-7342**	Not Applicable Not Applicable
2227B Buffered Asynchronous Communications Controller	2227B	WL#212-2227-B	WL#210-6723 (MB)* WL#210-6730 (DB)* WL#210-7223-A(MB)** WL#210-6730 (DB)**
2227N Null Modem for 2227B Controller	Not Applicable	Not Applicable	Not Applicable
2228B Binary Synchronous Communications Controller	2228B Binary Synch. Comm. Controller	WL#177-2228-B	WL#210-7223-A (MB) WL#210-7224 (DB)
2228C Binary Synchronous Communications Controller	2228C Binary Synch. Comm. Controller	WL#177-2228-C	WL#210-7223-C (MB) WL#210-7224-A (DB)
2228N Null Modem for 2228B/C Controllers	Not Applicable	Not Applicable	Not Applicable
2230MXA-1 Master Daisy-Chain Disk Mux Controller	2230MXA-1 Master Dsy-Chain Disk Mux Cntrlr	WL#187-2225-A1	WL#210-7287
2230MXB-1 Slave Daisy-Chain Disk Mux Controller	2230MXB-1 Slave Dsy-Chain Disk Mux Cntrlr	WL#187-2225-B1	WL#210-6786-1

* Earlier Version
** Newer Version

PERIPHERAL MODEL # AND DESCRIPTION:	CPU I/O CONTROLLER: MODEL # AND DESCRIPTION	CONTROLLER: COMPLETED ASSEMBLY #	CONTROLLER: COMPOSITE ASSEMBLY #'s
2231W-1,-2, -6 Matrix Line Printers (W-1: 112 col, 120 cps; W-2: 132 col, 120 cps; W-6: 132 col, 70 cps, high-density characters)	22C02 Printer Cntrlr	WL#210-7079	Not Applicable
	22C11 Printer/Disk Controller	WL#210-7042-2* WL#210-7342**	Not Applicable
2231W-3 Aux. Printer for the 2282	22C02 Printer Cntrlr	WL#210-7079	Not Applicable
2232B Flatbed Plotter	22C01 Plotter Cntrlr	WL#210-6561	Not Applicable
2236D Interactive Terminal	2236MXD**	WL#177-3236-1	WL#210-7290-1 (MB) WL#210-7291 (DB)
2251 Matrix Line Printer (40 col/110 CPS)	22C02 Printer Cntrlr	WL#210-7079	Not Applicable
	22C11 Printer/Disk Controller	WL#210-7042-2* WL#210-7342**	Not Applicable
2260BC & 2260C F/R Disk Drives (2.5, 5, 10 or 20 megabytes)	22C12 for 2.5 Meg: for 5.0 Meg: for 10 Meg: for 20 Meg:	WL#212-2260-C2 WL#212-2260-C1 WL#212-2260-C WL#212-2260-C	WL#210-7487-C (DB) WL#210-7487-B (DB) WL#210-7487-A (DB) WL#210-7487-A (DB) WL#210-7486 (MB for all)
	22C13 for 2.5 Meg: for 5.0 Meg: for 10 Meg: for 20 Meg:	WL#212-2260-C5 WL#212-2260-C4 WL#212-2260-C3 WL#212-2260-C3	WL#210-7487-C (DB) WL#210-7487-B (DB) WL#210-7487-A (DB) WL#210-7487-A (DB) WL#210-7488 (MB for all)
2261W Matrix Line Printer 240 LPM	22C02 Printer Cntrlr	WL#210-7079	Not Applicable
	22C11 Printer/Disk Controller	WL#210-7042-2* WL#210-7342**	Not Applicable

* Earlier Version
** Newer Version

PERIPHERAL MODEL # AND DESCRIPTION:	CPU I/O CONTROLLER: MODEL # AND DESCRIPTION	CONTROLLER: COMPLETED ASSEMBLY #	CONTROLLER: COMPOSITE ASSEMBLY #'s
2263-1,-2 Chain Line Printers 400 and 600 LPM	22C02 Printer Cntrlr	WL#210-7079	Not Applicable
	22C11 Printer/Disk Controller	WL#210-7042-2* WL#210-7342**	Not Applicable
2270A-1D,-2D,-3D Wang IBM 3740-Compatible Diskette Drive (.25, .50, & .75 megabytes)	22C03 Floppy Cntrlr	WL#210-6541-2	Not Applicable
2271 Bidirectional Output Writer (15 CPS) and 600 LPM	22C02 Printer Cntrlr	WL#210-7079	Not Applicable
	22C11 Printer/Disk Controller	WL#210-7042-2* WL#210-7342**	Not Applicable
2272-2 Triple Pen Drum Plotter	22C02 Matrix Printer Controller	WL#210-7079	Not Applicable
2280-1,2, & 3 Fixed/Removable Disk Drive (CDC Phoenix)	22C03 Disk Controller	WL#210-6541-2	Not Applicable
2281 Daisy Output Writer (30 CPS)	22C02 Printer Cntrlr	WL#210-7079	Not Applicable
2281P Daisy Plotting Output Writer (30 CPS)	22C02 Printer Cntrlr	WL#210-7079	Not Applicable
2282 Graphic CRT Plotter	22C02 Printer Cntrlr	WL#210-7079	Not Applicable

* Earlier Version
** Newer Version

1.4.1 THE 2236MXD CONTROLLER

Each 2236D Terminal is connected to a 2236MXD Multiplexer/Controller, which in turn simultaneously handles hardcopy (data for printout), operator key entry, and screen displays. The multiplexer/controller collects keystrokes into lines of text, and contends with speed discrepancies between the asynchronous signal line, the display, and local printers. With the controller managing these tasks, the CPU is free--under the control of the Operating System--to execute a program in each partition and to monitor the operations of other terminals and system peripherals.

A single 2236MXD controller occupies one I/O port in the CPU and can support up to four Model 2236D terminals. A maximum of two 2236MXD controllers can be installed in a 2200MVP CPU, so that up to eight terminals may be accommodated in a single system.

Communication between the MXD controller and each 2236D Terminal is asynchronous full-duplex, with line speeds selectable from 300 to 19,200 baud. A terminal can be connected to a controller locally at distances of up to 2000 feet via direct cabling, or the terminal can be located in more remote locations using a telecommunications link. Such flexibility is possible, due to the fact that 2236 MXD controllers and 2236D Interactive Terminals are compatible to the EIA RS-232-C and CCITTV.24 standards for telecommunications.

Any combination of local, extended local, and remote connection may be used. However, the 2236D Terminal connected to port #1 of the first MXD controller should be positioned relatively close to the CPU because it acts as the "system console" for "Master Initialization" whenever the system is powered up. Allowable configurations of the terminal relative to the CPU (and MXD controller) are as follows:

a) LOCAL - for distances up to 25 ft. (7.6 m) transmission rates of 19,200 baud are available with direct four-wire conection, using a Wang-supplied cable. (<u>This is the standard configuration</u>).

b) EXTENDED LOCAL - for distances from 25 ft. to 2000 ft. (610m) optional cables in up to 100 ft. (30.5m) increments provide direct extended local connection at speeds of up to 19,200 baud.

c) REMOTE - for distances greater than 2000 ft., asynchronous full-duplex, RS232C-compatible modems must be used to provide the communication link.

Distances up to 5 miles (8km): short-haul modems using private 4-wire connection between modems may be employed.

Distances exceeding 5 miles: telephone lines provide the dial-up connection between two modems.

Specifically, communication speeds of 300, 600, 1200, 2400, 4800, 9600, and 19,200 baud are supported by the 2236MXD controller. There are four switch banks (one for each port on the MXD controller), each bank having six switches corresponding to the 300-9600 baud rate selections; the 19,200 baud rate selection requires additional hardware changes. A 2236D terminal and its associated 2236MXD I/O port must have identical baud rate selections. Optional cables for modem connections to Wang equipment are available in 12 ft. (3.7m), 25 ft. (7.6m), and 50 ft. (15.2m) lengths. The local and remote modem(s) must also be set to the same baud rate as the terminal and controller.

1.5 THE SYSTEM DISK

The 2200 MVP Operating System and BASIC-2 interpreter are contained on a system diskette. The contents of the system diskette can only be loaded from a 2270A-D Diskette Drive into Control Memory after the system is powered up and Master Initialized.

1.6 SYSTEM EXPANDABILITY

The 2200 MVP will not support certain unbuffered and time-dependent devices, certain telecommunications and instrument interfaces, the Model 2209 9-track 800 BPI tape drive, 2226 consoles, 2202 and 2212 plotters, and the 2224 Multiplexer Controller.

1.7 PERIPHERAL DESCRIPTIONS

FIGURE 1-18

The Model 2201L Output Writer is a modified IBM Selectric II. This unit types, with full format control, numeric and upper/lowercase alphabetic output from the System 2200.

FIGURE 1-19

The Model 2209A 1600 BPI Nine-Track Magnetic Tape Drive provides the capability to store programs and data on half-inch IBM-compatible tapes. A ten-inch diameter reel can accommodate up to 20 megabytes of information.

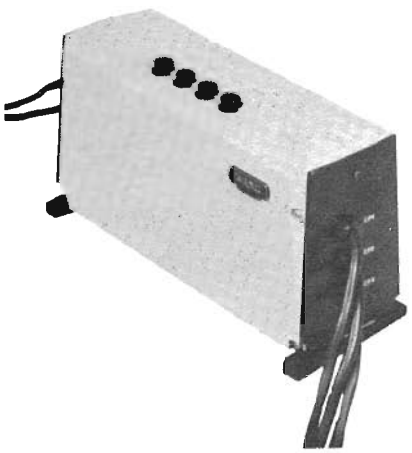


FIGURE 1-20

The 2211M and the 2221M Printer Multiplexers allow up to four 2200 CPUs to share a single printer. Manual selection of one CPU connected to the multiplexer mutually excludes other CPUs connected to the mux.

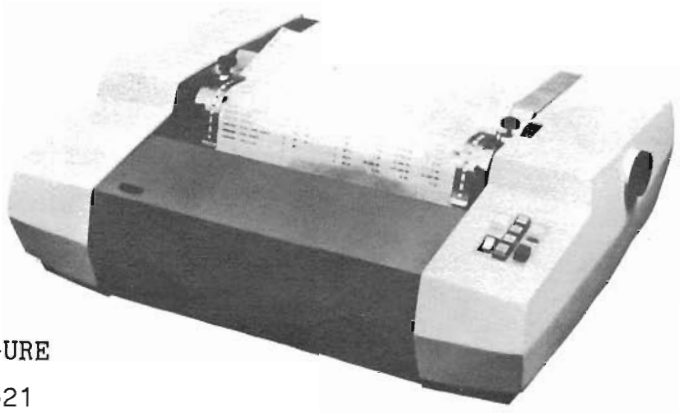


FIGURE
1-21

The 2221W Dot Matrix Impact Printer (132-column), hardcopy output is 200 characters per second and 65-300 lines per minute, depending on line length.

FIGURE
1-22

(No Photograph available)

The Model 2227B Asynchronous Telecommunications Controller allows local or remote asynchronous communication between two System 2200's or, with the aid of software emulators, remote telecommunications with "foreign" CPUs (IBM, Univac, Honeywell, etc.). The MVP system becomes an "intelligent terminal" with the Model 2227B.

Through a 2227N Null Modem, two 2200MVP CPU's equipped with identical 2227B controllers set to the same baud rates may have direct local asynchronous communications.

FIGURE
1-23

The Model 2228B and 2228C Binary Synchronous Telecommunications Controllers, when accompanied by a suitable modem and an emulator program, enables the 2200MVP system to transmit and receive data over dial-up communications lines to another remotely-located, comparably-equipped Wang system. Also, communication is possible with any mainframe computer that is capable of communicating with an IBM 2780 terminal.

Through a 2228N Null Modem, two 2200MVP CPU's equipped with identical 2228B controllers set to the same baud rates may have direct local synchronous communications.

(No Photograph Available)

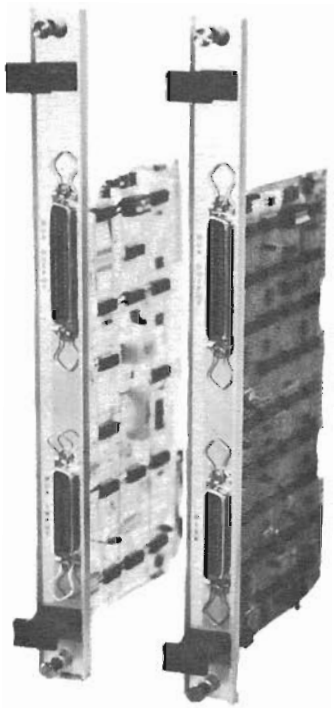


FIGURE
1-24

The Model 2230MXA-1 Master Daisy Chain Disk Multiplexer (1st CPU) and the 2230MXB-1 Slave Mux (2nd, 3rd, or 4th CPU) allows up to four 2200MVP CPU's to access any on-line disk.

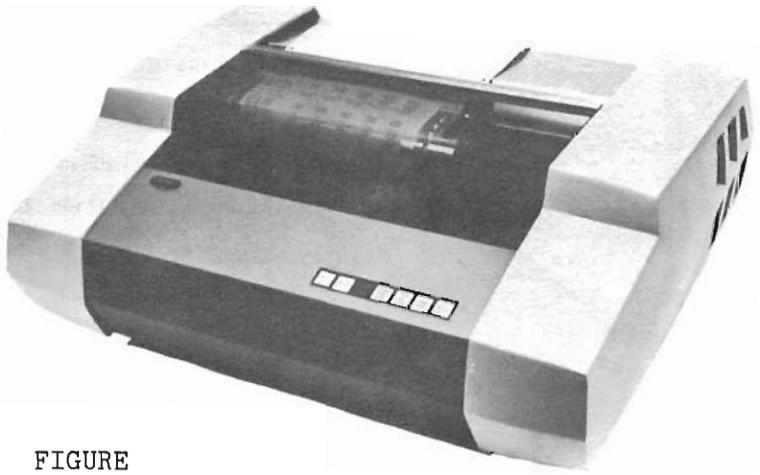


FIGURE
1-25

The 2231W-1, 2, 3, & 6 are dot-matrix printers (W-1: 10-pitch, 112 col, 120 cps; W-2: 12-pitch, 132 col, 120 cps; W-3: 14.4-pitch, 120 cps, graphic display printout capability; W-6: 12-pitch, 132 col, 70 cps, high-density characters).

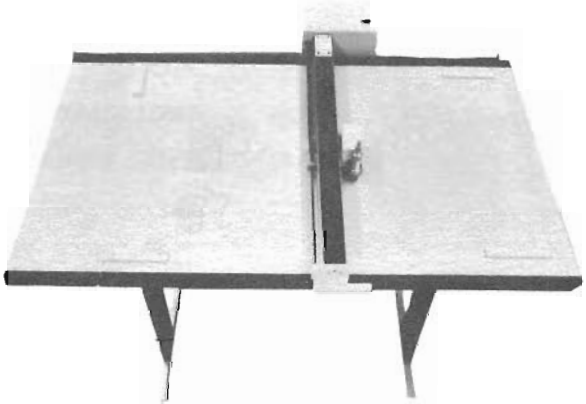


FIGURE
1-26

The 2232B digital flatbed plotter provides continuous line or point plotting of curves and data, with an accuracy of ± .005 inches over the entire 31 x 48-inch plotting surface.

FIGURE
1-27

The 2236D is given more extensive descriptive treatment in paragraph 1.3, since these terminals are an integral part of every 2200MVP system.

FIGURE
1-28

The Model 2251 is a 40-column, 110-cps matrix line printer.

FIGURE
1-29

The total storage capacity (10 Megabytes, typical) of the Model 2260BC & C Fixed/Removable Disk Drives is divided equally between two separate hard-disk platters, one of which is removable and can be conveniently stored.

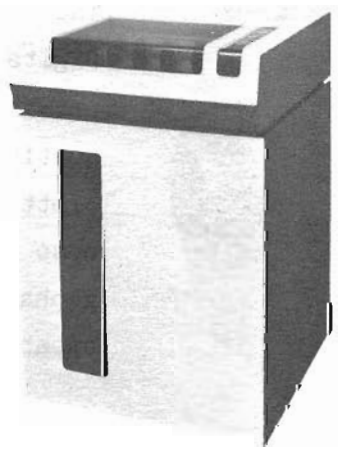


FIGURE
1-30

The Model 2261W High-Speed Printer utilizes two bidirectional heads to print up to 330 characters per second, or 125 lines per minute (132 characters per line, maximum).

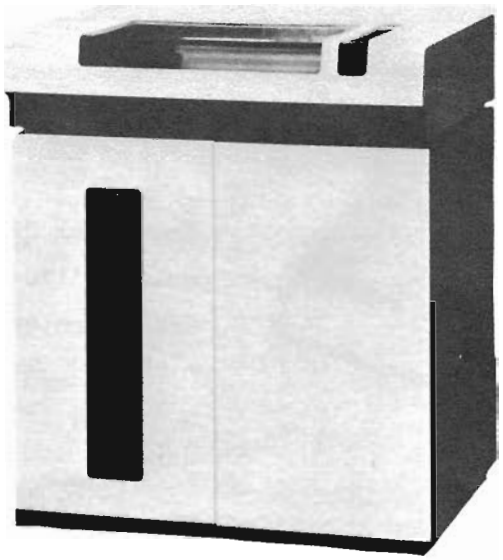


FIGURE
1-31

The 2263-1, and -2 printers produce up to 132 characters per line using a chain of solid characters (hence the alternate designation "chain printer"). The 2263-1 prints 400 lines per minute; the 2263-2, 600 lines per minute.

FIGURE
1-32

The Model 2270A-D IBM-compatible Floppy Disk unit is available in three models (2270A-1D, -2D, and -3D) containing one to three flexible disk drives.

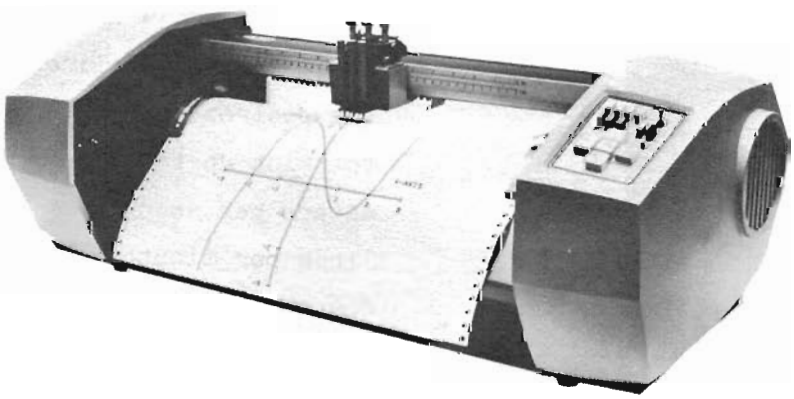


FIGURE
1-33

The 2272-2 Triple-Pen, Digital Drum Plotter provides point and continuous-line plotting. The 2272-2 also has full alphanumenric labelling capabilities.

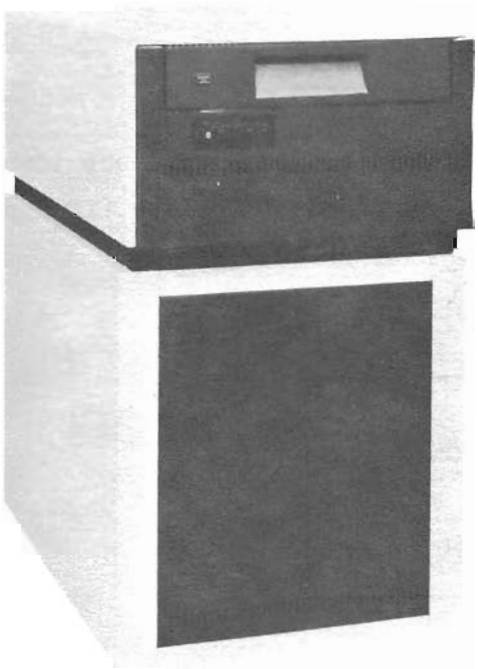


FIGURE
1-34

The Model 2280 fixed/removable hard disk drive comes in three versions: the 2280-1 (13.4 meg fixed, 13.4 meg removable), the 2280-2 (40.2 meg fixed, 13.4 meg removable), and the 2280-3 (67 meg fixed, 13.4 meg removable).

FIGURE
1-35

The Model 2281P is a 30-cps daisy wheel character printer with plotting capability.

FIGURE
1-36

The Model 2282 graphic display terminal adds an interactive CRT plotting capability to the 2200MVP system. Screenloads from the 2282 can be duplicated on the 2231W-3 matrix printer.

1.8 MODEL INFORMATION

A Wang serial tag attached to the rear panel of each product identifies model number, memory size (if applicable), number of I/O slots (if applicable), and line frequency/voltage/wattage ratings.

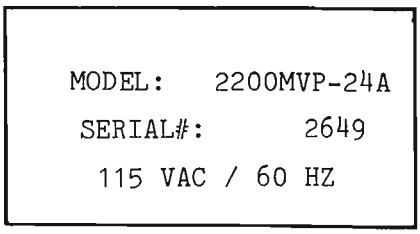


FIGURE 1-37 A TYPICAL SERIAL TAG

EXAMPLE: (MEMORY SIZES)

CPU MODEL:	MEMORY SIZE:
2200 MVP-4	CPU with 9 I/O Slots & 16K-Byte Memory
2200 MVP-8	Same as above, but with 32K
2200 MVP-12	Same as above, but with 48K
2200 MVP-16	Same as above, but with 64K
2200 MVP-24	Same as above, but with 96K
2200 MVP-32	Same as above, but with 128K
2200 MVP-48	Same as above, but with 192K
2200 MVP-64	Same as above, but with 256K

Some peripheral devices may be further identified by an O.E.M serial tag (i.e., Diablo, Shugart, CDC, etc.).

NOTES:

NOTES:

SECTION 2
SITE PLANNING

2.1 GENERAL

This section presents detailed physical planning information for the 2200MVP installation. Proper attention to the selection and preparation of the computer site will ensure easy installation and efficient, trouble-free operation of the system.

The computer's operation and reliability can be greatly affected by environmental factors, the most important being temperature, humidity, dust, electrical power, and electromagnetic interference.

While the 2200MVP is designed to operate in normal office environments, office environments may vary greatly. Because of this, it is important that the environment for the system be carefully chosen and regulated. An ideal location would be one in which temperature and humidity are controlled, airborne dirt and contaminants are reduced to a minimum, AC power outlets are adequate, regulated, and noise free, and sufficient room exists for future expansion.

The recommended operating environment is defined by the following parameters:

Temperature: 60°F to 80°F (18°C to 24°C)
Relative Humidity: 35% to 65%, non-condensing
Dust: No accumulation should be obvious in a 24-hour period
Power: Grounded, noise-free, dedicated 115 or 230 VAC ± 10%, 50 or 60 Hz ± 1Hz
Interference: All sources of static electricity, magnetic fields, and EMI must be controlled.

Important considerations for the system's physical location, ideal environment, and electrical requirements are presented in the paragraphs that follow. In addition to being helpful in system installations, these topics will give the CE an adequate background for making knowledgeable recommendations to the customers.

2.2 SELECTING A LOCATION

Three important considerations for site selection are:

a. The task to be done - the system should be located in or near the department that has primary use of the system, so that it is easily accessible by operating personnel.

b. The availability of adequate space - The computer room should be large enough to provide good air circulation for system cooling. The computer room should also have additional space for computer materials and accessories, shelves for the storage of disks and diskettes, and bookcases or files for the storage of system manuals. Extra space should be allowed for future system expansion.

NOTE:

Disks may be stored in a remote area if computer room storage space is a problem, but the remote location must have the same environmental controls as the computer room.

c. Isolation of computer room - The location should be sufficiently removed from the main flow of personnel traffic to prevent any interference with the smooth operation of the 2200MVP System.

More specific considerations and guidelines pertaining to site selection are listed below.

A. Access Route - Movement of equipment from the unloading point to the actual site.

1. Hallways and doors - Are they wide enough? All hallways and doors along the access route must have a minimum 36" clearance.

2. Floor loading capacity - Will the floor of the proposed computer room support the weight of this new 2200MVP? Will that floor be adequate if the system is upgraded?

3. Elevator capacity - Are the load size and weight specifications of the elevator adequate for equipment movement? Note that the heaviest units, the 2263-1,-2 Line Printers, weigh approximately 570 pounds (approx. 260 Kg.) unpacked.

4. Unloading facilities - Is any special equipment needed to transport system components from the unloading point to the installation site?

B. Proximity of the Main Computer Area to Users' Departments

1. Allocation of system printer facilities.

2. Minimizing operator traffic.

3. If the computer room door is opened too frequently (should one exist), the efficiency of the environmental control systems might be degraded.

C. Computer Room Layout (Placement of equipment)

The layout of the computer room should be planned in advance on paper. For each unit the distance from the wall plugs should be estimated, along with the needed cable lengths. See Section 1 for a complete listing of the available cables and extensions.

NOTE:

Most Wang units are equipped with exhaust fans and entry vents. To ensure proper cooling, these vents and fans must not be obstructed. Never place system equipment against file cabinets or other surfaces that might impede proper air flow.

1. AC Power cords - In order to minimize Electromagnetic Interference, power cord lengths should not be extended by the addition of extension cords. All system units should have their own electrical outlets.

   a. The 2200MVP CPU must be within nine feet (approx. 2.75m) of a wall outlet.
   b. Disk drives must be within six feet (approx. 1.82m) of a wall outlet.
   c. System printers must be within 6 feet of a wall outlet; one exception is the Model 2263, which must be within 12 of a wall outlet.
   d. Each 2236D Workstation must be within 8 feet of a wall outlet.

2. Plan the computer room for optimum efficiency and serviceability.

   a. Optimize operator access - Allow room for the operators to load printer paper and to mount/dismount disks.
   b. Allow for service access on each unit - Allow 30" between the wall and each unit in the system.
   c. Allocate work areas.
   d. Optimize the workflow into and out of the computer room.
   e. Minimize system cable lengths wherever it may be practical to do so without degrading the site layout.
   f. Allocate some space for short-term storage of printer paper, printer ribbons/cartridges, tape, and disk media

D. Fire Protection & Security Equipment

Inform the customer of the advantages of the following:

1. A fire-resistant safe or file for backup copies of critical data and files, preferably located in a separate area, perhaps even in a different building.

2. A suitable fire alarm system.

3. Physical security devices and systems, such as locks, alarms, etc.

F. Lighting and Acoustics

1. Normal business lighting is sufficient.

2. To reduce the acoustic noise level, construct the computer room walls, ceiling, and floor, if necessary, with soundproofing materials.

3. Carpeting reduces noise, but it is not recommended, because it contributes to static build-up. See Section 2.3.2 for a discussion of static build-up and carpeting.

E. Future Upgrade Considerations

1. Installation of AC power to the computer room, including the grounding requirements.

2. Cabling (routing through conduits, walls, floors, etc.)

3. Additional environmental controls; include static suppression and noise suppression.

4. Fire protection & detection equipment.

5. Allocate extra space in the computer room for future 2200MVP system upgrades.

2.3 CONTROLLING THE ENVIRONMENT

The physical environment in which the system operates can greatly affect its performance. Once a location has been selected, three critical parameters to be considered are temperature, humidity/static build-up, and dust/contamination. These parameters are treated separately in the paragraphs that follow.

2.3.1 TEMPERATURE

Temperature is the the most important environmental consideration because it can vary greatly from day-to-day. If the system is used where temperatures exceed the maximum specified, component failure rates will drastically increase, resulting in costly downtime for the user. High temperatures (or rapidly changing temperatures) can also cause warping and distortion of data storage material, resulting in lost data.

Low outside temperatures are usually not a problem because nearly all locations are heated. High temperatures can be a problem because many locations do not have air conditioning.

Temperature can be controlled by the usual heating and air conditioning units. When planning heating and air conditioning needs, remember to consider the heat output of the 2200MVP system.

If an air conditioning unit is already installed or if one is to be installed, it is imperative that a separate power line be used for the air conditioner. This will prevent electrical noise on the MVP line. If a separate power line is not used, system errors may occur when the air conditioner is in use. See Section 2.4 for a more detailed description of power line requirements.

A. Common sources of heat accumulation/loss in the computer room environment are:

1. Heat dissipated by all equipment.

2. Heat dissipated by all personnel working in the computer area.

3. Air circulation in computer room.

4. Presence of large windows - these may require thermal insulation.

5. Heat entering the computer room through walls, ceiling, and floor.

6. Personnel traffic through the computer room.

B. Temperature Limits

1. Temperature must be maintained between 60 and 80 degrees Fahrenheit (between 15 and 28 degrees Celsius).

2. Areas allocated for long-term media storage must have temperature specifications that closely match the computer room environment.

C. BTU Ratings

1. Calculate the <u>total</u> BTU dissipation of the Wang equipment, and make this figure available to the customer; the rest is up to the customer's air conditioning specialist. Remind the customer to allow for any non-Wang Equipment that may be in the Computer Room.

2. For a listing of BTU outputs for the 2200MVP CPU and peripherals, see Table 2-1.

2.3.2 HUMIDITY AND STATIC BUILD-UP

Heating and air conditioning units are good for maintaining proper room temperature, but unfortunately, these units also remove moisture from the air, thereby lowering the humidity.

Low humidity can be a prime cause of equipment problems. If the system is installed in a carpeted room, the lower humidity plus the static generating capability of carpets and operator's clothing will impart a static electrical charge on operating personnel. When the operator touches the system, the resultant staic discharge, possibly several thousand volts, can cause system malfunctions and the destruction of recorded data.

Static can be particularly severe during the winter months when buildings are heated. As the heating dries the air, the relative humidity may drop to as low as 20 percent.

Low humidity not only increases the certainty of static build-up but also causes oxide shed in data storage material. High humidity, on the other hand, rapidly deteriorates paper stock, magnetic disks, and tape.

Humidifiers and dehumidifiers should be installed in the heating, ventilating, and air conditioning system to increase or decrease the humidity as required.

A. Humidity Limits

1. The recommended humidity range is from 35% to 65% R.H. (non-condensing).

2. Areas allocated for long-term media storage must have humidity specifications that closely match the computer room environment.

B. Guidelines for Minimizing Static Electricity

1. No furniture with plastic upholstery and/or rubber wheels can be situated in the computer room.

2. Maintain the computer room humidity above 35%.

3. Ensure that the entire 2200MVP system is connected to a good earth ground (See Section 2.4).

4. Do not install carpeting - If carpeting is unavoidable, liberal usage of chemical anti-static sprays and/or overlays of good anti-static carpeting will be necessary. Follow the guidelines in the following paragraphs.

C. Guidelines for Computer Room Carpeting

1. Generally speaking, the computer room should never be carpeted, since carpeting plus low humidity will generate significant amounts of static electricity. Nevertheless, if a customer plans to install carpeting in the computer room, be certain to recommend the special metal-impregnated, anti-static carpeting, which can be grounded.

2. In facilities that already have carpeting, check to see if it is the anti-static type. If it is not, recommend that the carpeting be treated with a anti-static spray, or recommend that an electrically conductive mat be installed over the existing carpeting to prevent static build-up.

   Carpets treated with non-static spray should be thoroughly cleaned before the first treatment and retreated at least once every three months thereafter.

If an electrically conductive mat is used, it should be installed under the system operating area and must be properly connected to an earth ground to prevent static build-up.

2.3.3 DIRT AND CONTAMINANTS

In dusty computer room environments, airborne contaminants may accumulate rapidly on circuit boards and components, forming a greasy film. This can degrade system performance and cause system malfunctions by:

a. Preventing adequate heat dissipation from the electronic components.
b. Creating a leakage path for electrical signals.
c. Causing excessive mechanical wear in tape and disk drives, and leaving scratches in the oxide coating of storage media or in the read/write heads themselves.

Dust can be controlled effectively by the usual HVAC (heating, ventilating, and air conditioning) equipment if these units are equipped with adequate filters.

The filters of all HVAC equipment should be cleaned or replaced regularly. In areas where these filters do not sufficiently remove airborne contaminants, an electrostatic air filter should be installed.

Guidelines for Controlling Air Contamination

1. No accumulation of dust on equipment should be obvious over a given 24-hour period.

2. All HVAC systems must have adequate air filters; these filters must be cleaned or replaced regularly.

3. Avoid foods, beverages, and smoking in the computer room, especially in the vicinity of disk and tape drives. Recommend to the customer that he institute rules to govern these activities.

4. Recommend that the computer room be cleaned and vacuumed regularly. Do not buff the floor with steel wool pads; steel wool particles, drawn into the units by their cooling fans, can contaminate the PC boards and cause system failures.

2.4 ELECTRICAL REQUIREMENTS

Before installation, check to be certain that the power requirements can be met for the area where the system is to be installed. The 2200MVP system should have a dedicated AC power line. This power line must be regulated to within ± 10%, must be properly grounded, and must be noise free. The following paragraphs discuss these requirements in detail.

2.4.1 COMPUTER ROOM AC POWER

The electical requirements of the 2200MVP--voltage, current, and frequency--must be fulfilled by the customer. It may be necessary for the customer to have special power lines and receptacles installed prior to system delivery. This is especially true in older buildings, where the wiring may be inadequate for the 2200MVP system.

For most system configurations, a 20 ampere, 115 VAC power line, regulated to within ± 10%, will be adequate. If the voltage fluctuates outside the required limits, corrective devices must be installed on the power line: constant voltage transformers which correct voltage fluctuations, or AC line conditioners which correct voltage fluctuations and eliminate power-line electrical noise.

NOTE:

When power line disturbances are suspected, the actual cause must be determined before a correct solution can be proposed. Some power line problems are difficult to diagnose, and may require the use of a power line analyzer.

Guidelines for Computer Room AC Power (Ideal)

1. The 2200MVP System should have a dedicated feedline from the main AC power source; in particular, this line must be isolated from the computer room air conditioning system and any other unusual loads, such as motors and office equipment.

2. Power lines to the computer room should be routed through grounded conduits, separate from other AC lines.

3. AC power to the computer room should be distributed to the various units in the 2200MVP System from a power panel, preferably located in the computer room.

4. All branch wiring should be suitable for motor-load applications.

5. All branch circuits should be protected by circuit breakers that are suitable for motor-load applications. The circuit breakers should be clearly labeled for easy identification.

6. There should be an easily accessible master emergency circuit breaker at one designated location. All computer room personnel should know where this breaker is.

2.4.2 ELECTROMAGNETIC INTERFERENCE (EMI)

Computers and peripheral equipment are susceptible to malfunction due to Electromagnetic Interference (EMI). The sources of EMI may include electric office machines such as typewriters; HVAC units such as air conditioning; water coolers, electric motors and machinery; fluorescent lighting and arc welders.

EMI can enter the system by conduction along wiring and cabling, or by direct radiation (radiated EMI) when the EMI generating equipment is located near the 2200MVP system.

When EMI problems are suspected, make an effort to determine the source(s) of the EMI before proposing a solution.

Guidelines for Controlling Electromagnetic Interference (EMI)

1. Provide a dedicated AC line for the system, isolated from interference generating devices (including fluorescent lighting).

2. Provide proper grounding for the AC line. See the following paragraphs for grounding guidelines.

3. Make certain that the AC power line has been properly installed in steel conduit, for shielding, and that the conduit is properly connected to junction boxes.

4. If EMI generating devices are located near the system, relocate, repair, or filter them to prevent interference to the system.

5. If the source of the noise cannot be found, install EMI filters, isolation transformers, and line conditioners on the system's AC power line, as needed.

6. In extreme cases, such as when arc welders are used near the system, it may also be necessary to shield the peripheral cables.

2.4.3 GROUNDING

Proper grounding is critically important. To protect the operating personnel from electrical shock, the power cords for all units should be attached, with the 3-prong plugs provided, to an appropriately grounded line.

It is essential that the system ground be a true ground. A poor ground will aggravate power line problems and make the system more susceptible to power line disturbances.

CAUTION:

Always connect the 2200MVP CPU and peripherals to properly grounded outlets to prevent electrical shock to the operating personnel.

Guidelines for System Grounding (Ideal)

1. For grounding puposes, each customer-supplied branch circuit should have an insulated conductor at least equal in size to the phase conductor.

2. Every branch circuit grounding wire should be tied to a single point, common to all branch circuits, at the distribution panel.

3. A single ground conductor, larger than the wires used to carry AC power to the computer room, should connect that common grounding point to a true earth ground, NOT NEUTRAL.

4. Conduit must NOT be the sole means of grounding the system.

2.4.4 SPECIFIC AC POWER REQUIREMENTS

Each unit has specific current, voltage, and circuit breaker requirements as indicated in Table 2-1 of this section.

As stated earlier, a single 20 ampere, 115 VAC power line will be adequate for most system configurations. However, to determine if a larger line is necessary, or if two lines are necessary, calculate the maximum total current demand of the system. Find the units in the customer's configuration in Table 2-1, and add up their individual amperage requirements. Whenever the sum exceeds 20 amps, a larger line or more than one separate line must be used.

NOTE:

For disk drives and for printers with large motors, use the start-up current in the calculation.

For example, a typical system configuration consisting of the Model 2200MVP CPU, a 2270A-2D Diskette Drive, a Model 2260 Disk Drive, three Model 2236D Terminals, and a Model 2261W Matrix Printer would require the following calculation:

	MODEL	AMPS (115V)	(230V)*
	2200MVP CPU	2.0A	1.0A
	2270A-2D	2.0A	1.0A
	2260	7.0A	3.5A
(3)	2236D	1.8A	0.9A
	2261W	3.8A	1.9A
		16.6A	8.3A

Thus, for this example configuration, one 20 amp power line is sufficient.

*Current calculation for 230VAC system

TABLE 2-1
2200MVP SYSTEM UNITS

EQUIPMENT	ACTUAL POWER USED	BTU/HR OUTPUT (MAX)
2200MVP CPU	115VAC (± 10%) 60HZ 2.0 AMPS	800 BTU/hr
2236D INTERACTIVE TERMINAL	115VAC (± 10%) 60HZ 0.6 AMPS	250 BTU/hr
2201L OUTPUT WRITER	115VAC (± 10%) 60HZ 1.1 AMPS	450 BTU/hr
2221W MATRIX PRINTER	115VAC (± 10%) 60HZ 2.5 AMPS	1200 BTU/hr
2231W-1,2,3,6 MATRIX PRINTERS	115VAC (± 10%) 60HZ 1.25 AMPS	550 BTU/hr
2232B DIGITAL FLATBED PLOTTER	115VAC (± 10%) 60HZ 1.5 AMPS	600 BTU/hr
2261W MATRIX LINE PRINTER	115VAC (± 10%) 60HZ 3.75 AMPS	1600 BTU/hr
2263-1,-2 LINE PRINTERS	115VAC (± 10%) 60HZ 5.5 AMPS	2700 BTU/hr
2271 PRINTER	115VAC (± 10%) 60 HZ 1.1 AMPS	450 BTU/hr
2272-2 TRIPLE PEN DRUM PLOTTER	115VAC (± 10%) 60 HZ 2.0 AMPS	850 BTU/hr
2281P PLOTTING DAISY OUTPUT WRITER	115VAC (± 10%) 60HZ 2.2 AMPS	900 BTU/hr
2282 GRAPHIC CRT	115VAC (± 10%) 60HZ 0.6 AMPS	250 BTU/hr
2209A 9-TRACK TAPE DRIVE	115VAC (± 10%) 60HZ 4.1 AMPS	1700 BTU/hr
2260 DISK DRIVES (Several Models)	115VAC (± 10%) 60HZ 7.0 AMPS STARTUP 4.0 AMPS OPERATING	1800 BTU/hr
2270A-1D,2D,3D IBM COMPATIBLE DISKETTE DRIVES	115VAC (± 10%) 60HZ 2.0 AMPS	900 BTU/hr
2280-1,2,3 DISK DRIVES*	115VAC (± 10%) 15.0 AMPS STARTUP 8.2 AMPS RUNNING	3000 BTU/hr

*Dedicated power line required.

NOTES:

NOTES:

SECTION 3
SYSTEM INSTALLATION

3.1 GENERAL

This section contains installation, checkout, and system interconnection instructions for the Model 2200MVP computer system. Because of the wide range of peripherals available to this system, it would be impractical to present here a full installation procedure for each. All available peripherals are fully documented in other Wang or OEM publications. For complete information on any specific peripherals, refer to the 2200MVP SYSTEM-LEVEL DOCUMENTATION list, contained in the preface of this manual.

3.2 UNPACKING AND INCOMING INSPECTION

Each peripheral model has its own inspection procedure. Refer to the maintenance publications named in the 2200MVP System-Level Documentation list for specific unpacking and inspection procedures. In all cases, the critical assemblies must be inspected, first for damage and then for proper adjustment.

The following general guidelines for unpacking and inspection apply to all 2200MVP system units:

A. Check to be certain that all equipment (peripherals, cables, stands, etc.) has been delivered.

B. Unpack each unit, using extreme caution, especially with the workstations. For shipping, larger peripherals are generally bolted to wooden skids and enclosed in cardboard shipping boxes. Carefully remove these packing containers, using pry bars and open-end wrenches as needed.

C. Inspect each unit for shipping damage. Immediately report any physical damage to the shipping carrier and the Home Office.

D. Move the units to their permanent locations. During transit, protect the cabinets from scratches, keeping the protective wrapping on the units until they are in their final positions.

E. Remove the covers from the CPU and other peripheral devices. Remove any shipping clamps. Inspect the units for damaged or loosened assemblies. Also check for loose hardware. Ensure that the units are throughly clean. Be certain that each printed circuit board, including the power supply board, is in its proper location and fully seated.

F. Assemble the peripherals, as necessary. For workstations, this step will include the installation of PC boards; for other peripherals, this step will include the installation of accessories, such as paper racks for printers.

G. Inspect the storage media (diskettes, tapes, etc.) for damage.

H. Check the electrical wiring of the computer room to ensure that the electrical requirements of the 2200MVP system will be met. Pay particular attention to grounding. This topic is covered in detail in Section 2.

H. Set the device switches and baud rate switches where applicable, as described in the following paragraphs. Also where applicable, set the AC voltage (115/230) and line frequency (50Hz/60Hz) switches.

I. Route peripheral cables to the CPU as described in section 3.5.

3.3 BAUD RATE SELECTION

Four 2236D Terminals can be attached to one 2236MXD controller, and a maximum of two 2236MXD controllers may be used in a 2200MVP system.

The baud rate setting of the each port of the 2236MXD controller must match the baud rate setting of its corresponding terminal. For systems used in local operation (without modem), the baud rate may be set as high as 19.2K baud, regardless of cable length. For remote operation, the baud rate of the terminal must be set to match the baud rate of the modem. Asynchronous communications modems are available for transmission speeds as high as 2400 baud.

3.3.1 2236D TERMINAL 5-BANK BAUD RATE SWITCH

Set the baud rate switch on the 7292-1 board of each 2236D Terminal. When the terminal cover is on, access to the baud rate switch is through the large plug-button on the rear of the cover. See Figures 3-1 and 3-2. Set the switches of the five-bank switch as follows:

Switch:	1	2	3	4	5	Baud Rate
	ON	OFF	OFF	OFF	OFF	300
	ON	OFF	OFF	OFF	ON	600
	ON	OFF	OFF	ON	OFF	1200
	ON	OFF	OFF	ON	ON	2400
	ON	OFF	ON	OFF	OFF	4800
	ON	OFF	ON	OFF	ON	9600
	ON	ON	ON	OFF	ON	19.2K

In all cases switch 1 is ON to enable parity error detection. Switch 1 must always be ON for proper operation.

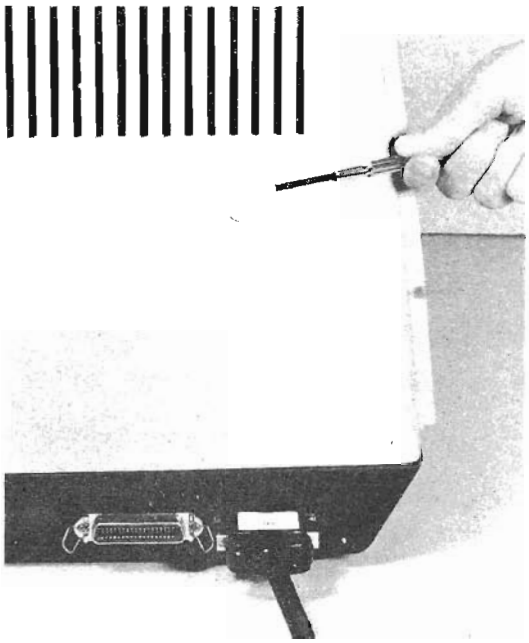


FIGURE 3-1 ACCESS TO THE BAUD RATE SWITCH

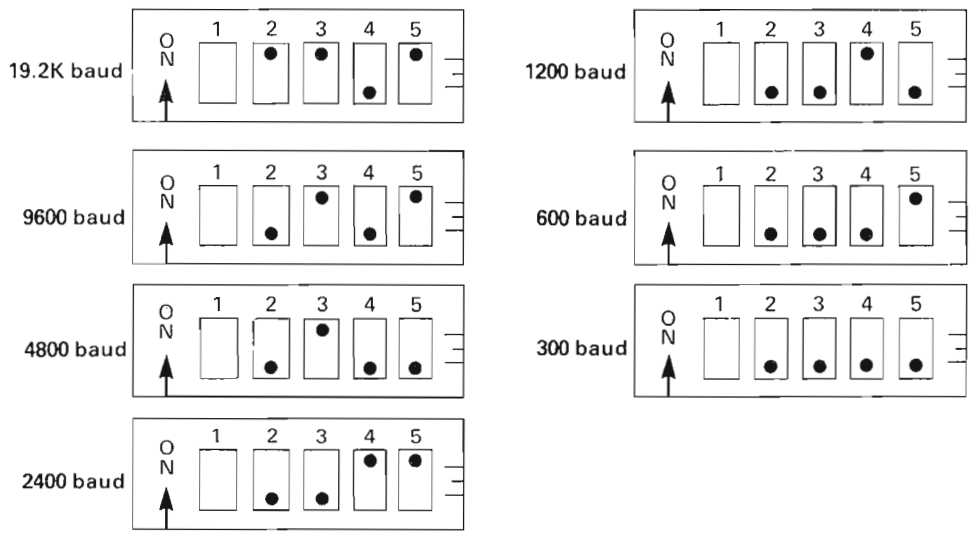


FIGURE 3-2 BAUD RATE SWITCH SETTINGS FOR THE 2236D TERMINAL

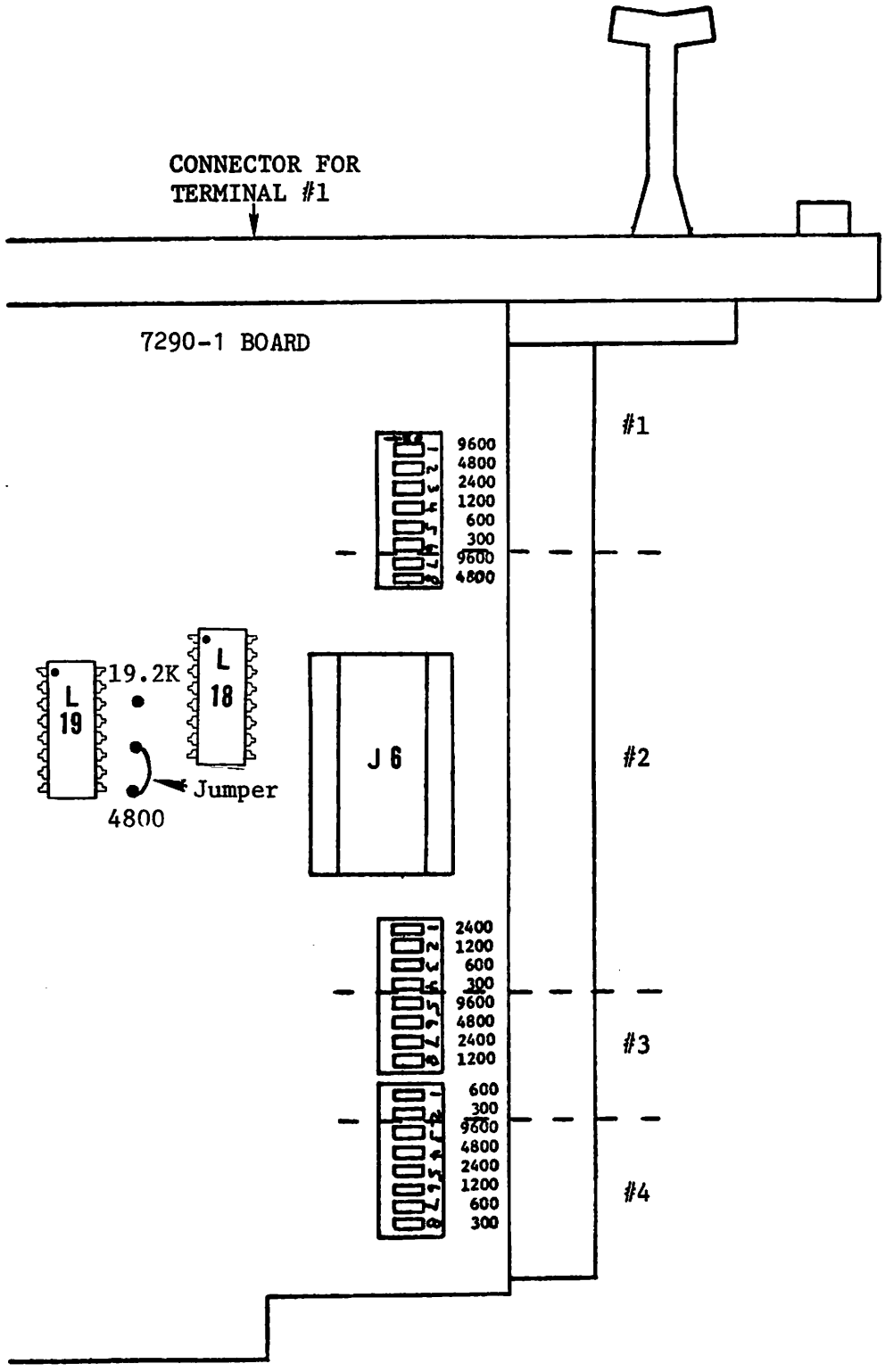


FIGURE 3-3 2236MXD CONTROLLER - BAUD RATE SWITCH IDENTIFICATION

3.3.2 2236MXD CONTROLLER BAUD RATE SWITCHES

For baud rate selection, there are three 8-bank switches (a total of 24 individual switches) located on the 7290-1 controller board. These switches comprise four groups of six switches each, with each group corresponding to a RS-232-C connector on the top panel. The switches in each group are labeled for specific baud rates: 300, 600, 1200, 2400, 4800, or 9600. See Figure 3-3.

Set the controller baud rate switches. Only one switch in any group of six may be ON at any one time. Remember that the baud rate setting for each connector must match the baud rate setting of the corresponding terminal.

NOTE:

The 4800 switch setting is used for both 4800 and 19.2K baud. The selected rate depends on the position of jumper A13, located between IC's L18 and L19. See Figure 3-3.

3.4 DEVICE ADDRESSES

During system installation, a two-digit (HEX) device address must be set on the controller card for each peripheral device. The following paragraphs pertain to device selection. The first part of this section presents background information about device selection codes; the last part of the section is devoted to the actual procedures for setting device addresses.

3.4.1 DEVICE SELECTION CODES

The controller for each peripheral attached to the CPU is assigned a unique Device Selection Code, consisting of three hexadecimal digits. The device selection code is in the form XY_1Y_2, where X is the Device Type (or Device Class) and Y_1Y_2 is the Device Address (also called unit address or hardware address).

TABLE 3-1 SUMMARY OF DEVICE-TYPE CODES (DEVICE CLASSES)

1st HEX DIGIT (X)	CATEGORY
0	Used with workstations (CRT and keyboard). Outputs a line feed (HEX OA) after each carriage return. Also used with nine-track tape drives.
1	Not used.
2	Used with printers and output writers that internally generate a line feed following a carriage return. Outputs a null character (HEX 00) after each carriage return.
3,B	Used with disk drives and diskette drives.
4	Used with plotters and plotting writers. Plotting writers normally use type 4 (to plot) or type 2 (to print). System generated Carriage Return (HEX OD), Line-Feed (HEX OA), and Null (HEX 00) characters are suppressed.
5	Not used.
6	Reserved for card readers; not used in MVP.
7	Reserved for certain output applications; not used in MVP. Does not output any extra character after a Carriage Return (HEX OD) is output.
C	Used with certain plotter operations.

TABLE 3-2 SUMMARY OF DEVICE-ADDRESS CODES

	MODEL #	DESCRIPTION	USUAL HEX ADDRESS	ALTERNATIVE HEX ADDRESSES
CRT's	2236D*	Interactive Terminal		
		. CRT	05	-
		. Keyboard	01	-
		. Local Printer/Plotter	04	-
	2282	Graphic CRT	13	14, 15
Printers	2221W	Matrix Line Printer: 132 col/200 cps	15	16
	2231W-1	Matrix Line Printers: 112 col/120 cps	15	16
	-2	132 col/120 cps		
	-3	132 col/120 cps		
	-6	132 col/70 cps		
	2251	Matrix Line Printer: 40 col/110 cps	15	16
	2261W	Matrix Line Printer: 220 LPM	15	16
	2263-1	Chain Line Printers: 400 LPM	15	16
	-2	600 LPM		
Plotters	2232B	Digital Flatbed Plotter (31"x48")	13	14
	2272-2	Triple Pen Drum Plotter	13	14, 15
Output Writers	2201L	Output Writer: 156 col/15 cps	15	16
	2271	Bidirectional Output Writer: 15 cps	15	16
	2271P	Bidirectional Plotting Output Writer: 15 cps	15	16
	2281	Daisy Output Writer: 30 cps	15	16
	2281P	Daisy Plotting Output Writer: 30 cps	15	16

* These addresses are not user modifiable.

TABLE 3-2 SUMMARY OF DEVICE-ADDRESS CODES
(continued)

	MODEL #	DESCRIPTION	USUAL HEX ADDRESS	ALTERNATIVE HEX ADDRESSES
Controllers	2227B	Buffered Asynchronous Communications Controller	1C	1A-1F
	2228B	Synchronous/Asynchronous Communications Controller	1C	1A-1F
	2228C	Synchronous/Asynchronous Communications Controller	1C	1A-1F
	2230MXA-1 MXB-1	Disk Multiplexer Controllers	10	10-70
	2236MXD*	Interactive Terminal Multiplexer	01-07	41-47
Storage Devices	2209A	Nine-Track Tape (1600 BPI-PE)	7B	7D, 7F
	2260BC	F/R Disk Drives (2.5, 5, 10 or 20 Mbytes)	10	10-70
	2260C	F/R Disk Drives (2.5, 5, 10 or 20 Mbytes)	10	10-70
	2280	F/R Disk Drives (30, 60, or 90 Mbytes)	10	10-70
	2270A-1D	Wang-IBM 3740 Compatible Diskette Drives .25 Megabytes	10	10-70
	-2D	.50 Megabytes		
	-3D	.75 Megabytes		

* All listed addresses are used by one device.

The device-type digit is used by the Operating System to determine which internal system I/O routines will be used to control the peripheral. This digit is needed because the various peripheral devices on the system often require different control procedures for performing an input/output operation. For example, a device-type digit of 3 indicates to the Operating System that the peripheral is a disk. Device type codes are summarized in Table 3-1.

The last two digits correspond to the actual unit's device address, which must be set on each device controller card in the 2200MVP CPU. The device address is used to electronically select the peripheral for operation. A unique device address must be assigned to each peripheral attached to the system.

When the 2200MVP is first turned on (Master Initialized), a set of default device addresses are supplied to the Master Device Table by the Operating System. These addresses will be valid in the system until changed in the Master Device Table or in the user's Local Device Table. Some addresses, like the local printer address of 204, are not modifiable by the user. See Table 3-2.

A system with one device belonging to a particular device class uses the first address for that class. Additional devices belonging to the same class are assigned the alternative address, as listed in Table 3-2.

3.4.2 SETTING THE DEVICE ADDRESS SWITCHES

Controller boards generally have device address switches like the ones shown in Figure 3-4.

The three-digit device selection code (XY_1Y_2) is treated as follows:

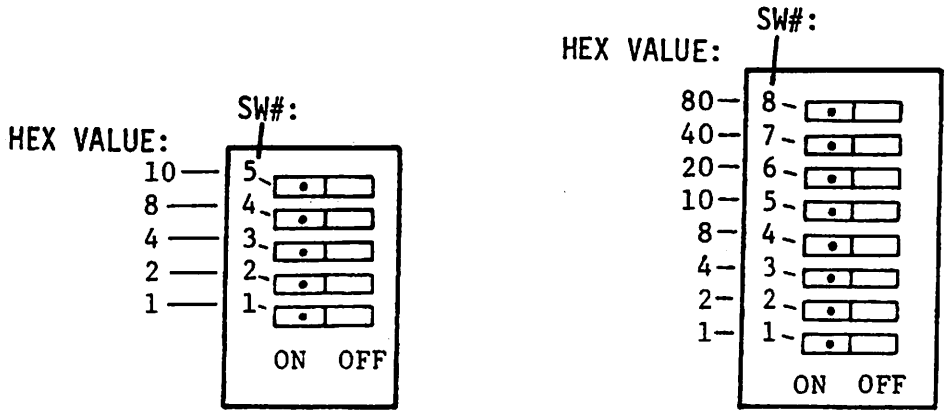


FIGURE 3-4 TYPES OF CONTROLLER ADDRESS SWITCHES

TABLE 3-3 HIGH ORDER SWITCHES

HEX VALUE	80	40	20	10
SWITCH #	SW8	SW7	SW6	SW5
HEX DIGIT				
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

1 = Switch is ON; 0 = Switch is OFF

X The most significant digit of the hex address. It is used by the Operating System to identify the device type of the peripheral. This digit is not used in device-address switch settings.

Y_1 The next most significant digit of the hex address. This digit, broken down into four binary bits, determines the setting of switches 8 through 5. See Table 3-3.

Y_2 The least most significant digit of the hex address. This digit, broken down into four binary bits, determines the settings of switches 4 through 1. See Table 3-4.

TABLE 3-4 LOW ORDER SWITCHES

HEX VALUE	8	4	2	1
SWITCH #	SW4	SW3	SW2	SW1
HEX DIGIT				
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

1 = Switch is ON; 0 = Switch is OFF

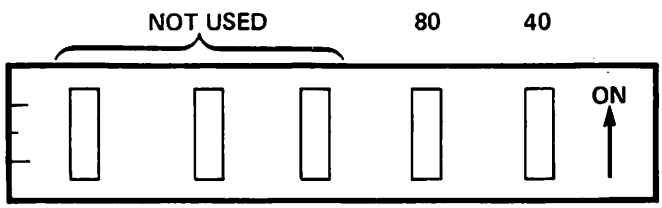
The device address conventions used in the 2200MVP system are as follows:

2236MXD TERMINAL CONTROLLERS

Each 2236MXD Terminal Controller can support a maximum of four 2236D Interactive Terminals. When the system has four or less 2236D terminals, one 2236MXD controller is used. When the system has five to eight 2236D terminals, two 2236MXD controllers are used.

The 2236MXD controller address is set by means of a five-bank switch. See Figure 3-5. For systems with a single 2236MXD controller, set the controller address switches to 00; that is, all five switches in the bank must be OFF.

In systems using two 2236MXD controllers, set the address switches of the primary controller (the one with the system terminal in connector #1) to 00 (all switches OFF). Set the address switches of the other controller to 40 (switch #1 is ON; all others are OFF).



PORT # 1 2 3 4 5
1-4
5-8 x
9-12 x

FIGURE 3-5 SETTING THE DEVICE ADDRESS OF THE 2236MXD CONTROLLER

Note that the physical device address set on the controller is not the address specified in a program for access to the 2236D terminal CRT, keyboard, and local printer. The programmable device addresses for all terminals are: 005 for a CRT; 001 for a keyboard; and 204 for a local printer. The Operating System translates these programmable addresses into the appropriate physical controller addresses.

PRINTERS

The system printer normally has the program address 215; therefore, the unit address switches of the 7079 Printer Controller must be set to HEX 15. In a configuration with two system printers, the address switches of the second printer controller would be set to HEX 16. As stated earlier, local printers (printers connected to the back of a 2236D Terminal) do not have any address switches but respond to an address of 204 under program control.

DISKS

If the diskette drive is the only disk unit on the system, the first (or leftmost) drive slot normally has the address 310, while the second drive slot has address B10. A third diskette drive slot will be addressed by 350.

If there are two separate disk drives in the system, one 6541-2 Disk Controller is to be set at 310 and the other at 320. For drives containing fixed (F) and removable (R) disk cartridges, device type 3 designates the fixed platter and the device type B designates the removable platter. In a configuration with two drives, the programmable addresses would thus be: 310 & B10 for the first drive; and 320 & B20 for the second drive.

The procedures for addressing disks when more than one is contained in the system are fully discussed in the 2200VP/MVP Disk Reference Manual.

PLOTTERS

Plotters are normally addressed by 413 or 414. For more specific addressing instructions, refer to the maintenance manuals listed in the preface of this manual.

3.5 SYSTEM CABLE INSTALLATION

A comprehensive listing of system cables is presented in Section 1 of this manual. For complete information on the installation of specific peripherals, refer to the 2200MVP System-Level Documentation list.

If peripheral I/O cables are routed through conduit, ceilings, walls, or floors, it will may be necessary to install connectors on the ends of these cables. This procedure is given in the next paragraph.

3.5.1 I/O CABLE CONNECTOR INSTALLATION

To install the I/O connectors, use a Champ Palm Grip Insertion Tool (PN 726-9412). The tool consists of a palm inserter, a lanyard, and an index slide. See Figure 3-6.

1. Position the connector in the index slide, attach the I/O cable to the slide, and then slide it into the palm inserter as indicated in Figure 3-7.

   The I/O cable should be placed so as to allow 1/2 inch of sheathing to extend beyond the stabilizer. Four inches of unsheathed twisted pairs should be allowed for correct use of this tool.

2. Orient the palm inserter with the connector, making certain that a contact about to receive a wire is on the same side as the wire slot in the inserter.

3. Align the contact to be terminated with the index mark on the palm inserter.

4. Place the palm inserter so that the pusher faces towards the heel of your hand, and your fingers should grip the base (allow the wire discharge chute to extend through your fingers).

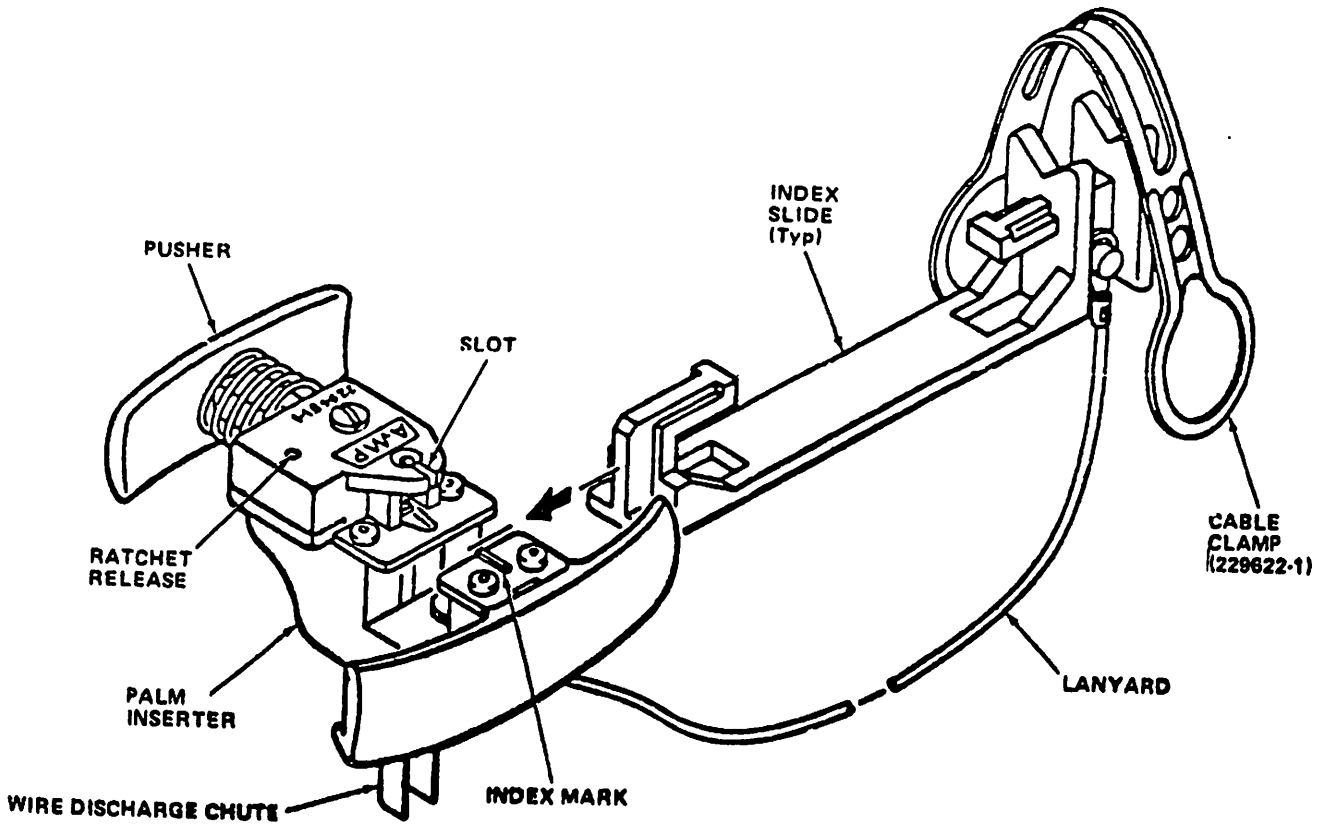


FIGURE 3-6 INSERTION TOOL

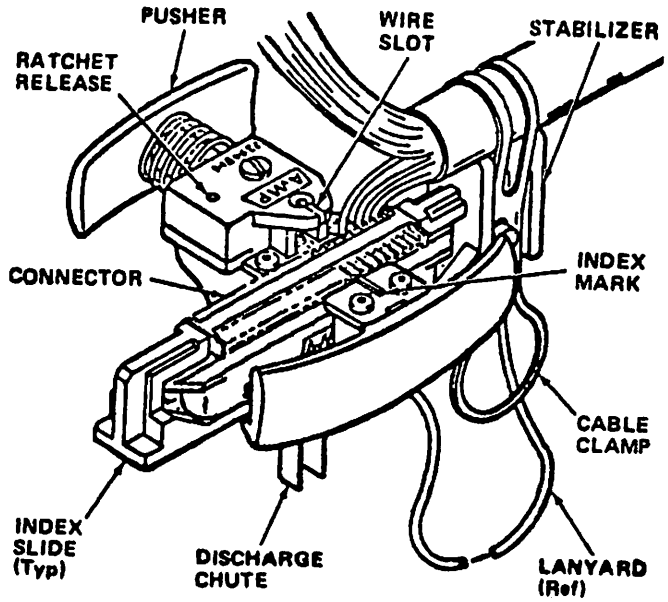
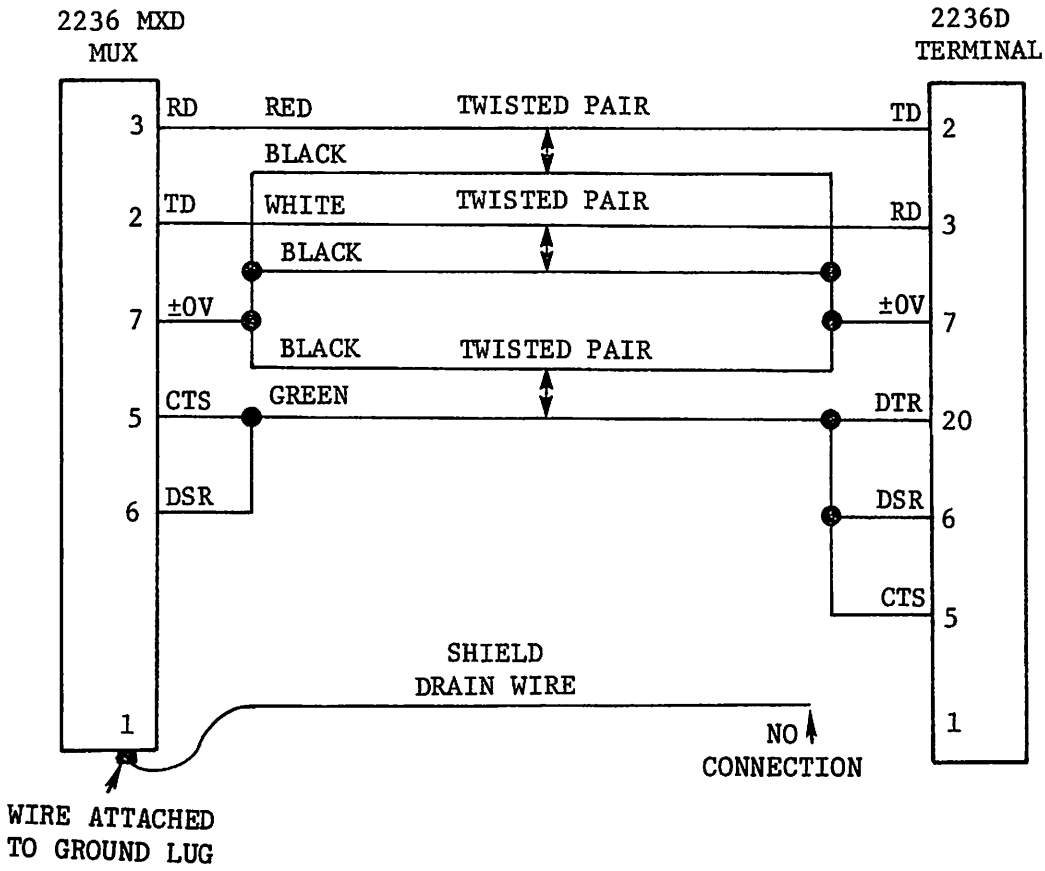


FIGURE 3-7 CONNECTOR INSTALLATION



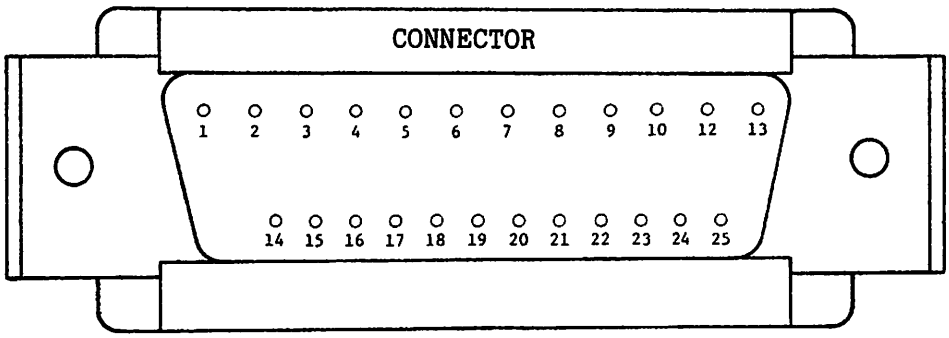


FIGURE 3-9 WIRING OF THE 2236 (RS-232-C) CABLE CONNECTOR

5. Select a wire of the proper color or number (see the cable assembly diagrams in the rear of this manual) and insert the wire through the wire slot and discharge chute; do this until all slack is out of the wire.

6. Make certain the contact and wire are centered on the index mark, and then squeeze the palm inserter until the pusher is bottomed.

7. Release your grip, allowing the pusher to retract.

NOTE:

If the palm inserter jams during this step, rotate the ratchet release in a clockwise direction with a hex wrench (supplied with the kit); this should effect release.

8. Remove the scrap wire from the discharge chute.

9. Repeat steps 1 through 8 until all contacts have been terminated on that side of the connector.

10. With the pusher released, remove the index slide and connector from the palm inserter.

11. Perform steps 1 through 10 for contacts on the other side of the connector.

12. After all contacts have been terminated, loosen the cable clamp and remove the index slide.

13. Inspect each termination, making sure that each wire has been FULLY inserted into BOTH wire slots of its contact (See Figure 3-8) and that all wires have been cut to the proper length (no exposed wire strands should be visible). Also, make sure that the insulation is NOT cut in any area other than the slot insertion area. Finally, make sure that the contacts are not crushed or deformed.

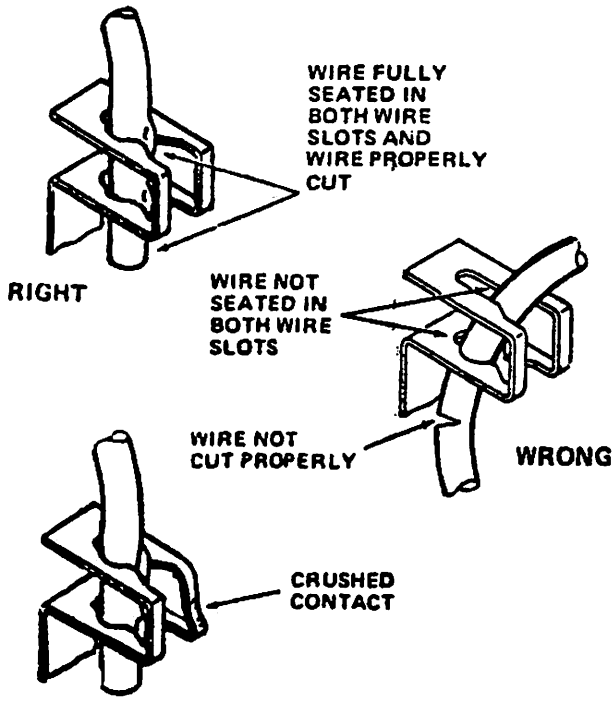


FIGURE 3-8 INSPECTING THE TERMINATIONS

If a faulty termination is found, carefully remove the wire and contact from its connector. Install another contact, trim 1/8 inch off the end of the faulty wire, and reinstall that wire, using steps 2 through 8.

14. Before the cover is installed on the 2236MXD connector, the I/O cable ground shield must be soldered to a ground lug, and that lug must be attached to the connector by one of the two screws.

15. Install a connector cover over the finished connector.

16. Connector installation is now completed.

NOTE:

The connectors for the 2236D Interactive Terminal are soldered on, and the cable insertion tool is not needed. The wiring diagram for the RS-232-C connector is shown in Figure 3-9.

3.6 MVP-A CHASSIS REQUIREMENT

The following paragraphs present a simplified method for determining whether or not the proper CPU chassis has been selected; that is, whether the system configuration requires the MVP Standard Chassis or the MVP-A Chassis. Ideally, this calculation should have been performed at the time the system was sold to the customer. Yet, because power supply damage will result if the total current demand of the controllers exceeds the rating of the chassis, it is important to perform this handy check prior to power-on testing of the system.

In this procedure, each peripheral controller is assigned a "configuration weight". All of the individual peripheral configuration weights are then added together to arrive at a "system configuration weight". The standard 2200MVP CPU will support a maximum system configuration weight of 100. If the system configuration weight exceeds 100, an MVP-A Chassis must be used.

The following listing specifies the configuration weights of most of the available 2200MVP peripherals.

	DESCRIPTION	CONTROLLER	RATING
CRT's			
2236D	Interactive Terminal	2236MXD	18
2282	Graphic CRT	22C02	6
Mass Storage Devices			
2209A	Buffered 9-Track 1600 BPI	----	17
2260BC ¼	Disk Drive	22C13	28
2260BC ½	Disk Drive	22C13	28
2260BC	Disk Drive	22C13	28
2260BC-2	Disk Drive (dual)	22C13	28

	DESCRIPTION	CONTROLLER	RATING
Mass Storage Devices (cont.)			
2260C ¼	Disk Drive	22C12	28
2260C ½	Disk Drive	22C12	28
2260C	Disk Drive	22C12	28
2260C-2	Disk Drive (dual)	22C12	28
2270A-D	Diskette Drive	22C03	4
2280-1,-2,-3	Disk Drives	22C14	5
Output Devices			
2201L	Output Writer	22C02	6
2221W	Matrix Printer	22C02	6
2231W (All)	Matrix Printer	22C02	6
2232B	Flatbed Plotter	22C01	8
2251	Matrix Printer	22C02	6
2261W	High Speed Matrix	22C02	6
2263-1,-2	High Speed Matrix	22C02	6
2271 & 2271P	Bidirectional Printer	22C02	6
2272-2	Drum Plotter	22C02	6
2281 & 2281P	Daisy Wheel Printer	22C02	6
Interfaces			
2227-B	Async TC	----	8
2228-B	Bisync TC	----	16
2228-C	Bisync TC	----	18
Multiplexer Controllers			
22C11	MVP Dual Controller (Printer, Diskettes)	----	5
2230MXA-1	Disk Multiplexer Controller		8
2230MXB-1	Disk Multiplexer Controller		5

This list should be used in the following manner. First, make a list of all the peripherals that the system configuration contains, along with their ratings. Secondly, determine if dual controllers are being used. When these controllers are used, substitute their ratings in place of the ratings for the single peripheral controllers. Add together the ratings of all devices in the system configuration. If the sum is over 100, be certain that an MVP-A Chassis is being used. Good judgement must be used on any configurations bordering the maximum. Some allowance should be left for future system upgrades.

Notes on the above listing:

a. Four Model 2236D Interactive Terminals may use a single 2236MXD Controller, which has a rating of 18.

b. Local printers, which are connected to 2236D Terminals, do not contribute to the total system configuration weight.

c. Note that the 2260BC disk drive might include a 2230MXA-1 (rating of 8).

d. Memory size of the 2200MVP CPU does not contribute any configuration weight, even for systems that contain the maximum memory size of 256 Kilobytes.

e. One other consideration is the use of 2228B or 2228C and 2236D controllers. A system should never be configured which contains more than three of the these controllers in a standard MVP chassis, or five of these controllers in an MVP-A chassis.

NOTE:

For system upgrades, the MVP chassis must be exchanged for an MVP-A chassis, WL# 270-0451 (50Hz) or WL# 270-0452 (60Hz). A conversion kit (WLI #200-0322) is available containing an MVP-A chassis and a 210-7397 regulator (to replace the standard 210-6797). The MVP-A makes 20 amps available to the I/O.

Sample Calculations

1. Average MVP System

Component	Configured Weight
MVP-8 CPU	0
2236MXD Terminal Multiplexer (for three 2236D Terminals)	18
2270A-1D Diskette Dual Controller	5
2261W Printer Dual Controller	
2260BC Disk 22C13	28
Total Configured Weight	51
Total Number of I/O slots	4

MVP-A Chassis is not required

2. Large MVP System

Component	Configured Weight
MVP-64 CPU	0
2 2236MXD Terminal Controllers (for eight 2236D Terminals)	36
2280 Disk Drive	5
2260BC Disk Drive	28
2230 MXA-1 Disk Multiplexer	8
2228B Bisynchronous TC	16
2209A 9 Track Tape Drive	17
2261W Matrix Printer	6
Total Configured Weight	116
Total Number of I/O slots Required	8

MVP-A Chassis is required

3.7 INSTALLATION/POWER-ON PROCEDURE

1. Be certain that the customer site has been prepared according to the the guidelines given in Section 2, and then place the system units in their assigned physical locations.

2. Set address switches on all I/O controllers per Section 3.4.2. Initially, plug only the first 2236MXD controller (address set to 00) and one disk controller into the CPU. Make sure the controllers are seated firmly. The system disk (or diskette) drive must be at address 310 or 320. Other peripherals and their respective controllers will be installed and tested in a later part of this procedure.

NOTE:

Set the baud rate switches in the 2236D terminals to match the baud rate switches in the 2236MXD controller.

3. Connect the 2236D terminals and system disk to their respective I/O controllers. Ensure that the peripheral cable connectors are securely fastened.

NOTE:

Be certain that the 2236D/2236MXD cable is installed correctly. One end of the cable is labeled MUX and the other end is labeled TER. Always insert the MUX end into the 2236MXD Controller and the TER end into the 2236D Terminal.

4. Make sure the AC power switches of all system units are in the OFF position, and then plug in all AC power cords.

NOTE:

Check peripherals to see that all (115/230) AC voltage switches and (50Hz/60Hz) line frequency switches are set to match the wiring at the customer site.

5. One at a time, turn on the AC power switch for each unit in this minimal system configuration, using the correct power-up sequence: first the CPU, then the disk, and then the terminals.

6. Check, and adjust if necessary, the voltages in the CPU and 2236D terminals per voltage adjust procedure in section 7.3.2. Replace the top covers when this has been completed.

7. At this point, the 2236D Terminal connected to port #1 of the 2236MXD should be displaying in the upper left corner:

```
MOUNT SYSTEM PLATTER
PRESS RESET
```

If this message is not displayed, turn the AC power switch of the CPU to OFF. After 4 or 5 seconds, turn the switch back on. If the message is still not displayed, refer to sections 3.9.1 and 7.4.1.

8. When the message:

```
MOUNT SYSTEM PLATTER
PRESS RESET
```

is displayed, place the System Platter Diskette (701-2294H) into the system diskette drive and press the RESET key on the keyboard.

9. The message "KEY SF'?" should now be displayed.

10. There are only three selections that can be made with the function keys when the "KEY SF'?" message is displayed. BASIC-2 can be loaded, the User Menu of diagnostics can be loaded or the Field Service Menu of diagnostics can be loaded. The operator should now select the User menu (SF'16 - SF'19 for disk address of 310, B10, 320, or B20, respectively). Refer to sections 3.9.2 and 7.4.1 in case of trouble.

The following should be displayed:

```
  KEY SF'
  USER DIAGNOSTIC MENU
'00 CPU DIAGNOSTIC              '02 DATA MEMORY DIAGNOSTIC
'01 CONTROL MEMORY DIAGNOSTIC
```

11. Press SF'00

LOADING CPU DIAGNOSTIC (DATE)

should be displayed for approximately 5 seconds;

then,

```
  CPU DIAG PASS LLLL
IMMED REG XX
REG INSTR XX
X-REG INSTR XX
MASK BR XX
REG BR XX
IMMED R/W XX
REG R/W XX
AUX/STACK R/W XX
```

should be displayed. See section 6.3.1 for interpretations of the CPU Diagnostic.

This test runs continuously until either an error occurs or RESET is keyed.

When satisfied that a sufficient number of successful test passes have occurred (5 to 10 minutes), key RESET. The User Menu is reselected by pressing the appropriate SF Key after each diagnostic; any other diagnostic may then be selected.

12. Press SF'01

LOADING CONTROL MEMORY DIAG (DATE)

should be displayed for approximately 5 seconds; then,

```
*** CONTROL MEMORY DIAGNOSTIC***          MEMORY SIZE = 0XXXK
  NO ERR'S   PRESS 'P' TO PRINT ERRORS at ('T' FOR /204)

PRESS 'CONTINUE' TO START-
```

should be displayed. Press "CONTINUE" and the last line of the display should change to:

ADDRESSING TEST (PASS 0001)
Upon completion of this test, the prompt will be changed to:

MAT C&S TEST (PASS 0001)

Upon completion of this test, the last line of the display will change to:

ROWPAT TEST (PASS 0001)

These SF'01 tests are repeated in sequence until either an error occurs or RESET is keyed. When satisfied that a sufficient number of successful test passes have occurred (5 to 10 passes), key RESET. The User Menu should once again be reselected. See paragraph 6.3.2 for interpretations of the Control Memory diagnostic.

13. Press SF'02 (Data Memory Diagnostic)

The display should be similar to the one for the Control Memory diagnostic except that "CONTROL" will be replaced by "DATA" and the memory size will change.

SF'02 Data Memory Tests are also repeated in sequence until either an error occurs, or RESET is keyed. When satisfied that a sufficient number of successful test passes have occurred (5 to 10 passes), key RESET. See section 6.3.3 for interpretations of the Data Memory Diagnostic.

14. When all diagnostics listed in the User Menu have been completed, key RESET and select the Field Service Menu.

    To load the Field Service Diagnostic Menu, key SF'28, SF'29, SF'30 or SF'31 for disk addresses of Hex 310, B10, 320, or B20, respectively.

    After the appropriate SF' Key is pressed, the following will be displayed:

    KEY SF'?

      FIELD SERVICE DIAGNOSTIC MENU

'00 CPU DIAGNOSTIC	'05 MAT C & S 8
'01 ADDRESS 24	'06 ROWPAT 8
'02 MAT C & S 24	'07 REGISTERS
'03 ROWPAT 24	'08 AUXILIARY REGISTERS
'04 ADDRESS 8	'09 STACK REGISTER

    Note that User Diagnostics comprise merely the individual Field Service Diagnostic tests, not including the Field Service Register tests. Therefore, Register tests must be accessed from the Field Service Menu and run for any power-up and/or installation.

    Tests initiated from the Field Service Menu are normally used for troubleshooting purposes.

15. Key SF'07. Once the Register Diagnostic is loaded and begins to execute, key RESET and then function key 15. The Register Diagnostics are chained together by this operation and will run sequentially just as the diagnostics in the User Menu did, stopping only on an error or RESET.

See section 6.3.4 for interpretations of the Register Diagnostics.

16. After running the Field Service Register diagnostics, key RESET and load BASIC-2. BASIC-2 is loaded by keying the coresponding SF' key ('00 for 310, '01 for B10, '02 for 320, '03 for B20).

17. Once BASIC-2 is loaded and "READY (BASIC-2)" is displayed, the system platter should be removed from the disk drive.

18. Place the disk which contains the BASIC-2 Language Diagnostic (701-2261) in the disk drive and key LOAD, RUN EXECUTE, at each 2236D Terminal.

19. When satisfied that a sufficient number of successful test passes have occurred, key HALT/STEP.

20. After the microcode diagnostics and the BASIC-2 Language Diagnostics have been executed without failure, turn the CPU power OFF and insert all remaining I/O Controllers.

21. Install all the remaining peripherals in the system configuration. Check and adjust the voltages of the other peripherals as described in their specific maintenance manuals, making mechanical checks and adjustments where applicable.

22. Power up the system. Again run the diagnostics in this section to check for proper system operation. Execute the peripheral diagnostics described in section 6.

3.8 BOOTSTRAP

A BOOTSTRAP, by definition, is a "technique or device designed to bring itself into a desired state by means of its own action."

In general, the Wang MVP BOOTSTRAP, is a set of microcoded routines loaded in three 1024 x 8 bit Intel 2708 PROMs. The purpose of the BOOTSTRAP is to handle four system functions and make available certain subroutines which are used for I/O operations.

IMPORTANT:

The BOOTSTRAP described is release 2.2 (R1 PROMS) of the VP/MVP Bootstrap, implemented in all MVP Systems on September 1, 1978.

The four system functions handled by BOOTSTRAP are:

1) Master Initialization (Power-On).
2) Reset (Initiated by depressing the RESET key on the keyboard).
3) Control and Data Memory Parity Error Detection.
4) Loading the desired system software (i.e., diagnostics, or BASIC-2) from disk and initiating their execution.

An explanation of each of the above functions follows.

3.8.1 MASTER INITIALIZATION

Master Initialization begins by turning the CPU power switch to the ON position. A branch to Control Memory address 8003 (HEX), located in the BOOTSTRAP PROMs, is executed and the BOOTSTRAP routine begins controlling and performing its various tasks.

The tasks performed by the Master Initialization routine in BOOTSTRAP are:

a) To exercise the CPU to determine if any obvious malfunctions exist.
b) To verify the BOOTSTRAP PROMs still maintain the desired data.
c) To write zeros to all locations in Data Memory in preparation for subsequent Data Memory Reads.

If all Master Initialization tasks are completed satisfactorily, the prompt "MOUNT SYSTEM PLATTER CR/LF PRESS RESET" will be displayed.

3.8.2 RESET

Reset is initiated by depressing the RESET key located in the upper right hand corner of the keyboard. This action causes the execution of a branch to Control Memory address 8001 (HEX), located in BOOTSTRAP PROMs.

The tasks performed by Reset are:

(a) To pass control to the loaded system program currently loaded, located in Control Memory (BOOTSTRAP, Microcode Diagnostics, or BASIC-2).

(b) To allow the user to recover from any of the various system error conditions which may be encountered.

(c) To abort a BOOTSTRAP load.

Should task a) be called for, the user may expect those messages and/or actions designed into the particular system program, that is, a display a menu of user-selectable software (key Special Function), or for instance, a return to a starting point in the current software in Data Memory.

Otherwise, whenever task b) is to be performed, the user is expected to inform the BOOTSTRAP of what action to take (by keying a Special Function, for instance).

If the expected response does not occur on RESET, consult section 3.9.2 and 7.4.1.

3.8.3 CONTROL AND DATA MEMORY PARITY ERRORS

In both Data and Control Memory a bit has been set aside, called the parity bit, to aid in error detection.

In Control Memory, bit 24 is set aside for parity; it is turned on whenever the even number of the remaining bits turns on. This is called ODD Parity. This bit must be properly set when writing the instruction into Control Memory.

In Data Memory, a ninth bit is used in the same manner as described above. However, the hardware determines and sets this bit, whenever a write is executed into Data Memory.

Whenever the system detects bad parity in Control Memory, during an instruction fetch, a branch is made to location 8000, located in the BOOTSTRAP PROMS. The BOOTSTRAP will then perform its designated task.

Similarly, whenever the system detects bad parity in Data Memory, during a read from Data Memory, a branch is made to location 8002, located in the BOOTSTRAP PROMS. The BOOTSTRAP will then perform its designated task.

Whenever a trap to location 8000 and 8002 is executed by the system, the appropriate display is made.

3.8.4 LOAD SYSTEM FILES

Whenever the operator has made a response to the BOOTSTRAP requesting a system file to be loaded, the following tasks are performed.

a) Check if the disk is ready.

b) Verify whether the file exists on the mounted platter.

c) Load the file into Control and/or Data Memory.

d) Verify Control Memory checking instruction parity and built in CRC and LRC checksums.

e) Check Data Memory Parity.

f) Pass control to the newly loaded system file.

3.9 BOOTSTRAP ERROR MESSAGES AND RECOVERY

Three types of errors and five possible error messages can be reported by BOOTSTRAP. These error types--initalization, reset, and system--are discussed below.

3.9.1 INITIALIZATION ERRORS

The BOOTSTRAP, during Master Initialization, fails to display the complete

```
MOUNT SYSTEM PLATTER
PRESS RESET
```

message upon the CRT.

This error implies that some function of the MVP has failed. This may be either a CPU-related error or an I/O-related error.

In some cases, a device address may need to be corrected and the system powered on again.

The Master Initialization sequence is described on the following pages.

MASTER INITIALIZATION

Step-By-Step Breakdown of Function

CRT DISPLAY	SEQUENCE OF OPERATIONS	POSSIBLE FAILURES
CLEAR SCREEN	1. Power On Trap to 8003.	1. Hardware Trap Failure. Branch Instruction Failure.
"M"	2. Enable CRT, Clear Screen and Display "M".	2. CRT Address is wrong. I/O Register Failure. I/O Lines are Bad. CIO Instruction Failure.
"MO"	3. Test 24-Bit Parity Trap. Execute IC 800F which has Bad Parity.	Parity Checking Logic Failure. Hardware Trap Failure. TSP Instruction Failure (IC + 1 stored in stack) PC's may not hold IC retrieved from Stack. Compare Instruction Failure.
"MOU"	4. Test Subroutine Branch and Subroutine Return Instructions.	4. Subroutine Branch Instruction Failure. Subroutine Return Instruction Failure. Stack Failure.
"MOUN"	5. Clear CH, CL Parity Bits.	5. Write/Read Data Memory Failure.
"MOUNT"	6. Check File Registers.	6. Register Instruction Failure. Register Chip Failure. Compare Instruction Failure.
"MOUNT S"	7. Check PC Incrementing on the A-BUS.	7. PC Chip Failure. LPI Instruction Failure. Register Instruction Failure. A-Bus Increment Hardware Failure. Compare Instruction Failure.
	8. Test Auxiliary Registers.	8. Auxiliary/Stack Chip Failure. PC Chip Failure. Auxiliary Register Instruction Failure. Compare Instruction Failure.

MASTER INITIALIZATION
Step-By-Step Breakdown of Function (Continued)

CRT DISPLAY	SEQUENCE OF OPERATION	POSSIBLE FAILURES
"MOUNT SY"	9. Test Binary ALU.	9. Binary ALU Failure. AC, ACX, AI, SC or SCX Instruction Failure. Compare Instruction Failure.
"MOUNT SYS"	10. Test Stack.	10. Auxiliary/Stack Chip Failure. PC Chip Failure. Stack Instruction Failure. Compare Instruction Failure.
"MOUNT SYST"	11. Test Decimal ALU.	11. Decimal ALU Failure. DAC, DACI, DACX, DSC, DSCI or DSCX Instruction Failure. Compare Instruction Failure.
"MOUNT SYSTE"	12. Test Binary Multiply.	12. Multiply Hardware Logic Failure. M OR MI Instruction Failure. Compare Instruction Failure.
"MOUNT SYSTEM"	13. Test Shift.	13. Shift Logic Error. Compare Instruction Failure.
"MOUNT SYSTEM "	14. Verify PROM.	14. PROM Chip Failure.
"MOUNT SYSTEM P"	15. Zero 8-Bit Data Memory.	15. SR Failure. Bad IC's.
"MOUNT SYSTEM PLATTER" "PRESS RESET"	16. Write/Read Control Memory.	16. WCM/RCM Instruction Failure. Stack Failure. Auxiliary Register Failure. PC Chip Failure. SB Instruction Failure. Compare Instruction Failure.

MASTER INITIALIZATION
Step-By-Step Breakdown of Function (Continued)

CRT DISPLAY	SEQUENCE OF OPERATIONS	POSSIBLE FAILURES
	17. System Loops, diagnosing data and control memory. To resume depress RESET. (This aids in initializing the disk).	

3.9.2 RESET ERRORS

During the Reset function, when the operator has properly responded to the "KEY SF'?" message by keying the desired special function key:

The hexdigit display of the keyed special function did not appear upon the CRT.

This implies that the special function key was not depressed sufficiently, or the 2236D or 2236MXD may be defective, or an SF' key not defined was depressed.

NOTE:

During the RESET function, several of the SYSTEM ERROR messages may appear. If one does, consult the recovery procedure for that particular message, given in section 3.9.3.

The system reset sequence is described on the following pages.

SYSTEM RESET
Step-By-Step Breakdown of Function

CRT DISPLAY	SEQUENCE OF OPERATIONS	POSSIBLE FAILURES
	1. Reset has been keyed while BOOTSTRAP is in control.	1. Reset Trap Error.
Clear Screen "KEY SF'?"		
	2. Enable Keyboard (address = 01) and accept Special Function key input. Operator keys the desired SF key. NOTE: if any undefined SF' key is despressed, the "KEY SF" message re-appears and step 2 must be repeated.	2. Inactive SF is keyed. Keyboard address 01. I/O Register Failure. I/O Lines Failure. CRB or KFN Failure. Keyboard Failure.
*"KEY SF'?" name platter		
	3. Enable specified disk.	3. Improper disk address. I/O Register Failure. I/O Lines Failure. Disk Not Powered On. Disk Not Ready.
	4. Search disk for desired file. If file cannot be found, Step 2 is repeated.	4. Wrong Special Function key depressed. Wrong disk mounted.

*The name of the file to load and the platter to load from is displayed.

SYSTEM RESET
Step-By-Step Breakdown of Function
(Continued)

CRT DISPLAY	SEQUENCE OF OPERATIONS	POSSIBLE FAILURES
"KEY SF'?" name platter "COMMENT"	5. Load desired file from disk into Memory NOTE: System files should contain a comment block containing file date. If a disk error results, the system error message will appear. Consult Error Recovery, for proper procedure. If a parity error occurs during loading 'P' will be displayed and the previous sector will be reloaded. If no control memory data is found, skip to step 9.	5. I/O Register Failure. I/O Lines Failure. Disk Problems.
	6. Verify Control Memory. (Parity, LRC & CRC). If an error results, the system error message will appear. Consult Error Recovery, for proper procedure.	6. Memory Failure. WCM/RCM Instruction Failure.
	7. Check 8-Bit Data Memory. If an error results, the system error message will appear. Consult Error Recovery, for proper procedure.	7. Memory Failure. Read/Write Instruction Failure.
	8. Control is passed to loaded system file which now takes over control. Consult proper system file documentation. (Address = 3000)	

SYSTEM RESET
Step-By-Step Breakdown of Function
(Continued)

CRT DISPLAY	SEQUENCE OF OPERATIONS	POSSIBLE FAILURES
	9. Display Diagnostic Menu listing upon CRT.	
"KEY SF'?"		
	10. Enable Keyboard (address = 01) and accept Special Function key input. Operator keys the SF key of the desired diagnostic.	10. Inactive SF is keyed. Keyboard (address = 01) I/O Register Failure. I/O Lines Failure. CRB OR KFN Failure. Keyboard Failure.
"KEY SF'?" name platter		
	11. Go to Step 4.	

3.9.3 SYSTEM ERRORS

The third grouping of error conditions is reported to the operator via a SYSTEM ERROR message on the CRT.

First, should memory fail, the following message will appear:

```
*** SYSTEM ERROR MMMM XXXX ***
PRESS RESET
```

where MMMM - PECM = Parity Error Control Memory
PEDM = Parity Error Data Memory
VECM = Verify Error Control Memory
VEDM = Verify Error Data Memory
XXXX - Various error information pertinent to the type of error.

Secondly, a disk error will result in the following message being displayed:

```
*** SYSTEM ERROR DISK 00XX ***
PRESS RESET
```

where 00XX - is the Disk Error Code

The procedure used to recover from these SYSTEM ERRORS is similar. Therefore, the general procedure will be outlined and each error will be discussed.

The general procedure is:

a) Key RESET in response to the "PRESS RESET" message on line 2 of the CRT.

b) Choose one of the four following courses of action.

   1. Key SF'15 to resume, using the currently loaded system program (usually BASIC-2).

   2. Key SF'00-'05, '08-'013 to load BASIC-2 from disk 310, B10, 320, B20, 330, B30, 350, B50, 360, B60, 370 or B70.

   3. Key SF'16-'19 to load a diagnostic menu from disk 310, B10, 320, or B20, respectively.

   4. Key SF'28-'31 to load the Field Service Diagnostic menu from 310, B10, 320, or B20, respectively.

Use special caution when you choose #1 above: depending on what type of error and where it occured, BASIC-2 may not function properly in all cases.

The following discussion will outline each of the SYSTEM ERRORS and what may be done, in particular, to recover from them.

3.9.3.1 CONTROL MEMORY ERRORS

In both Data Memory and Control Memory, one bit has been set aside for parity error detection.

In Control Memory, the 24th bit (bit #23) of every micro-instruction is set aside for parity (it is turned ON whenever an even number of the remaining 23 bits turns on). This is called ODD Parity. This bit must be properly set when writing the instruction into Control Memory.

*** SYSTEM ERROR (PECM aaaa dddddd) ***

This error implies that bad parity was detected while the system was trying to execute an instruction from Control or BOOTSTRAP Memory.

Whenever the system detects bad parity in Control Memory (PECM message) during an instruction fetch, a branch is made to Control Memory address 8000 (HEX), located in the BOOTSTRAP PROMs. The BOOTSTRAP then performs its designated error routine and displays PECM aaaa, dddddd.

Bad parity may be the result of:

a) dropping of bits by Control/BOOTSTRAP Memory
b) picking up of bits by Control/BOOTSTRAP Memory
c) writing bad parity to Control Memory
d) defective parity checking logic

This error should be serious enough to warrant the executing of a Control Memory diagnostic. However, it may be possible to resume execution of the currently loaded system program. If the error is reported again, a Control Memory diagnostic should be run to locate the defective memory chip.

*** SYSTEM ERROR VECM aaaa ***

Case 1 (aaaa = 0000 thru 7FFF)

This error implies that the load of Control Memory from the disk was not successful. However, bad memory locations cannot be entirely ruled out.

This error is reported prior to a system program being given control and is the result of the program not being loaded properly into Control Memory.

The operator should attempt to reload that particular system program. However, should successive failures be reported, a Control Memory diagnostic should be run to determine if there are any bad memory chips. If no chips are reported defective, a CPU instruction may be failing, requiring a CPU diagnostic to be run.

Should the error be reported in low memory (i.e., address between 0000 and 0FFF) it may be necessary to change memory boards in order to load the diagnostic into memory.

Case 2 (aaaa = 8000 thru 83FF)

This error implies that the BOOTSTRAP Memory is not as expected.

This error may be caused from dropping or picking up bits by one or more of the three PROMs that make up the BOOTSTRAP.

Try to power on again, and if the problem still persists replace the BOOTSTRAP PROMs and perform a MASTER INITIALIZATION. If the error continues, the board may have failed or in some cases a microinstruction may have failed.

3.9.3.2 DATA MEMORY ERRORS

In Data Memory, a ninth bit allocated for each 8-bit byte is used in the same manner as described above. However, the CPU hardware determines the required state and sets this bit whenever a write is executed in Data Memory.

*** SYSTEM ERROR (PEDM ss.aaaa)***

This error implies that bad parity was detected during a read of Data Memory.

Whenever the system detects bad parity in Data Memory (PEDM message) during a read from Data Memory, a branch is made to Control Memory address 8002 (HEX), located in the BOOTSTRAP PROMs. The BOOTSTRAP then performs another error routine and displays PEDM ss.aaaa.

Bad parity may be the result of:

a) dropping of bits in Data Memory
b) picking up of bits in Data Memory
c) defective parity checking logic

This error should be serious enough to warrant the executing of a Data Memory diagnostic. However, it may be possible to resume execution of the currently loaded system program. If the error is reported again, a Data Memory diagnostic should be run to locate the defective memory chip.

*** SYSTEM ERROR (VEDM ss.aaaa)***

This error implies that the area of data memory used for system constants (verb tables, match constants, messages), was not loaded properly when BASIC-2 was loaded. However, bad memory locations cannot be entirely ruled out.

This error is reported prior to a system program being given control. The operator should attempt to reload BASIC-2. However, should successive failures be reported, Data Memory Diagnostics should be run to determine if there are any defective memory chips.

3.9.3.3 DISK ERRORS

*** SYSTEM ERROR DISK 00XX ***

There are several possible DISK errors that may occur while BOOTSTRAP is trying to load a particular system program. The only recovery procedure that should be taken is to attempt to reload the particular system program.

The possible disk errors are:

DISK 0082

Error: File not in catalog

Cause: The file to be loaded does not reside on the platter specified.

Recovery: Make sure that the proper platter is properly mounted, that the proper disk drive was specified, and that the proper special function key was pressed. Press RESET, as prompted, and select the appropriate special function.

DISK 0088

This is a WRONG RECORD TYPE ERROR which occurs during a load when the format of the record read does not conform to the bootstrap format.

To recover from this error:

a) Make sure that the proper platter is properly mounted, the the proper disk drive was specified, and the the program special function key was pressed. Press RESET, as prompted, and select the appropriate special function.

DISK 0090

Error: Disk Hardware Error

Cause: The disk did not recognize or properly respond to the system at the beginning of a read or write operation (the read or write has not been performed).

DISK 0091

Error: Disk Hardware Error

Cause: A disk hardware error occurred; i.e., the disk is not in file-ready position. This could occur, for example, if the disk is in LOAD mode or power is not turned on.

Recovery: Ensure that the disk is turned on and properly set up for operation. Set the disk into LOAD mode and then back into RUN mode, with the RUN/LOAD selection switch.

DISK 0092

Error: Disk Hardware Error

Cause: The disk did not respond to the system at the beginning of a read or write operation in the proper amount of time (time-out). The read or write has not been performed.

Recovery: Run program again. If error persists, reinitialize disk.

DISK 0093

Error: Disk Format Error

Cause: A disk format error was detected during a disk read or write. The disk is not properly formatted. The error can be either in the disk platter or the disk hardware.

Recovery: Format the disk again.

DISK 0094

Error: Format Key Engaged

Cause: The disk format key is engaged (the key should be engaged only when formatting a disk).

Recovery: Turn off the format key.

DISK 0095

Error: Seek Error

Cause: A disk-seek error occurred; the specified sector could not be found on the disk.

Recovery: Run program again. If the error persists, reinitialize (reformat) the disk.

DISK 0096

Error: Cyclic Read Error

Cause: A cyclic redundancy check error occurred during a disk read operation; the sector being addressed has never been written to or was incorrectly written.

Recovery: If the disk has been formatted, rewrite the bad sector or reformat the disk.

DISK 0097

Error: Longitudinal Read Error

Cause: A longitudinal redundancy check error occurred when reading a sector.

Recovery: Make sure the SYSTEM PLATTER is properly mounted in the operator specified disk unit. Key RESET, as prompted, and try to reload. If the error persists, try a backup platter.

DISK 0098

This is a DISK ADDRESSING ERROR which is caused when the disk sector being addressed is not on the disk.

To recover from this error

a) Make sure that the disk is ready and the SYSTEM PLATTER is properly mounted in the operator specified disk unit. Key RESET, as prompted, and try to reload.
b) If the problem persists, then BOOTSTRAP may be bad or the disk may have a problem.

NOTES:

SECTION 4
SYSTEM GENERATION

4.1 GENERAL

When the 2200MVP is powered on, an operator at terminal #1 has the responsibility to "Master Initialize" the system and to load/execute the partition/peripheral configuration suited to the current application(s).

The process of Master Initialization (loading the BASIC-2 Operating System) creates a preliminary single-partition system that is controlled exclusively from terminal #1. No devices connected to the system--other than terminal #1 and the system disk--are available until total system configuration takes place. Configuration is performed either by execution of the BASIC-language system utility called @GENPART, or by the BASIC statement $INIT (discussed in later text). As a part of Master Initialization, the system microcode (BOOTSTRAP) automatically loads and runs @GENPART, which is a file stored on the system disk. If @GENPART is not on the system disk, a READY message is displayed at terminal #1.

A system configuration created by either the standard @GENPART utility or by a customized version of @GENPART (using the $INIT statement) remains in effect until the system is reinitialized. Note that @GENPART is always assumed (by the BASIC-2 Operating System) to be the name of the system generation/configuration utility, whether Wang-written or user-written.

When @GENPART is initiated, parameters from the previous configuration (called 'current') are automatically loaded. If the Wang version of @GENPART is used, a list of user-selectable options and previously-saved configurations is displayed.

On completion of Master Initialization and System Generation/Configuration, terminal #1 switches to console mode and functions like all other terminals connected to the MVP Central Processor.

After configuring the system, at least one backup copy of the system disk should be made. By taking this step, a user might prevent system "down time" that could result from accidental damage to the original system disk.

The COPY or MOVE statements are used for duplication of the system disk. (A detailed explanation of the COPY and MOVE statements is given in the 2200VP/MVP Disk Reference Manual, WL# 700-4081)

4.2 SYSTEM POWER-UP, MASTER INITIALIZATION, AND GENERATING THE SYSTEM

The following explanation should provide the reader with enough information to power-up the system, Master Initialize the system, and configure the system.

4.2.1 POWER-UP

To begin, switch AC power ON in the Central Processor, Workstation #1, and the System Disk Drive. After power is applied to the system, the prompt appears:

```
MOUNT SYSTEM PLATTER
PRESS RESET
```

The system disk contains the BASIC-2 Operating System, as well as a variety of hardware diagnostics. When the disk drive achieves the ready state, steps may be taken to load the Operating System or hardware diagnostics via Special Function Keys on terminal #1. (Use of diagnostics is discussed in Chapter 6.)

Mount the system disk, then press the RESET key (located in the upper-right corner of the keyboard). The following prompt is displayed:

```
KEY SF'?
```

4.2.2 LOADING THE OPERATING SYSTEM

A Special Function Key must be depressed to specify the address of the disk drive in which the system disk is loaded.

The following options are available:

Key SF '00 to load BASIC-2 from the disk @ address 310 (Hex).
Key SF '01 to load BASIC-2 from the disk @ address B10 (Hex).
Key SF '02 to load BASIC-2 from the disk @ address 320 (Hex).
Key SF '03 to load BASIC-2 from the disk @ address B20 (Hex).
Key SF '04 to load BASIC-2 from the disk @ address 330 (Hex).
Key SF '05 to load BASIC-2 from the disk @ address B30 (Hex).
Key SF '08 to load BASIC-2 from the disk @ address 350 (Hex).
Key SF '09 to load BASIC-2 from the disk @ address B50 (Hex).
Key SF '10 to load BASIC-2 from the disk @ address 360 (Hex).
Key SF '11 to load BASIC-2 from the disk @ address B60 (Hex).
Key SF '12 to load BASIC-2 from the disk @ address 370 (Hex).
Key SF '13 to load BASIC-2 from the disk @ address B70 (Hex).

CASE #1: System Disk is a Diskette:

Normally, the leftmost diskette drive slot in the primary or default diskette unit is assigned Hex address 310 and the second drive slot is assigned Hex address B10. If there are two separate diskette units on the system, the leftmost drive slot on the second diskette unit is usually assigned Hex address 320; the second drive slot, Hex address B20.

CASE #2: System Disk is a Fixed/Removeable Disk Drive:

Normally, the fixed platter in the primary or default disk unit is assigned Hex address 310 and the removable cartridge is assigned Hex address B10. If there are two separate disk units on the system, the fixed platter in the second unit is usually assigned hex address 320; the removable cartridge, Hex address B20.

In either CASE #1 or CASE #2, approximately 15 seconds are required for the BASIC-2 Operating System to be loaded into Control Memory. While this takes place, the following message will appear on the display screen of terminal #1:

```
LOADING:  MVP BASIC-2 RELEASE X.X
```

When loading is complete, the system displays the "READY (BASIC-2)" message, unless the @GENPART partition-generation program is resident on the system disk. If such is the case, the @GENPART Partition Generator is automatically loaded after the BASIC-2 Operating System is loaded. (The @GENPART data file is normally on the system diskette.) Terminal #1 should then be ready for limited use, the other terminals are enabled only after configuring the system as desired with @GENPART or $INIT.

If the wrong SF Key is depressed (i.e., if the system disk is mounted at address 310, but the operator depresses SF Key 01), an error message will be displayed:

```
***SYSTEM ERROR (DISK 00XX)***
PRESS RESET
```

Recovery from such errors may be accomplished by simply pressing RESET, followed by the correct Special Function key. If RESET fails, turn the Central Processor OFF then ON again. If this latter step is required, Master Initialization will be repeated per paragraph 4.2.

In some instances, the Special Function key code is displayed. This may indicate that an incorrect disk address was specified, or that a disk I/O controller has failed. Check the I/O controller address, or replace the I/O controller if that board is suspected to be defective.

4.2.3 PARTITION GENERATION

Configuration parameters must now be passed to the Operating System. As stated previously, the @GENPART program is automatically loaded and executed when it is resident on the system disk (no operator intervention required). If such is the case, immediately following Master Initialization (RESET, KEY SF'?) the @GENPART menu will be displayed at terminal #1, instead of the READY message. (The "READY (BASIC-2)" message will appear once @GENPART has finished execution.) If so desired, the user may elect to customize the BASIC language @GENPART program, thus providing more suitable display prompts (etc.) for his specific needs.

Basically, using either method of partition generation (@GENPART or $INIT), the operator has control over the following:

(Explanations follow in subsequent text)

* Number of partitions
* Size of each partition
* The terminal associated with each partition
* The "programmability" of each partition
* The "bootstrap" program for each partition
* Addresses of the peripherals connected to the system
* Access to peripherals
* The "system message"

Standard Partition Generation:

The standard Wang "@GENPART" program has two important provisions for user convenience:

1) If partition-generation modules have been previously defined, a list of those module names will be displayed on the @GENPART menu screen. The user can select and load one of these modules using the following procedure:

   a) First, type in the name of a previously-saved configuration module, then press RETURN.

b) Depress Special Function key '15, causing the system to begin execution with the presently-loaded partition configuration module.

2) If the user wishes to define a new partition module, he can do so by depressing any of the other Special Function keys; this action initiates partition generation.

NOTE:

It may be useful to depress the large FN (HELP) key in the upper-left part of the workstation key pad; descriptive information will be automatically provided on the screen that explains the partition generation process. (Depress the RETURN key to see successive screenloads of instructions.)

When the BASIC-2 Operating System is fully loaded, the @GENPART menu should appear:

```
                                          LIST OF OPTIONS:
LIST OF STORED CONFIGURATIONS  (# PARTITIONS)
     1.  current                  (X)     SF'00 - CLEAR PARTITIONS
     2.  ....                             SF'01 - CLEAR DEVICE TABLE

                                          SF'02 - DIVIDE MEM. EVENLY

                                          SF'04 - EDIT PARTITIONS
                                          SF'05 - EDIT DEVICE TABLE
                                          SF'06 - EDIT $MSG

                                          SF'08 - LOAD CONFIGURATION
                                          SF'09 - SAVE CONFIGURATION
                                          SF'10 - DELETE CONFIGURATION

                                          SF'15 - EXECUTE
                                             FN - HELP


CONFIGURATION "CURRENT" LOADED.  NAME OF CONFIGURATION TO LOAD? _______
```

DESCRIPTIONS OF @GENPART SPECIAL-FUNCTION OPTIONS

SF' 00 - Clear Partitions: Clears partition-configuration parameters currently in memory, allows the user to specify the total number of terminals and the total number of partitions in each bank, then automatically advances to SF'04 (Edit Partitions). The Master Device Table is not altered when this function is selected. Any number of partitions between one (1) and sixteen (16) that will not exceed the available memory capacity is allowable. (Note that since each partition must be 1.25K (16 partitions, max.) and since there is a 3K Operating System overhead space to account for, the minimum memory size that will accommodate 16 partitions is (1.25K x 16 partitions) + 3K = 23K.

SF' 01 - Clear Device Table: Clears Master Device-Table parameters currently stored in memory, resets default peripheral addresses to Hex 215 (printer), 310 (System Disk), and 320 (secondary disk), allocates these devices to all users (specifies common access), then advances to SF'05 (Edit Device Table). (Default device addresses can be edited, if necessary, using SF' 05.)

SF' 02 - Divide Memory Evenly: Divides remaining User Memory equally among the number of partitions specified with SF' 04.

SF' 04 - EDIT Partitions: Displays and allows editing of partition parameters such as size, terminal assignment, programmability, and name of bootstrap program. SF'04 does not allow addition or deletion of defined partitions in an existing configuration.

Descriptions of EDIT functions follow:

1. Number of partitions: From one (1) to sixteen (16) partitions may be created.

2. Size of partitions: Any size greater than--or equal to--1.25 kilobytes is allowable. This specification is made in 256-byte (1/4K) increments. The maximum allowable size is 61K (64K minus 3K for housekeeping).

3. The terminal associated with each partition: Any terminal number from 0 to 8 is valid; terminals 1 to 8 are the actual user-terminals connected to the system; terminal number 0 is a non-existent "dummy" or "null" terminal. All partitions must have a terminal assignment, even if the 0 (null; non-existent) terminal is specified, and even if there are partitions that will contain "background jobs" that never print on the CRT or require keyboard entry. In general, any singular partition may be placed in assignment with any singular terminal; however, a singular terminal may be specified to be in assignment with several partitions, in order to create a multiple-partition "personal" system. In general, the lowest-numbered partition(s) to be placed in a state of assignment with a terminal should contain the foreground (interactive) jobs for that terminal. Background jobs should be placed in the higher-numbered partitions within that assignment. Only the terminal that has been specified to be in a state of assignment with a particular partition can list or modify the program in that partition. Finally, note that while it is possible for partitions to access global program text and modify global variables, it is not possible for non-global partitions to list or modify program text in a global or universal-global partition.

4. Programmability of partitions: Any partition can be specified for the "disabled programming" mode, whereby that partition is inhibited from certain operations. Terminals attached to "disabled programming" partition(s) are inhibited from entering or modifying program text, or from performing certain other system operations. Thus, the operator is prevented from inadvertent or unauthorized use of protected or restricted programs and data.

5. Bootstrap programs for partitions: Any program that resides on the system disk can be loaded into a partition and run automatically when a configuration is executed. When no bootstrap program is specified for a partition, the 'READY' display will appear on the CRT once the configuration has been executed.

SF' 05 - EDIT Device Table: Displays and allows editing of device addresses for all peripherals. All peripherals connected directly to I/O controllers must be specified in the Master Device Table (this, of course, excludes terminals and local printers connected to them). Console device addresses (i.e. Hex 005--CRT, 001--keyboard, 204--local printers) are not specified in the Master Device Table, nor may they be specified using SF'05; these are specified in each partition device table. Partition Device-Table specifications and modifications are discussed later in this section.

By default, all system peripheral devices listed in the Master Device Table are available to all partitions. However, devices can be given exclusive assignmment with one partition until the next system configuration is executed. This is accomplished by entering, in the Master Device Table, the number of the partition that is to have control of the device. For disk controllers that respond to more than one address, only the primary address must be specified in the Master Device Table (i.e. Hex 310 but not B10, 350, 390, etc.). For all other multi-address controllers, all valid addresses must be listed.

SF' 06 - EDIT $MSG: Displays and allows editing of a user-defined broadcast message that will be displayed on each terminal's CRT whenever the READY message is displayed. The user-defined message is displayed on line 0 of the CRT, immediately above the "READY" message.

SF' 08 - Load Configuration: Loads a named configuration from the Configuration File, which is located on the system disk. To modify and/or execute any previously-defined configuration other than "current", this option must be used.

SF' 09 - Save Configuration: Save a system configuration in the Configuration File under a user-specified name (up to eight characters in length). If the user specifies a configuration name already used, @GENPART will verify that the user desires to replace the old configuration on disk file with the configuration currently in memory.

SF' 10 - Delete Configuration: Deletes a configuration from the Configuration File on the system disk.

SF' 15 - Execute Configuration: Allows the operator to review first, and then to execute, a configuration. This configuration will be automatically saved in the Configuration File under the name "current" when the configuration is executed. Once a configuration has been executed, the system may be reconfigured again only after the Master Initialization procedure has been repeated.

FN - Help: Displays @GENPART operating instructions.

4.2.4 GENERATING A SAMPLE CONFIGURATION

The following example illustrates how, typically, @GENPART can be used to configure a system. In this example, a 2200MVP with 48K bytes of User Memory, three terminals, and telecommunications option are to be configured. The configuration (named "SAMPLE") will have four partitions. A 15K-byte telecommunications program will be designated for automatic bootstrapping, as a background job sharing terminal #1. Disabled programming will be specified for this partition so that it cannot be modified inadvertently. Remaining memory will be divided equally among the other three partitions.

In general, the order of executing @GENPART options is: (1) SF'08--to load a configuration, (2) SF'00--to modify this configuration by adding or deleting partitions, (3) SF'04--to create the new partition parameters, (4) SF'05--to create the Master Device Table, (5) SF'06--to create the broadcast message, (6) SF'09--to save the configuration with a name other than 'current', and (7) SF'15--to execute the configuration. Therefore, in the example that follows, these options are discussed in their probable order of use.

Load a Configuration (SF'08) (When @GENPART is first executed, this display occurs without pressing SF'08)

```
        LIST OF STORED CONFIGURATION (#PARTITONS)
                    current          (1)

CONFIGURATION 'current' LOADED. NAME OF CONFIGURATION TO LOAD? ____
```

The last configuration executed (called 'current') is automatically loaded. To load any other configuration, enter its name, then press RETURN. Since, in this example, a completely new configuration is to be created, press SF'00--Clear Partition.

Clear Partitions (SF'00) The program responds with a display that requests the total number of terminals that are to be configured into the system and the number of partitions that will be created. Available User Memory is automatically calculated and displayed. Note that the 3K of Operating System overhead space in bank #1 is automatically deducted from the available-memory quantity. Remaining memory is updated and displayed as memory is allocated to the partitions.

```
AVAILABLE USER MEMORY = 45K
REMAINING USER MEMORY = 45K
NO. OF TERMINALS?
NO. OF PARTITIONS?
```

In this example, there will be four partitions; enter 4 in response to the "NUMBER OF PARTITIONS?" prompt, and then key RETURN. The program automatically invokes option SF'04 (Edit Partition) to allow the editing of partition parameters.

Edit Partitions (SF'04) This option displays default parameters for all partitions and initiates a cycle of prompts for the altering of these parameters. The cycle recurs until another option is selected. The user is thus allowed to modify parameters for each partition. The display is updated each time an item is entered.

```
PARTITION SIZE (K)     TERMINAL PROGRAMMABLE PROGRAM
   1      _____            1              Y
   2      _____            2              Y
   3      _____            3              Y
   4      _____            4              Y

EDIT WHICH PARTITION (default = 1)?
```

In this example, the telecommunications program will be run in partition #2. Begin, therefore, by editing the parameters for partition #2. Enter 2, then key RETURN. An asterisk (*) appears beside the number of the partition whose parameters are being edited, and the following series of prompts will be displayed in succession at the bottom of the screen:

```
PARTITION SIZE (default = 0)?
```

Any value greater than 1.25K and less than the amount of remaining User Memory is a valid response. Note that the default value (zero kilobytes) is not a legal value when a user specifies each partition size individually; however, when all remaining memory is to be divided evenly, a partition size of 0 (zero) is legal.

The telecommunications program that is to be run in this partition will require 15K. To allocate 15K of User Memory to partition #2, enter 15, then key RETURN. The following prompt should be displayed at the bottom of the screen:

```
TERMINAL (default = 2)?
```

The telecommunication program will be a background job controlled at terminal #1. To establish assignment between this partition (partition #2) and terminal #1, enter 1 and key RETURN. The following prompt then occurs.

```
ENABLE PROGRAMMING (Y or N)?
```

By default, programming is allowed for all partitions; however, to prevent inadvertent modification of the telecommunications program, "disabled programming" will be specified for partition #2. To specify disabled programming mode for this partition, enter N, then key RETURN. The name of a program to be automatically loaded into this partition is now requested as follows:

```
NAME OF PROGRAM TO LOAD?
```

The name of the telecommunication program that will be run in partition #2 is "TELE-COM". Enter "TELE-COM" and then key RETURN. When the configuration is executed, the telecommunications program will be automatically loaded from the system disk into partition #2, and will then be run.

At this point, editing of the parameters for partition #2 is complete. Partitions #1, #3, and #4 require further modification. Remaining memory is to be divided evenly between those remaining partitions. Press SF'02 (Divide Memory Evenly) and the remaining 30K should be distributed evenly among partitions #1, #3, and #4. The system returns to the initial "EDIT WHICH PARTITION?" prompt. All that remains is to establish assignment between terminal #2 and partition #3, and between terminal #3 and partition #4. Enter these values into the table for partitions #3 and 4. Upon completion of this operation, the table should appear as follows:

PARTITION	SIZE (K)	TERMINAL	PROGRAMMABLE PROGRAM
1	10.00	1	Y
2	15.00	1	N
3	10.00	2	Y
4	10.00	3	Y

Once all partitions have been edited, SF'05 is used to leave the "Edit Partition" cycle and then invoke the "Edit Master Device Table" option. Note that it is legal to exit the Edit Partition Cycle (SF'04) without answering all prompts; in this case, the specified default values are used by @GENPART and the Operating System.

Edit Device Table (SF'05) This option displays the default values resident in the Master Device Table. Notice that by default, every device specified is available to all users.

```
DEVICE      PARTITION          DEVICE      PARTITION

1.          /215               all         17.

2.          /310               all         18.

3.          /320               all         19.

 .                                           .
 .                                           .
 .                                           .

16.                                         32.

   EDIT WHICH ENTRY (default = 1)?
```

In this example configuration, a fourth device (telecommunications controller) is used, in addition to the three default devices. The device address of this controller is Hex 01C. To specify this device in the Master Device Table, enter "4", then key RETURN. An asterisk (*) will appear beside the number 4 in the table. Several prompts are displayed in succession at the bottom of the screen; the table is updated each time an item is edited. The user is requested to enter the device address with the following prompt:

```
DEVICE ADDRESS (default = /000,/000 to delete entry)?
```

Enter /01C, then key RETURN. Another prompt now appears, and the user is requested to specify assignment for the peripheral device with one or more partitions:

```
ALLOCATE DEVICE TO WHICH PARTITION (default = all)?
```

For this example, enter a "2", then key RETURN to allocate the peripheral and its controller to partition #2. This display cycle will continue, in order to allow the user to edit all entries in the Master Device Table. When the parameters for all peripheral/partition allocations have been specified, the user can select another S.F. option to exit the "Edit Device Table" mode.

Broadcast Message (SF'06) When SF'06 is depressed, the following display occurs at the bottom of the CRT display.

```
BROADCAST MESSAGE:

----------------------------------------------------------------
```

NOTE:

The system is in EDIT mode during entry of the broadcast message. While in EDIT mode, all S.F. Keys revert to their system-defined EDIT functions. The S.F. Keys cannot be used for their @GENPART-defined functions until the entry of the broadcast message is complete and the system leaves the EDIT mode.

Any message in which the number of characters and spaces does not exceed the number of dashes displayed on the CRT is valid. For this example, enter * * * THE SYSTEM WILL GO DOWN AT NOON * * *. Now key RETURN. When the broadcast message has been entered, all partition-generation parameters for the example configuration have been specified. This configuration can now be saved for later use (SF'09) or executed (SF'15). Pressing SF'09 allows the operator to save this configuration on disk under a unique name.

Save Configuration (SF'09) When SF'09 is depressed, the following display occurs at the bottom of the CRT display.

```
CHECK CONFIGURATION TO SAVE.  CONFIGURATION NAME? ----------
```

NOTE:

In order to save a configuration, the system diskette must be write-enabled (i.e., unprotected; the write-protect notch must be covered). If the system disk is a hard disk, note that the hard disk is always write-enabled.

The configuration currently in memory will automatically be saved under the name 'current' (if the system platter is write-enabled). However, each time a new configuration is executed, the new parameters replace the old parameters in the 'current' file. In order to save a configuration so that it can be retrieved for future use, it should be saved under a unique name. The name to be used for this sample configuration is, appropriately, "SAMPLE". Enter "SAMPLE", then key RETURN. The configuration is saved under the name SAMPLE.

Execute Configuration (SF'15) Once all parameters of a configuration have been defined, the system configuration can be executed. To execute a configuration, press SF'15. The configuration table will appear near the bottom of the CRT, along with a prompt requesting the operator to verify the configuration parameters to be executed.

```
CHECK CONFIGURATION OK TO EXECUTE (Y or N)?
```

If Y (RETURN) is entered, this configuration will be executed. If N (RETURN) is entered, the system returns to the beginning of the "Edit Partition" cycle (SF'04).

NOTE:

Once executed, a configuration can only be changed by first Master Initializing the system, and then, by specifying the new parameters.

Delete a Configuration (SF'10)

Since this exercise generates only a sample configuration, the configuration should be deleted, in order to save more space for actual configuration records. The following prompt will request which configuration to delete.

```
DELETE WHICH CONFIGURATION?
```

Enter "SAMPLE", then key RETURN; the configuration will be deleted from the system disk.

4.3 GENERATING EVENLY-DIVIDED PARTITIONS: A SAMPLE PROGRAM

Load the MVP BASIC-2 Operating System by keying the appropriate SF' key on terminal #1. Approximately thirty seconds later, the following should appear on terminal #1's display:

```
                    *** PARTITION GENERATION ***

                                                  OPTIONS:
LIST OF STORED CONFIGURATION (#PARTITIONS)
                                        SF'00 - CLEAR PARTITIONS
     1.  current            (2)         SF'01 - CLEAR DEVICE TABLE

                                        SF'02 - DIVIDE MEM. EVENLY

                                        SF'04 - EDIT PARTITION
                                        SF'05 - EDIT DEVICE TABLE
                                        SF'06 - EDIT $MSG

                                        SF'08 - LOAD CONFIGURATION
                                        SF'09 - SAVE CONFIGURATION
                                        SF'10 - DELETE CONFIGURATION

                                        SF'15 - EXECUTE
                                           PN - HELP

CONFIGURATION "current" LOADED.  NAME OF CONFIGURATION TO LOAD? _________
```

Key SF'00 to initialize all terminals and clear the partitions. The following will then appear:

```
                    *** PARTITION GENERATION ***


AVAILABLE USER MEMORY = 61K () () ()
REMAINING USER MEMORY = 61K () () ()  OPTIONS:
NO. OF TERMINALS? ____                   SF'00 - CLEAR PARTITIONS
NO. OF PARTITIONS? ____                  SF'01 - CLEAR DEVICE TABLE

                                         SF'02 - DIVIDE MEM. EVENLY

                                         SF'04 - EDIT PARTITION
                                         SF'05 - EDIT DEVICE TABLE
                                         SF'06 - EDIT $MSG

                                         SF'08 - LOAD CONFIGURATION
                                         SF'09 - SAVE CONFIGURATION
                                         SF'10 - DELETE CONFIGURATION

                                         SF'15 - EXECUTE
                                            FN - HELP
```

Answer the prompt "NO. OF TERMINALS?" prompt with the number of terminals on the system, then answer the "NO. OF PARTITIONS?" prompt. Enter the appropriate number, then key EXECUTE.

```
                    *** PARTITION GENERATION ***

AVAILABLE USER MEMORY = 61K
REMAINING USER MEMORY = 61K                    OPTIONS:
PARTITION SIZE (K) TERMINAL PROGRAMMABLE           SF'00 - CLEAR PARTITIONS
                                                   SF'01 - CLEAR DEVICE TABLE
PROGRAM
  1          -          1          Y                SF'02 - DIVIDE MEM. EVENLY
  2          -          2          Y
                                                   SF'04 - EDIT PARTITION
                                                   SF'05 - EDIT DEVICE TABLE
                                                   SF'06 - EDIT $MSG

                                                   SF'08 - LOAD CONFIGURATION
                                                   SF'09 - SAVE CONFIGURATION
                                                   SF'10 - DELETE CONFIGURATION

                                                   SF'15 - EXECUTE
                                                      FN - HELP

CHECK CONFIGURATION.  OK TO EXECUTE (Y OR N)?
```

Key SF'02 - Divide memory evenly. Available memory should be apportioned equally among the number of terminals entered in the above step. The following should appear:

```
                    *** PARTITION GENERATION ***


AVAILABLE USER MEMORY = 61K
REMAINING USER MEMORY = 0 K
                                               OPTIONS:
                                                SF'00 - CLEAR PARTITIONS
PARTITION SIZE (K) TERMINAL                     SF'01 - CLEAR DEVICE TABLE
   1       30.50      1
   2       30.50      2                         SF'02 - DIVIDE MEM. EVENLY

                                                SF'04 - EDIT PARTITION
                                                SF'05 - EDIT DEVICE TABLE
                                                SF'06 - EDIT $MSG

                                                SF'08 - LOAD CONFIGURATION
                                                SF'09 - SAVE CONFIGURATION
                                                SF'10 - DELETE CONFIGURATION

                                                SF'15 - EXECUTE
                                                   FN - HELP

EDIT WHICH PARTITIONS (default = 1)?
```

Finally key SF'15 (EXECUTE). A prompt will appear "CHECK CONFIGURATION. OK TO EXECUTE (Y OR N)?". Enter "Y" and key EXECUTE if the configuration is correct. All terminals should now display "READY (BASIC-2)": each terminal can now be used as an independent processor, a "personal" system.

4.4 CUSTOMIZED PARTITION GENERATION

The user may, if he so desires, write his own partition-generation utility. Further description of this approach is given below; also, refer to the BASIC-2 Language Reference Manual (WL# 700-4080, 80.1, & 80.2) for a detailed description of the $INIT statement.

Streamlining the @GENPART Program:

Once initially defined and stored on disk, configuration parameters in a specified system configuration can be passed to the Operating System and executed automatically during Master Initialization, with no operator intervention. REM statements near the beginning of the @GENPART program will tell the user how to streamline the program to operate in this manner.

Use of the $INIT Statement:

When the Wang utility @GENPART does not meet a user's needs, it is also possible to create a customized configuration program using the BASIC-2 statement $INIT.

$INIT

General Forms:

Program Mode Statement: (Pass initial configuration parameters to the Operating System)

$INIT (alpha-1, alpha-2, alpha-3, alpha-4, alpha-5 (, alpha-6)

Where: alpha = literal-string
alpha-variable

Immediate Mode Statement: (Reconfigure system)

```
$INIT "password"
```

Where: password = System reconfiguration password; this must be a literal string.

Once configured, the system can be reconfigured only by executing the "$INIT password" statement at terminal #1. Control is passed to the system bootstrap; the message

```
MOUNT SYSTEM PLATTER
PRESS RESET
```

is displayed, and the system can be loaded and reconfigured as if it had just been powered-up.

In order to protect against inadvertent reconfiguration, $INIT can be executed at terminal #1 only. Additionally, reconfiguration is password-protected. An error results if the proper password is not included in the immediate-mode $INIT command and reconfiguration does not occur. The default password is "SYSTEM"; thus, the operator on terminal #1 would enter:

```
:$INIT "SYSTEM"
```

in order to pass control to the system BOOTSTRAP. The password can be changed by passing a new password to the OS via the 'alpha-6' parameter in the $INIT program statement (explanation follows). However, if the system is powered off, or if an immediate mode $INIT is executed, the password reverts back to "SYSTEM". The password can be from 1 to 8 characters in length.

The user need not be concerned with the complex form of $INIT, unless a customized partition-generator program is required. It is recommended that the Wang-supplied utility, "@GENPART," or a modified version of it be used for configuring the system, to ensure that the proper configuration parameters are passed to the Operating System. If $INIT parameters are not properly set, the system may be erroneously configured, produce unpredictable errors, and/or lock out all terminals. In order to restore operation following any of these error conditions, it may be necessary to power the CPU off and on (reinitialize the system).

Configuration parameters are defined as follows:

alpha-1 = size of each partition.

Length of string = 17.
Size = binary value indicating number of 256-byte pages of memory allocated for a partition.
Byte 1 = size of partition 1.
Byte 2 = size of partition 2.
.
.
.
Byte n = size of partition n.
Byte n+1 = HEX (00).

alpha-2 = terminal number for each partition.

Length of string = 16.
Terminal number = (in binary) of terminal assigned to a partition.
Byte 1 = terminal number for partition 1.
Byte 2 = terminal number for partition 2.
.
.
.
Byte n = terminal number for partition n.
Remaining bytes must = HEX (00).

alpha-3 = partition modes.

Length of string = 16.
Mode, bit 01 = 1 if and only if programming is not allowed on this partition.
Mode, bit 02 = 1 if and only if a program is to be bootstrapped into this partition.
Byte 1 = mode of partition 1.
Byte 2 = mode of partition 2.
.
.
.
Byte n = mode of partition n.

alpha-4 = bootstrap program name for each partition.

Length = 128 bytes.
Bootstrap program name = 8-byte literal-string specifying the program to be automatically loaded and run after partition generation.
1st 8 bytes = bootstrap name for partition 1.
2nd 8 bytes = bootstrap name for partition 2.
.
.
.
Nth 8 bytes = bootstrap name for partition n.

alpha-5 = device table.

Length of string = 99.
A device is specified by 3 bytes.
1st byte, low 4-bits = device-type (disk must be 3 or B).
2nd byte = physical device-address.
3rd byte = number of the partition for which the device is to be opened (0 if none).
1st 3 bytes = device specification for device 1.
2nd 3 bytes = device specification for device 2.
.
.
.
Nth 3 bytes = device specification for device n.
(N + 1) 3 bytes = 000000_{16}

alpha-6 = reconfiguration password.
Length of string = 8
1st eight bytes are the password.

Example of Valid Syntax:

```
$INIT "SYSTEM"
10 $INIT (S$,T$,M$,N$(),D$)
20 $INIT (S$,T$,M$,N$(),D$, P$)
```

4.5 COPYING THE SYSTEM DISK

Using Floppy Disk:

1. Be sure the Write-Protect Notch on the backup diskette is covered (the diskette must be unprotected, write-enabled). Insert the backup diskette into the leftmost slot of the primary diskette unit (address 310). Ensure that the Write-Protect Notch on the system disk is uncovered (protected from write operations, write-disabled) and insert the system diskette into the second drive slot.

2. The backup diskette must be formatted before any information can be written on it. The FORMAT button is surrounded by a protective ring to prevent accidental activation of the formatting procedure; this is a safety feature. (The formatting operation erases any data stored on the diskette.) To format the diskette, use the tip of a pen or pencil to depress the FORMAT button on the disk control panel, located above Drive #1. The FORMAT button must be held in for approximately $1/10^{th}$ of a second; the Format lamp above the drive slot should light.

3. When formatting has been completed, a message will be displayed to that effect. Enter COPY RF or MOVE RF and then RETURN to create a backup copy of the system disk.

Using a Hard Disk Platter -- 2260C, 2260BC, 2280 ONLY:

1. Insert the backup removable cartridge into the disk drive (address Hex B10). Note that the system disk (to be copied) is the fixed platter, resident in the same disk drive.

2. The backup cartridge must be formatted before any information can be written on it. (The formatting operation erases any data stored on the disk.) To format the backup removable cartridge, clear the CPU and then load "@FORMAT" from the system disk.

EXAMPLE: CLEAR (Return)
LOAD DCF "@FORMAT" (Assuming default address to be Hex 310)
RUN (Return)

3. When formatting has been completed, a message will be displayed to that effect. Enter COPY FR or MOVE FR and then RETURN to create a backup copy of the system disk.

Using a Hard Disk Platter -- 2260B ONLY:

1. Insert the backup removable cartridge into the disk drive (address Hex B10). Note that the system disk (to be copied) is the fixed platter, resident in the same disk drive.

2. To format the backup removable cartridge, place the platter-select switch, located on the disk processor chassis front panel, in the "UP" position (this selects the removable cartridge). Turn the format KEY switch to the right (clockwise). Depress the yellow format button located next to the KEY switch. The yellow lamp located next to the yellow pushbutton switch should illuminate, indicating that formatting is in-process. When the yellow lamp extinguishes--and the red error lamp should not be on at this time--formatting is complete and the key switch should be turned off (to the left, counter-clockwise).

3. Enter COPY FR or MOVE FR and then RETURN to create a backup copy of the system disk.

4.6 MODIFYING DEVICE TABLE ENTRIES

Master Device Table Modifications:

Refer to the EDIT DEVICE TABLE function (SF'05) in the @GENPART discussion given earlier in this section.

Partition Device Table Modifications:

Device Table entries can be modified either explicitly, with a SELECT statement, or implicitly with a CLEAR command, the RESET key, or Master Initialization of the system. In general, therefore, Partition Device Table entries remain in effect until one of the following operations is performed:

- A SELECT statement is executed explicitly redefining one or more specified entries
- A CLEAR command with no parameters is executed
- The system is Master Initialized (see below);

Whenever necessary, the Partition Device Table can be displayed for debugging purposes by using the BASIC statement LIST DT (List Device Table).

LIST DT displays, in hexadecimal notation, the device table belonging to the partition/terminal originating the LIST DT statement. The Partition Device Table is displayed at the requesting terminal. More detailed information concerning partition device-table modifications can be found in the 2200MVP Reference Manual: WL#700-4080

4.7 SPECIAL PROGRAMMING CONSIDERATIONS

4.7.1 Time-Dependent Software

1. The execution time of a given program varies from one machine to another. Execution on the MVP depends upon the current load of the CPU.
2. 2236D CRT refresh speed, 19.2 Kilobaud, is much slower than in 2226 CRTs. Thus, programs written to update the entire screen may affect the operating speed of the system.

3. LINPUT rather than KEYIN is recommended for data entry, since response time with KEYIN will vary, and LINPUT requires no CPU processing between keystrokes.

4. Using FOR/NEXT loops for delaying, (e.g., maintaining a message on the screen for a specified amount of time) uses excessive CPU time. Delay time varies depending upon the current work load of the CPU. Use of the SELECT P statement is recommended.

5. Instrumentation that is critically timed by the program may not work properly.

4.7.2 Peripherals

1. For line printers, plotters, 2228B and any other device that must be allocated to a specified user for a period of time, new $OPEN and $CLOSE statements are provided. Other than making certain that these statements are added, the programmer need not change the body of a program.

2. All Console Input, INPUT, and LINPUT statements utilize 2236MXD controllers. Therefore, these statements may not be used with the Model 2250 or telecommunications-control boards. This means, further, that the echo characters may not be sent to the line printer.

4.7.3 $GIO Restrictions

1. CBS is not issued to the 2236MXD.

2. Input not allowed from 2236MXD (i.e., console keyboard).

3. Timeouts and delays are allowed for output; however, the timeout or delay value is a minimum time. The value applies to the execution time allocated to this program; if other programs are executing, the actual delay time will be longer than specified.

4. There is an implicit timeout (with error) of 1 millisecond for input (non-MXD). A timeout of up to 10 ms can be specified.

4.7.4 I/O Statement Restrictions

The following chart defines which devices the MVP Operating System permits the statement to communicate with. ERR #48 results when a BASIC statement addresses an illegal device.

STATEMENT OR OPERATION:	2236D TERMINAL KEYBOARD	2236D TERMINAL CRT	2236D TERMINAL LOCAL PRINTER	DEVICES OTHER THAN 2236D TERMINALS
Console Output*		X	X	X
PRINT		X	X	X
PRINTUSING		X	X	X
HEXPRINT		X	X	X
LIST		X	X	X
PLOT		X	X	X
Console Input	X			
INPUT	X			
LINPUT	X			
KEYIN	X			X
$IF ON/OFF	X			X
$GIO		X	X	X
SELECT ON (interrupt)				X
Disk Statements				X

*Console Output (keystroke echo, error, END, STOP messages, and LINPUT and INPUT prompts) is always directed to the terminal CRT except for TRACE output which can be selected to another device (such as a printer).

4.7.5 Default Disk Address

Unlike the 2200VP, whose default disk address is always /310 after power on, the MVP's default disk address after power on is set to the address of the disk from which the system was loaded. That is

SF'00 sets default address to	/310
'01	/B10
'02	/320
'03	/B20

After partition generation, the default disk address for each partition is set to the default disk address of partition #1 at the time of partition generation.

4.7.6 Continue

The MVP supports CONTINUE as an Immediate Mode statement rather than a command. Thus, CONTINUE need not be the only statement on a line; however, no statements may follow CONTINUE on the Immediate Mode line. This feature of CONTINUE is useful when program execution is to be continued with the terminal released to another partition. For example,

```
:$RELEASE TERMINAL : CONTINUE
```

4.8 PROGRAMMING THE 2209A ON THE 2200MVP

The present $GIO sequences, documented in table 4-1 of the 2209A manual, will lead to an input timeout error (I92) on the MVP. The MVP cannot allow one partition to wait for an input strobe (8607) for a long time, as this would be unfair to other users. The MVP hardware does not permit the MVP to switch users once an 860X microcommand has begun, because data may be lost in the process. The solution is to wait for the tape drive controller to become ready (1020) before asking the board for input. Thus the change to the $GIO sequence is to insert a 1020 microcommand after a CBS (44xx) that causes tape motion and before the single character input (8607) that follows the tape motion commands.

As mentioned in the 2209A manual, it is not necessary to keep the tape controller board enabled throughout an entire tape operation. The example of a look ahead read is given. In the example, the $IF ON statement is an acceptable substitute for the wait for ready micro-command (1020).

```
10 #GIO READ/07B (4400 1020 8607 442A C220, A$) B$ ()
or
20 $GIO LOOK AHEAD READ /07B (4400, A$)
.
.
.
30 $IF ON /07B, 500
.
.
.
500 $GIO READ CONTROLLER BUFFER /07B (1020 8607 442A C220, A$)
```

In the previous example, $IF ON and the 1020 microcommand in line 500 are redundant.

Another important MVP change is the increased importance of Master Reset (459C). The reset key on the 2236D console WILL NOT reset the tape drive controller. If a reset from the console happens to occur in the middle of the execution of a tape drive $GIO sequence, the tape drive controller will be left in an unpredictable state. In such cases, it is important that tape drive controller be reset by sending a CBS of HEX (9C) without waiting for ready (459C).

The Status $GIO sequence is currently documented as allowable at any time (CBS of 88 without waiting for ready). Experience has shown that reading controller status during tape operations sometimes interferes with proper controller operation. The status sequence should be used to read tape drive status when the tape is not in motion (448B rather than 458B). $IF ON or the $GIO micocommand 1010 should be used to test for "tape operation complete".

On the VP and MVP, the $GIO sequence 1300 A000 is a faster multi-character output than the A200 in the present tape drive manual.

To summarize, the new recommended VP/MVP $GIO sequence for the 2209A tape drive are listed below:

```
Backspace file       $GIO BSF /07B (4405 1020 8607, A$)
Backspace record     $GIO BSR /07B (4404 1020 8607, A$)
Forwardspace file    $GIO FSF /07B (4402 1020 8607, A$)
Forwardspace record  $GIO FSF /07B (4408 1020 8607, A$)
Read                 $GIO READ /07B (4404 1020 8607 442A C220, A$) B$()
Rewind               $GIO REWIND /07B (4446 1020 8607, A$)
Write EOF            $GIO WEOF /07B (4403 1020 8607, A$)
Write Gap            $GIO WGAP /07B (4407 1020 8607, A$)
Write                $GIO WRITE /07B (4429 1300 A000 4401 1020 8607, A$) B$()
Look Ahead Read      $GIO LAR /07B (4400, A$)
(Subset of Read)
Finish Read          $GIO FR /07B (1020 8607 442A C220, A$) B$ ()
(Subset of Read)
Buffer Write         $GIO BW /07B (4429 1300 A000 4401, A$) B$ ()
(Subset of Write)
Finish Write         $GIO FW /07B (1020 8607, B$)
(Subset of Write)
Master Reset         $GIO RESET /07B (459C, B$)
Status               $GIO STATUS /07B (448B, 1020 8706, B$)
```

NOTES:

SECTION 5
SYSTEM-LEVEL THEORY OF OPERATION

5.1 INTRODUCTION

Overall operation of the 2200MVP is handled collectively by hardware, firmware, and software; however, the key to understanding how each major element of the system interacts with others comes by first understanding the method of memory control used in the Central Processor. This discussion will therefore commence in that general area.

5.2 MEMORY RESOURCES IN THE 2200MVP

There are two random-access memory units in the 2200MVP--Control Memory and User Memory.

Microcode for the Operating System is contained in (loaded into) Control Memory. The Operating System is a software package dedicated to central processor time management, system memory management, and I/O operations management. Control Memory comprises twenty-thousand 24-bit words, and that microcode is not accessible to users.

Physically separate from Control Memory is the RAM space allocated for User Memory (also referred to as "Data Memory" in other sections of this manual)--for storage of user programs, user data, and other information needed for correct user program execution. User Memory is divided into areas known as "banks". In the 2200MVP, a maximum of four banks are possible. A system containing from 16 to 64 kilobytes of User Memory uses only bank #1. In that first bank, memory may be added in 16K increments up to the 64K maximum. Memory in banks 2 and 3 may be added only in 32K increments. User memory in bank #4 may be added only in the full 64-Kilobyte size.

5.3 MULTI-USER MEMORY MANAGEMENT

In a multiple-user system such as the 2200MVP, system resources must be shared. The simplest technique of sharing user memory space is called "partitioning".

Normally, the word "partition" means "a dividing wall". However, in the computer industry, the word has come to mean the space enclosed by the wall, rather than the wall itself. Henceforth, when discussing partitioned memory management, the "partition" is a block of memory space with specified address boundaries; it is not a boundary itself. The 2200MVP is configured such that each user is allocated one or more blocks (partitions) of User RAM which belong exclusively to him.

5.4 PARTITIONING 2200MVP USER MEMORY

5.4.1 MASTER INITIALIZATION -- A PREREQUISITE FOR PARTITIONING

During Master Initialization, before user partitions are generated and allocated for system users, a "system-use" block--comprising the first 3K in Bank #1 of User (Data) Memory--is established for Operating System housekeeping. (For this preliminary allocation, the Operating System might be loosely thought of as another "user" of User RAM space, requiring its own partition.)

5.4.2 GENERATING THE PARTITIONS

The number of partitions to be created and the amount of User Memory to be allocated to each partition are specified by the user in a process called "partition generation". This process also involves specifying certain attributes for each partition and supplying the addresses of peripheral devices connected to the system.

Once the Operating System has been loaded into Control Memory (thus completing Master Initialization), the special utility program "@GENPART" is loaded and executed at terminal #1. This program leads the system operator through the necessary steps for "partition generation". A series of display prompts appear at terminal #1 which require the user operating that terminal to supply information pertinent to each partition and each shared peripheral device.

A "system configuration" is created by the @GENPART utility. Once created, a system configuration can be saved on disk for later recall. For this reason, a system configuration need be defined only once. A variety of system configurations can be created for different processing requirements; the operator can then select an appropriate configuration, as needed.

When the user has provided all of the information requested by @GENPART, or when the desired saved configuration is selected from the @GENPART display, the BASIC-2 statement $INIT must be executed. In the case of the Wang version of @GENPART, execution of $INIT is accomplished by keying SF 15. $INIT directs the Operating System to allocate resources as prescribed in @GENPART, in order to create the desired system configuration. Note that the $INIT statement alone (customized configuration) may be used instead of the Wang @GENPART program. In either case, it is the $INIT statement which ultimately causes configuration to be carried out.

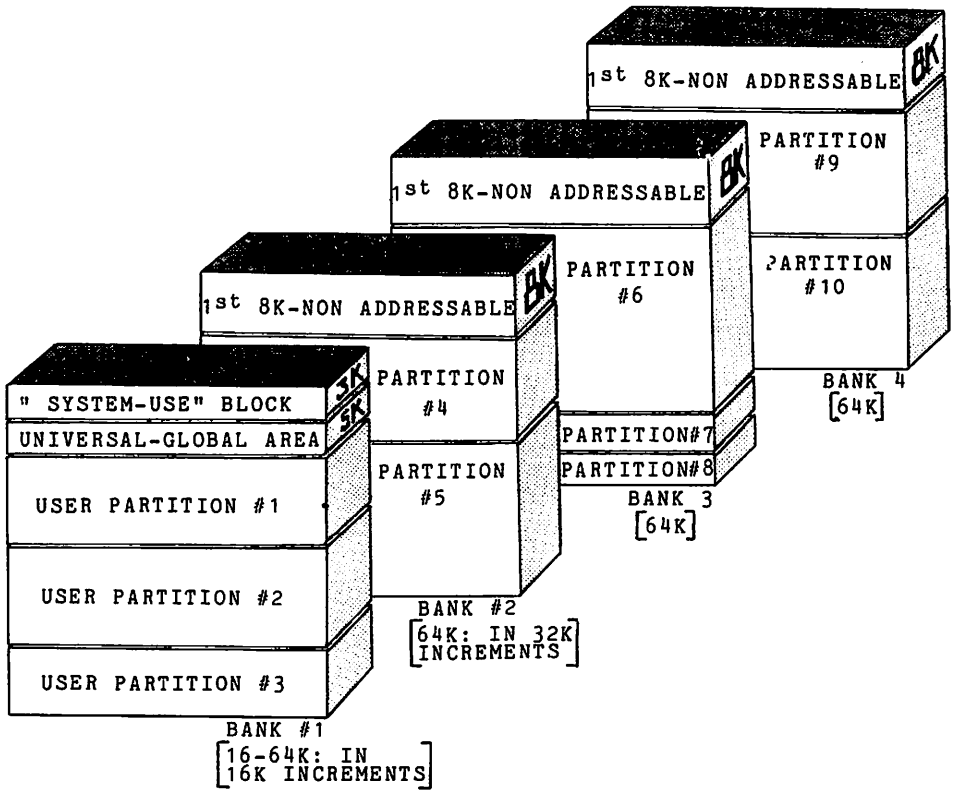
Once partition generation (partition allocation) has been implemented, each partition can be handled much like the entire user memory space of a single-user 2200 System: program text can be entered by a user, starting near the low end of his allocated partition, and his text entry progresses with ascending User Memory addresses; variable data for that program can be entered starting at the end (highest address) of his partition, and entry of that data progresses with descending User Memory addresses. This information will be illustrated in a partition-scheme diagram which appears in subsequent text of this section.

The MVP Operating System and CPU hardware will support a maximum of 16 partitions and 8 system users. All 16 partitions may be allocated to a single user, or multiple-parititon configurations may be created for each user. The 16 partitions (maximum configuration) may reside entirely within a single bank, or may be split up between all four banks (as could be the case for a 256K MVP). One restriction, in regards to this latter statement, is that each partition must be defined wholly within the confines of a bank; that is, no user partition is allowed to extend from one bank to the next.

NOTE:

The first 8K of banks 2, 3, and 4 are non-addressable, due to certain constraints of the MVP Operating System; this means that prior to partition generation time, there is only 56K (maximum loading) left for partitioning in each of those banks. A 256-Kilobyte MVP therefore provides an actual total of 229 Kilobytes for partitioning of User Memory. (61K in bank #1, plus 56K each for banks 2, 3, & 4)

FIGURE 5-1 2200MVP USER MEMORY



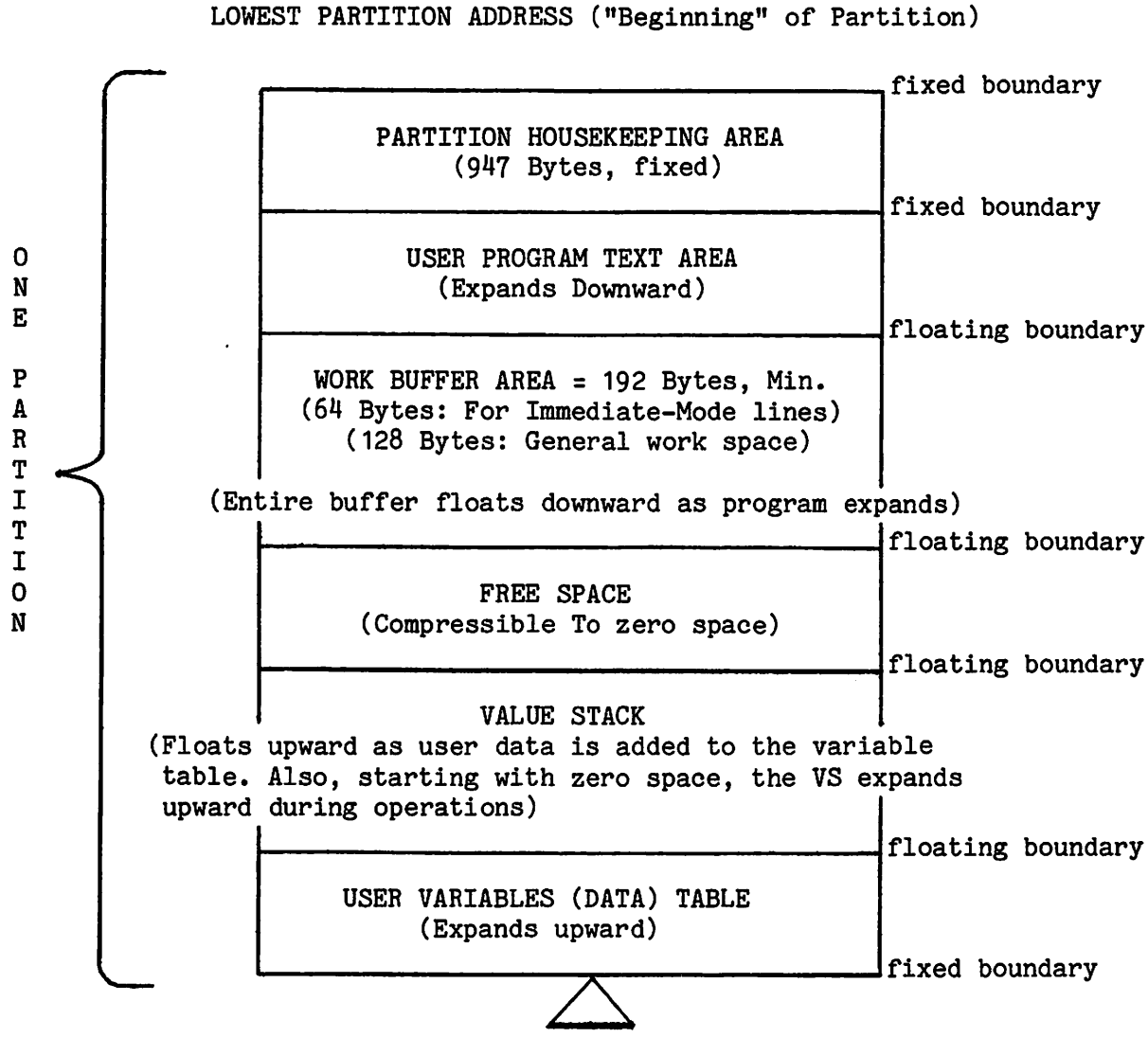
5.4.3 PARTITION SIZE & INTERNAL ALLOCATIONS

Partition sizes are specified in 256-byte (1/4K) increments. The minimum size that may be specified for any user partition is 1.25K. The guideline for maximum partition size is, as explained previously, that each partition must be defined wholly within the confines of a bank; no user partition is allowed to extend from one bank to the next.

The first 947 bytes of each partition is used by the Operating System for the operational Housekeeping" requirements of that partition (this is not to be confused with the "system-use" block in bank #1). Within each partition, there is also a User Program Text area, a Work Buffer, a Free Space area, a Value Stack, and a User Data Space (further explanation follows). Realize that neither the 947-byte housekeeping space, nor the Work Buffer, nor the Value Stack in each partition is addressable by the user; instead, values are stored in and retrieved from those blocks by the Operating System, according to the the conditions of execution existing in that partition at any given moment.

FIGURE 5-2

INTERNAL PARTITION ALLOCATIONS



The Value Stack is not of fixed size; it expands and contracts in size during the course of program execution, and its size is zero prior to program execution. Typically, the Value Stack serves as a storage space for transient operands during the evaluation of mathematical expressions; subroutine return address information is also stored here, as required by the user's program.

The Work Buffer "floats" at the end of the Program Text area in memory. It is used to temporarily store information transferred into memory from the keyboard's input buffer, as well as for temporary storage of data for certain system functions such as LIST DC, MOVE and COPY. Immediate Mode lines and

system commands transferred to the Work Buffer are immediately executed and then cleared; numbered program lines are moved from the Work Buffer area to the Program Text area so that they will be threaded into the user's program.

The Work Buffer can become as large as necessary (subject to available space) to contain an entered line. In every case, however, the system reserves a fixed minimum of 192 bytes for the Work Buffer.

When the addition of a new program line or variable threatens to overlap into the minimum buffer area, a memory overflow error is signaled, and the program line or variable is not stored.

The actual amount of free space that exists in a partition at any given moment may be calculated by the two BASIC functions SPACE and END. Before computing this free space, the system automatically subtracts 192 bytes from the available space (for the minimum Work Buffer area). Thus, if END and SPACE return free space values of zero, there remains a minimum of 192 bytes still available for the Work Buffer.

It is important to recognize that a situation may arise in which initially, there is sufficient free space to enter a program, but not enough free space to execute the program; this occurs when execution of a user's program causes the the Value Stack to expand beyond its allowed free-space limitations. The "SPACE" function can be used to determine just how much free space actually is available. Free space must be checked at the point during program execution where the Value Stack attains its maximum size. Typically, this condition occurs when the program executes the innermost loop in series of nested loops. SPACE can be executed in that innermost loop to determine how much free space is available at that point.

The SPACE function returns, to the workstation screen, the amount of memory not currently occupied by program text or data, minus the amount occupied by the Value Stack. This value represents the actual amount of free space in memory at any point during program execution.

The END function does not subtract the space taken up by the Value Stack.

The Meaning of "Negative" Free Space:

Although the system ensures that a minimum of 192 bytes always remain unoccupied by program text or variables in memory, it does permit the Value Stack to utilize a portion of this minimum buffer area. Up to 128 bytes of the 192-byte minimum Work Buffer can be used by the Value Stack. This fact implies that a program can be run even when memory is legally "full," since additions to the Value Stack during execution can overlap into the reserved Work Buffer area. Note that in this case the SPACE function would return a negative free space value. To understand why this is so, consider the following:

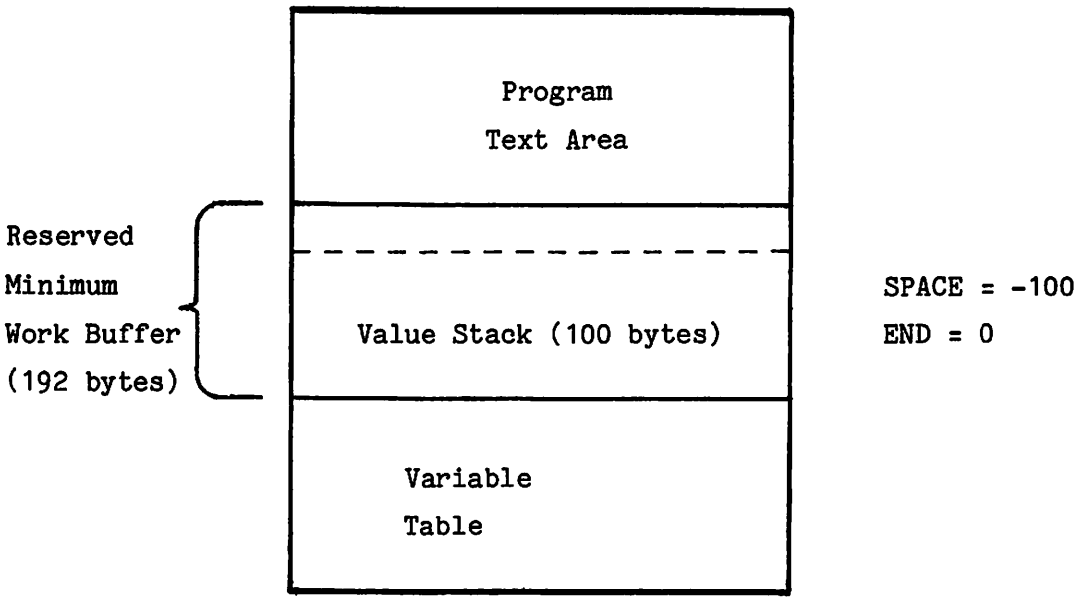


FIGURE 5-3
"Negative" Free Space

When memory is so fully packed that the Value Stack must occupy part of the minimum buffer area, size of the Value Stack is subtracted from zero by SPACE, yielding a negative free space figure. Thus, a free space value of -100, returned by SPACE, indicates that memory is legally "full"; however, 100 bytes of the reserved minimum buffer have been used by the Value Stack. Since a maximum of 128 bytes of the minimum buffer area can be used by the Value Stack, SPACE cannot return a value less than -128. When the Value Stack requires more than 128 bytes of the buffer, a memory overflow error is signaled.

5.5 THE SERVICING OF PARTITIONS

5.5.1 TIME-SLICE PROCESSING

The MVP CPU services each partition (max.= 16) in a repetitive, ordered sequence. Each partition is given a standard 30 ms. "time slice", during which exclusive use of the CPU is granted. A limited number of program or immediate-mode operations can be executed during this interval. For this purpose, the CPU has a 30-millisecond timer which is set at the beginning of each timeslice; this clock is checked periodically for expiration of the 30-ms limit. For reasons which will be explained in subsequent text of this section, note that time slices are not always allowed to last the full 30 ms.

When a partition's time slice ends, the Operating System saves (stores) all current status conditions for that partition. The Operating System then proceeds to load the status of the next partition into the CPU and begins a new 30-ms time slice. The exact moment when execution is halted in a partition is called the "breakpoint" of the time slice. The programmer cannot predict in advance when a breakpoint will take place, but the occurrence of breakpoints is of little or no concern to him. Further, since the ordered time slice arrangement is repeated at high speed, all user programs appear to operate simultaneously.

Whenever a partition is given a new time slice, conditions that existed at the end of that partition's previous time slice will be restored, and processing for that application resumes for the duration of the new time slice.

5.5.2 BREAKPOINTING

As previously mentioned, a time slice does not always last exactly 30 milliseconds. Unlike many operating systems, the MVP Operating System will cause breakpoints whenever it is convenient or advantageous, rather than only allowing breakpoints to occur upon expiration of the the CPU time-slice clock. Specifically, under the direction of the Operating System, a breakpoint may occur if a peripheral device being addressed is busy, or if a peripheral device being addressed is being "hogged*" by another partition; either condition is called an "I/O breakpoint".

---

* "Hogging" of system peripherals will be explained in paragraph 5.11.

For instance, if the partition that has the current time slice attempts a disk access, and if the disk is temporarily being "hogged" (used exclusively) by another partition, the hogging condition is quickly detected and a breakpoint occurs in the current partition's time slice.

The term "I/O breakpoint" should not be confused with "program breakpoint". Program breakpoints are conditional, scheduled halts in a user's program; they are a means, for instance, of monitoring an I/O port for pending data entry requests. Program breakpoints are written into the user's program by the user.

I/O breakpoints differ from program breakpoints in that the partition interrupted by an I/O breakpoint is specifically marked "waiting for I/O" by the Operating System. When that partition is given another time slice, the Operating System takes only microseconds to decide whether I/O processing may proceed or whether the partition is still waiting for the I/O device and must therefore be bypassed. The Operating System temporarily bypasses that partition as effectively as if it had been entirely removed from the system during the I/O waiting period.

The CPU is much faster than any of its peripherals, and for this reason, breakpointing during I/O allows the MVP to perform work with other partitions while the I/O operation is still being carried out. For example, when a program uses KEYIN to receive data from a keyboard, the CPU can give time slices to other partitions between operator keystrokes. In a similar manner, several partitions can be serviced by the CPU during a carriage return on a 2221W printer.

5.6 ASSIGNMENT, ATTACHMENT, and FOREGROUND/BACKGROUND PROCESSING

5.6.1 ASSIGNMENT

Although system resources must be shared in the 2200MVP, each user is given the impression of having his own personal system--his own terminal, his own memory, his own peripherals. As previously explained, the exact configuration of each user's "personal system" is specified by an operator at partition generation time. Partitions and terminals configured (by the Operating System) into one such "personal" system are said to be in a state of "assignment"; that is, they are assigned to each other as integral parts of an independently-functioning personal computer system.

Assignment alone is only a prerequisite for the actual operation of each "personal" system. In order to use any facility of the system, attachment is required.

5.6.2 ATTACHMENT

"Attachment" is a state that exists when the Operating System establishes an active bidirectional communications link between a partition and a terminal that already have previous assignment to one another. In effect, a partition, during attachment, is moved into the "foreground" by the Operating System; subsequent interaction between operator and system are thus allowed. Unless attachment occurs, a user has no access to the MVP central processor. Without attachment, the user terminal is dumb, having no program mode, no immediate mode.

At any given time, only one attachment is possible in each user's "personal" system configuration. Attachment with the lowest-numbered assigned partition occurs automatically on completion of @GENPART. (Ref: $INIT statement in the VP/MVP Language Reference Manual, WL#700-4080).

To illustrate the states of assignment and attachment, consider the following:

> Suppose that a program (arbitrarily called "program A") requires frequent operator interactions; another program, "B", belonging to the same user, requires only occasional interactions. The first requirement is that of assignment:
>
> > The two partitions (one with program "A", the other with program "B") and the user's terminal must have been previously assigned to each other by the Operating System, that they might function as an integral unit, a "personal system".
>
> So that program "A", the priority real-time program, can function on an interactive basis with the user terminal, the next requirement is that of attachment:

The Operating System moves the partition holding program "A" into the foreground. By this action, the Operating System attaches the user terminal and the partition to one another. For the duration of each subsequent time slice given to the foreground (attached) partition, both program and user can communicate with one another, and both have access to the CPU (program mode, immediate mode). Also by time-slice processing, program "B" runs "simultaneously" in the background, communicating with the CPU, communicating with certain peripherals. However, since this partition is running in the background, it is unable, for the moment, to interact with its assigned terminal.

When a background partition (program) attempts to communicate with its assigned terminal, and if that terminal is currently in a state of attachment with another assigned partition, execution of the background program is suspended (execution "hangs") until the requested terminal is released (detached) from the foreground partition and is then placed in a new state of attachment with the requesting partition. The formerly-attached partition is simultaneously moved into a background run-state by the Operating System.

Note that some background jobs may have no requirements for access to a terminal other than periodic displays of current job status. To avoid having such jobs "hang" while awaiting availability of the terminal, the $IF ON statement can be used to determine whether or not the terminal is currently attached (available) to the requesting partition; that is, $IF ON reveals whether or not the requesting partition is presently in the foreground run-state. If $IF ON does reveal that the terminal is in a state of attachment with the requesting partition, the status information is displayed; if not, the program branches to perform further processing before testing for availability of the terminal again.

5.7 "RELEASING" A TERMINAL:

"Release" of a terminal from a state of attachment is accomplished by executing the BASIC statement $RELEASE TERM in either the program mode or the immediate mode. When a terminal has been released (detached) from a foreground partition, the assignment that existed between the terminal and the partition is still recognized and maintained by the Operating System.

Further, when a $RELEASE TERM is executed, the foreground partition is moved immediately to the background by the Operating System. Simultaneously, the Operating System establishes a new state of attachment between the terminal and the lowest-numbered waiting (suspended, assigned) background partition. Of course, each new partition selected for attachment is considered to be in the foreground for the duration of that selection. Note that the term "background" implies only assignment; "foreground" implies both assignment and attachment.

All waiting background partitions may have a need for access to the terminal within their assignment; however, each of the assigned background partitions (programs) is sequentially given access to the terminal (i.e., is brought into the foreground for attachment) only when:

1) The program operating in the foreground partition executes a $RELEASE TERM statement; this means that the terminal is released, in the program mode, to the next-highest-numbered waiting partition. (Special case: If the $RELEASE TERM statement is executed in the highest-numbered assigned partition, the terminal is given to the lowest-numbered waiting partition in the assignment.)

OR When:

2) The user executes a $RELEASE TERM statement in the immediate mode; the terminal is released to the next-highest-numbered waiting partition. (Due to the fact that the processing order of partitions is repeated by the CPU, if the $RELEASE TERM statement is executed when the highest-numbered partition is in the foreground (attached), the terminal is given to the lowest-numbered waiting background partition in the assignment.)

If there are no assigned partitions actually waiting for a terminal after it been released, it is possible for the operator at that terminal to request the Operating System to re-establish a state of attachment between his terminal and one of the partitions assigned in his "personal" system.

This is accomplished by keying either RESET or HALT on the terminal. On that signal, the Operating System moves the user's lowest-numbered assigned background partition to the foreground, HALTs or RESETs any program operating in that partition, and then establishes a state of attachment between the terminal and the partition.

NOTE:

> In order to allow re-attachment, and in order to prevent the halting or resetting of an active background program, it is a good practice to generate a small control or "dummy" partition as the lowest-numbered assigned partition.

Optionally, the user himself may direct the swapping of terminal/partition attachments by executing a modified form of the $RELEASE TERM statement ($RELEASE TERM TO) in either the program mode or the immediate mode. A partition is named in the TO parameter, and that partition must, of course, be a partition that already shares assignment with his terminal. When a $RELEASE TERM TO statement is executed, the terminal is placed in attachment with the specified partition, even if that partition has not attempted to communicate with the terminal, and even if one or more other assigned partitions have attempted to communicate with the terminal. $RELEASE TERM TO does not halt the execution of programs running in either the current foreground partition or the target background partition specified in the TO parameter.

5.8 "RELEASING" A PARTITION:

Release of a parititon from a state of attachment is accomplished by executing the BASIC statement $RELEASE PART in either the program mode or the immediate mode. A partition may also be considered "released" if, at partition generation time, an operator specifies terminal #0 (a non-existent terminal, sometimes called the "null" terminal) for any terminal/partition assignment in the system. Another term used in place of "released partition" is "available partition". In any case, the flag which signifies that a partition is released (i.e., available) is the terminal #0 assignment. A released partition does not belong to any user's "personal

system"; it has no terminal associated with it; it has no terminal assignment. Note that if a program is running in a released partition, execution of that program will "hang" if any communications are attempted with a terminal.

The $RELEASE PART statement allows a partition to become available to any terminal connected to the system.

Consider the following:

1) If a terminal is in a state of attachment with some partition, and if that partition does not meet requirements for some new application (due to insufficient partition size, for instance), the operator may elect to use an "available" partition more suited to his needs. The characteristics of available partitions may be examined by executing a $PSTAT statement. When the available partition is found having characteristics most suited to the operator's needs, the user may then execute a $RELEASE TERM TO statement to the available partition; the newly-acquired partition will then be given a new assignment with the requesting terminal, and will be placed in a state of attachment with that terminal. Thus, the new partition becomes a new addition to the user's "personal" system.

2) An operator at a non-assigned terminal may also request assignment and attachment to a released (available) partition by keying RESET or HALT.

$RELEASE PART causes a present states of attachment and assignment between a terminal and a partition to be broken off. The terminal formerly belonging to that assignment can optionally be re-directed to a new partition for assignment and attachment (if a new assignment is specified in parameters of the $RELEASE PART statement). This carries the implication that, in addition to making a partition available, $RELEASE PART also performs a $RELEASE TERM TO for the terminal. If a new partition assignment is not specified for the terminal in the parameters of $RELEASE PART, that terminal will either be attached to a waiting partition already within the assignment (if there is one waiting), or the terminal will have no further

assignment or attachment with any partition. In the latter case, the terminal becomes non-assigned, having no immediate mode, no means of executing programs, no access to system peripherals; it would no longer be part of the active MVP system.

Note that $RELEASE PART does not clear a partition, nor does it terminate a program running in that partition.

5.9 "GLOBAL" PARTITIONS:

Although partitions function independently, there are situations in which it is highly expedient for two or more partitions to cooperate with one another, to share common information, common programs. This sharing eliminates needless duplication of applications software and data, thus allowing more efficient use of available User Memory space.

Partitions can therefore be "global"; that is, each partition so designated contains programs and/or data which become conditionally shareable. A foreground or background program that is running in a partition in one bank can access any global partition (i.e., global routine and/or global data) residing in that same bank. Additionally, a user terminal that is in a state of attachment with a partition in that same bank can access those global routines and/or data while in the immediate mode.

5.10 "UNIVERSAL GLOBAL" PARTITIONS:

The first 5K of User Memory in bank #1 (immediately following the System-Use Block) constitutes a special section of User Memory known as the "universal-global" area. (See Figure 5-1.) Partitions defined within this area are correspondingly called "universal-global partitions". A universal-global partition may be accessed by a program running in any foreground or background partition. Also, similar to standard global access, user terminals in a state of attachment are allowed access to universal-global routines and/or data while in the immediate mode. To summarize, a universal-global partition can be used to store programs and data that can be shared by all system users.

Note that the entire 5K universal-global area need not be used exclusively for universal-global partitions; the only restriction is that, for a partition to be universally global, it must reside entirely within the 5K universal-global address block in bank #1. When not required for universal-global purposes, that same 5K in bank #1 can be treated as all other partitionable memory.

5.11 USER PROGRAM EXECUTION:

5.11.1 GENERAL

The term "job flow" refers to the path of execution followed by a job from beginning to end. In the 2200MVP, job flow may be confined within a single partition, or it may extend across several partitions via global subroutine calls. The term "job" is preferred to "program" here, because the term "program" is too closely associated with the contents of a single partition. A job consists of one or more program routines; each line of each routine in the job contains one or more program statements. In the normal execution of an individual routine, each statement is executed from left to right, from lowest line number to highest.

5.11.2 SUBROUTINES:

The Operating System tracks execution of a job by using a "text pointer". The text pointer always points to the statement that is to be executed next in a particular job flow; the text pointer provides a "thread" leading from the statement currently being executed to the statement that is about to be executed.

If job execution is confined within a single partition, the text pointer contains all information required by the Operating System for the execution of a user's program. However, to execute global subroutines, the Operating System requires additional information that reveals which partition contains the currently-executing program text.

When a global subroutine call is made, the global text is executed as if that text were appended to the calling text within the originating partition. The "job" may therefore be thought of as the combination of all nonglobal and global program text, considered as a integral unit.

The "originating partition" is the partition in which the job is initiated; further, it is the partition that holds all status information pertinent to the execution (flow) of that job, even if that job extends across several partitions. Each job has only one "originating partition".

The "calling partition" is simply a partition making the current global/universal-global subroutine or data call in a multi-partition job.

When a user program issues a non-global, global, or universal-global subroutine call (or requires global/universal-global variables), the status and return-address information for each successive subroutine level is stored in the originating partition sequentially. If a time slice expires while execution is taking place in an originating partition, or if the time slice is terminated by the occurence of a breakpoint, or if the time slice ends while execution is taking place in a called global/universal-global routine, the conditions of execution that exist at the moment the time-slice ends are also stored in the originating partition.

In order to track all of the various conditions that arise during subroutine calls, each partition has two internal "stacks" and a "pointer table"; users are not allowed access to these housekeeping elements. The CPU and the Operating System service each partition, and in the process, each pointer and stack element is monitored, used, and updated. Note that the text pointer for each job is maintained within the originating partition's pointer table.

5.11.3 THE TEXT POINTER, POINTER TABLE, & INTERNAL STACKS:

Typically, when a subroutine call is issued (for instance, by a GOSUB' statement), the number of the statement following the GOSUB' becomes the current value of the "text pointer". Simultaneously, the same number is saved on top of the Value Stack, one of the internal stacks previously mentioned in this discussion.

NOTE:

> The Value Stack functions as a "push-down, pop-up" storage element. (The last, most recent entry in the value stack will be the first to be recalled at any given time by the Operating System.) The Value Stack can also be thought of as a "last-in, first-out" or "LIFO" storage element.

The Operating System searches the program for a DEFFN' that corresponds to the GOSUB' just issued. The statement number at which the DEFFN' is found becomes the a current value in the text pointer. The Operating System instantaneously passes execution to that point in the program.

The number in the value stack is unchanged; it is still the statement number following the GOSUB'. When a RETURN statement is executed in the subroutine, the Operating System retrieves the "old" text pointer entry from the top of the value stack. That entry is placed in the text pointer (in the pointer table), thus replacing the DEFFN' statement number, and then the Operating System passes execution back to the statement which immediately follows the GOSUB statement.

Pointer Table Format:

The following illustrates basic Pointer Table format:

Text Pointer	
Text Partition #	
Data Partition #	
Global Partition #	
Current Partition #	
Terminal #	

Basically, each text pointer consists of a line number and a statement number. For example, consider the following line of program text:

```
10  A = 100:  PRINT A
```

In line #10, when the statement "A = 100" is executed, the text pointer is automatically incremented to point to the next statement in that line, "PRINT A". Thus, during execution of the statement "A = 100," the text pointer would have the value "10,2", indicating that the next statement to be executed is the second statement in line 10.

Initially, all items in the Pointer table refer to the current partition. For example, immediately following Master Initialization, a system configuration could be established such that Partition #2 (in a state of assignment with Terminal #4 for this arbitrary example) would have the following values in its pointer table.

Text Pointer	0,0
Text Partition #	2
Data Partition #	2
Global Partition #	2
Originating Partition #	2
Terminal #	4

The last two items in the table--Originating Partition# and Terminal#--are constants set during Master Initialization. These values do not change unless the system is reconfigured; other items in the table can be modified frequently during job execution. The meanings and uses of each item in the pointer table follow:

- The Text Pointer - is updated by the Operating System, each time a statement is executed, to point to the next sequential statement. Further, it is modified by any branch statement (GOSUB, GOTO, GOSUB', etc.), in order to point to the branched-to statement.

- The Text Partition # - is the number of the partition to which the text pointer applies (i.e., it is the number of the partition containing the currently-executing text). It is modified by a GOSUB' statement whenever a branch is made to a DEFFN' in a global partition. In this case, GOSUB' sets the Text Partition # equal to the Global Partition #.

- The DATA Partition # - is the number of the partition containing DATA statements referenced by READ. The DATA Partiton # can be modified by a RESTORE statement, which always sets that number equal to the current Text Partition #.

- The Global Partition # - is the number of the currently- selected global partition. It is modified by a SELECT @ PART statement. It is the partition searched by GOSUB' for a corresponding DEFFN' when the DEFFN' cannot be found in the Text Partition. It is also the partition used for all global variable references.

- The Originating Partition # - is the number of the partition in which execution of the job originates and the Pointer Table is stored. The Originating Partition # is a constant for each partition. It is used for all local variable references, for LOAD operations, and for all system commands issued from the user terminal. The Originating Partition # is returned by the #PART function.

- The Terminal # - is the number of the terminal that is in a state of assignment with the originating partition. Like the Originating Partition #, it is set at configuration time and generally is not modified, except by reconfiguring the system. (Terminal # can be altered upon execution of a $RELEASE PART statement.) Terminal # is used for all CRT, keyboard, and local printer I/O operations performed during job execution; this includes CO, CI, PRINT, LIST, INPUT, LINPUT, KEYIN, etc. For any partition, the Terminal # is returned by the #TERM function.

5.12 ALLOCATION & HANDLING OF PERIPHERALS

5.12.1 GENERAL

The mental image of multiple partitions and terminals functioning as completely independent "personal systems" may be clouded somewhat by the problem of competition (between partitions) for shared peripheral devices ("system peripherals"). This situation is familiar to programmers accustomed to working with single-user Wang 2200 systems that share one or more disk drives via disk multiplexers. In such systems, it is sometimes necessary for one CPU to request exclusive control of a disk (i.e., to "hog" the disk) while a file update is conducted.

With the 2200MVP, it may be necessary for a partition to exclusively control a printer. For example, if, during a report printout, a printer were not exclusively available to one partition, that partition's print lines might become unintelligibly mixed with those of another partition's, if both were allowed access to one system printer at the same time. To solve this problem, the concept of disk hog mode has, in the MVP, been extended to all shared I/O devices ("system peripherals").

To state the situation more specifically: prior to configuration of the system through $INIT, and with the exception of user terminals and local printers, peripherals connected directly to 2200 I/O controllers are available to all partitions i.e., such peripherals are "sharable". This implies, further, that printers connected to terminals would not be considered "shareable". A conflict arises when more than one user partition simultaneously attempts access to a shareable device.

In order to avoid such situations, the MVP Operating System enables a partition, under program control, to request exclusive use of a peripheral with a $OPEN statement; the address of that peripheral must be specified in that statement. Once "open", the device remains hogged by the requesting partition until either a $CLOSE or an END statement is executed or if a CLEAR, RESET, or LOAD RUN command is initiated. Thus, if a disk is "hogged" by the $OPEN statement, only the user who executed that statement may read or write disk files until the device is released by one of the above prescribed methods.

With the exception of terminals and local printers connected to them, all peripherals connected to the system must be specified in the Master Device Table at partition generation time. Using the Master Device Table, a device can be placed in exclusive assignment with a specific partition until a new system configuration is generated.

Basically, peripheral assignments are established at partition generation time by the entry of a number--the number of the partition which is to have control of a particular device--in the "Master Device Table". Such entries are carried out indirectly by the Operating System during the execution of @GENPART. If any partition attempts access to a peripheral device that has not been allocated to it during @GENPART (i.e., use of that peripheral device was not specified in the Master Device Table), an error is signaled to the user.

Console device addresses (i.e., HEX 005 (CRT), 001 (Keyboard), 204 (terminal printers)) are not specified in the Master Device Table; these are specified in partition device tables. Each partition, in fact, has its own partition ("local") device table that should not be confused with the Master Device Table; the partition device table specifies use of console devices in a user's "personal" system configuration. This means that for each new attachment between a terminal and a partition, a new set of specifications for use of local console I/O devices will take effect; that is to say, certain options pertinent to console I/O devices in each "personal" system may be specified in each partition's device table. This method involves use of the SELECT statement with its various options (Ref: 2200VP/MVP Language Manual; WL# 700-4080).

Basically, when the system is instructed to perform an I/O operation with an I/O statement or command, it must be provided with the device-address to be used for that operation. If the device-address is not directly specified in the instruction itself (several classes of I/O instructions do not permit the direct specification of device-addresses), it is obtained from one of the device tables.

DEVICE SELECTION -- DETAIL EXPLANATION

The MVP has four I/O devices designated as the Primary I/O Devices for the system The device addresses of Primary peripherals are built into the system so that whenever the system is Master Initialized, these device addresses are automatically selected for I/O operations. The Primary I/O Devices normally are:

INPUT Device:	Keyboard @ hex address 001 (Terminal #1)
OUTPUT Device:	CRT @ hex address 005 (Terminal #1)
DISK Device:	The Disk @ hex address 310)
PLOTTER Device:	The Primary Plotter (address 413)

Note that these are not the same as Console I/O Devices, which are pertinent only to each "personal" system, each partition/terminal assignment having its own "Console" devices.

When an input/output operation is executed, the appropriate device is selected in one of three ways.

1. DEFAULT (Primary Console Device) - If no device-address is specified or selected, the system automically provides the device-address which is most commonly used for that particular operation.

2. SELECT - The SELECT statement can be executed. It assigns device-addresses for specified I/O operations.

3. SPECIFICATIONS - The device-address can be supplied with the BASIC I/O statement or command.

If a system does not contain additional input/output devices, then device addresses need not be specified or selected in the BASIC commands and statements which perform input/output operations. If more peripherals are added to the system, however, device address specification or selection is required.

When Master Initialization occurs, the Primary Console Input address (001) is assigned to Console Input, INPUT, LINPUT, and KEYIN operations. The Primary Console Output address (005) is assigned to Console Output, PRINT, PRINTUSING, and LIST operations.

Similarly, disk operations reference the Primary Disk address (310), PLOT statements reference the Primary Plotter address (413), and tape statements reference the Primary Tape address (10A).

5.12.2 BACKGROUND PRINTING

As an additional feature of the MVP system, if a printer is connected to the rear apron of an "assigned" terminal (thus making the printer an assigned "local printer"), it is possible for a background program to send output to that printer while a foreground program simultaneously interacts with the keyboard and display of the attached terminal. The only requirement for background printing is that the terminal to which the local printer is connected must be in a state of assignment with both the foreground and the background partition. The simultaneous I/O required for this type of action is handled by the 2236MXD controller and the 2236D firmware (PROMs).

NOTES:

SECTION 6
DIAGNOSTICS

6.1 GENERAL INTRODUCTION

There are four classes of diagnostic tests available for the 2200MVP System: 1) - "BOOTSTRAP" (the resident diagnostic program in the 2200 MVP CPU hardware), 2) - the Microcode (hardware/firmware) Diagnostics, 3) - the BASIC-2 Language Diagnostic, and 4) - the 2200 Peripheral Diagnostics.

The Microcode (hardware/firmware) Diagnostics for the 2200MVP CPU are available on the 2200MVP Operating System diskette (WL# 701-2294, latest version).

The BASIC-2 Language Diagnostic for the 2200MVP is available on WL diskette #701-2261. This diagnostic can be run on more than one 2236D terminal; in fact, this diagnostic should be run concurrently on all system terminals.

The 2200 Peripheral Diagnostics for the 2200MVP is available on WL diskette #701-2180. Note that when running the 2200 Peripheral Diagnostics, only one terminal can be used. When using any printer diagnostic for a local printer, all SELECT PRINT 215 statements in the program must be changed to SELECT PRINT 204.

6.2 MICROCODE DIAGNOSTICS

The 2200MVP diagnostics are microcoded routines that test the hardware components of the system and attempt to pinpoint any malfunction.

Additionally, there is a resident diagnostic program in the 2200 MVP CPU hardware called "BOOTSTRAP", and it too is a microcoded diagnostic routine (Ref: Section 3, paragraphs 3.7., 3.8, & 3.9). BOOTSTRAP runs automatically, whenever the central processor is powered up.

6.2.1 LOADING SYSTEM FILES

Whenever the operator responds to certain visual BOOTSTRAP requests, a System File will be loaded from the system disk and the following additional tasks are performed (by BOOTSTRAP):

a) Check for disk "ready".

b) Verify whether or not the requested file exists on the platter mounted.

c) Load the file into Control and/or User Memory, depending on whether the tests to be run are microcode diagnostics, language diagnostics, or peripheral diagnostics.

d) Verify correct Control Memory instruction parity, Control Memory CRC, and Control Memory LRC.

e) Check User-Memory Parity.

f) BOOTSTRAP passes control of the CPU to the System File currently loaded in Control Memory.

NOTE

Beginning with BOOTSTRAP release 2.2, one enhancement concerning the loading of system files has been made available; that is, the name of the file to be loaded by BOOTSTRAP can be entered by the operator. File names have a maximum length of 4 characters, the first of which must be "@". The appropriate disk-address SF' key should be pressed after keying-in the file name.

There are four "System File" diagnostics: 'CPU', 'Control Memory', 'Data Memory' (the User Memory test), and 'Registers'; these are microcoded routines designed to test the system hardware.

6.2.1.1 BOOTSTRAP SPECIAL FUNCTION KEYS

There are three groups of function keys defined for use from the "KEY SF'?" message that occurs during BOOTSTRAP.

a) BASIC-2.

b) User Menu of Diagnostics.

c) Field Service Menu of Diagnostics.

If BASIC-2 is selected by the operator, access to either of the other two groups is not possible without reinitializing the central processor (via CPU power off/on, or $INIT).

If either the User Menu or Field Service Menu is selected, access to either of the other two groups is possible by keying RESET and then by selecting either another diagnostic menu or BASIC-2. (No reinitialization is necessary in this case.)

One of the above programs may be loaded into Control Memory by keying the appropriate special function key in response to the "KEY SF'?" message, as follows:

a) SF'00 loads BASIC-2 from the disk @ address 310 (HEX).
b) SF'01 loads BASIC-2 from the disk @ address B10 (HEX).
c) SF'02 loads BASIC-2 from the disk @ address 320 (HEX).
d) SF'03 loads BASIC-2 from the disk @ address B20 (HEX).
e) SF'04 loads BASIC-2 from the disk @ address 330 (HEX).
f) SF'05 loads BASIC-2 from the disk @ address B30 (HEX).
g) SF'08 loads BASIC-2 from the disk @ address 350 (HEX).
h) SF'09 loads BASIC-2 from the disk @ address B50 (HEX).
i) SF'10 loads BASIC-2 from the disk @ address 360 (HEX).
j) SF'11 loads BASIC-2 from the disk @ address B60 (HEX).
k) SF'12 loads BASIC-2 from the disk @ address 370 (HEX).
l SF'13 loads BASIC-2 from the disk @ address B70 (HEX).
m) SF'16 loads the User menu from the disk @ address 310 (HEX).
n) SF'17 loads the User menu from the disk @ address B10 (HEX).
o) SF'18 loads the User menu from the disk @ address 320 (HEX).
p) SF'19 loads the User menu from the disk @ address B20 (HEX).
q) SF'28 loads the Field Service Diagnostics menu from the disk @ address 310 (HEX).
r) SF'29 loads the Field Service Diagnostics menu from the disk @ address B10 (HEX).
s) SF'30 loads the Field Service Diagnostics menu from the disk @ address 320 (HEX).
t) SF'31 loads the Field Service Diagnostics menu from the disk @ address B20 (HEX).

BOOTSTRAP ignores all undefined function keys while waiting for a response to the "KEY SF'?" message. Should a function key be depressed that specifies an unused hex address (no device at that address), BOOTSTRAP will halt; BOOTSTRAP always waits for a ready condition from disk. In case the wrong SF key is pressed, keying RESET restores the "KEY SF'?" message to the display of terminal #1.

When either the User or Field Service diagnostics menu is selected, a CPU system-diagnostics menu is displayed. (Ref: Paragraph 6.2.5)

USER DIAGNOSTICS:

When the User diagnostics menu is selected, the operator may select:

a) SF'00 to load and run the CPU diagnostic.
b) SF'01 to load and run the Control Memory diagnostics.
c) SF'02 to load and run the Data Memory (User Memory) diagnostics.

In general, the User diagnostics comprise a chain of diagnostics; these are executed without operator intervention. The selected sequence repeats until RESET is keyed.

FIELD SERVICE DIAGNOSTICS

When the Field Service menu is selected, the operator can individually select:

a) SF'00 to load and run the CPU diagnostic.
b) SF'01 to load and run the Control Memory Addressing diagnostic.
c) SF'02 to load and run the Control Memory MAT C&S diagnostic.
d) SF'03 to load and run the Control Memory ROWPAT diagnostic.
e) SF'04 to load and run the Data Memory (User Memory) Addressing diagnostic.
f) SF'05 to load and run the Data Memory (User Memory) MAT C&S diagnostic.
g) SF'06 to load and run the Data Memory (User Memory) ROWPAT diagnostic.
h) SF'07 to load and run the Register diagnostic.
i) SF'08 to load and run the Auxiliary Registers diagnostic.
j) SF'09 to load and run the Stack Register diagnostic.

In general, Field Service diagnostics will execute only the specified diagnostic until RESET is keyed. The diagnostics used by the Field Service menu and the User menu differ by the inclusion of Register

tests in the Field Service Menu. The only additional difference is that the user-menu chain runs every diagnostic category. Refer to paragraph 6.2.2 for a brief description of each cpu hardware test category, paragraph 6.2.3 for brief descriptions of user diagnostics, and paragraph 6.2.4 for brief descriptions of Field Service diagnostics. Note that in order to select another diagnostic test, one of the three test menus must first be reselected. Therefore, after each test, key RESET, key the appropriate SF' key for selection of a menu, then select the desired test from the menu just selected.

Note that in the Field Service Diagnostics, special function key '15 is defined uniquely to allow chaining of Register Diagnostics. After selecting one of the Register diagnostics, keying RESET and then SF' 15 will cause all three register diagnostics to run sequentially.

6.2.2 MICROCODE DIAGNOSTICS DESCRIPTION

DIAGNOSTIC	FUNCTION
CPU	Test instruction set, including Extended and Read/Write instructions.
CONTROL MEMORY	Test Control Memory from end-of-program to end-of-memory for addressing, duplication of the 2200 Option 5 memory diagnostic, and a modified ROW PATTERN test.
DATA (USER) MEMORY	Test Data (User) Memory from start-of-memory to end-of-memory for addressing, duplication of the 2200 Option 5 memory diagnostic, and a modified ROW PATTERN test.
REGISTERS	Test registers F0-F7, CH, CL, PH, PL, SL, K, AUX 0-32, and STACK 0-96 (the SH register is not tested due to the ability of the hardware to change bit status).

6.2.3 USER DIAGNOSTICS

DIAGNOSTIC	CONFIGURATION	REPETITIONS
CPU	Loads and runs the CPU diagnostic only. Runs continuously.	3 passes per second
CONTROL MEMORY	Loads ADDRESSING, MATC&S and ROWPAT. Runs ADDRESSING for 5 loops, MATC&S for 5 loops, and ROWPAT for 1 loop, then repeats sequence.	3 minutes per pass
DATA (USER) MEMORY	Loads ADDRESSING, MATC&S and ROWPAT. Runs ADDRESSING for 5 loops, MATC&S for 5 loops, and ROWPAT for 1 loop; the entire sequence then repeats.	Size-dependent

6.2.4 FIELD SERVICE DIAGNOSTICS

DIAGNOSTIC	CONFIGURATION	APPROX. TIME PER LOOP
CPU	Loads and runs CPU diagnostic only. Runs continuously.	3 seconds per pass
CONTROL MEMORY	Loads ADDRESS, MATC&S, and ROWPAT. Runs only the selected diagnostic (continuously).	'ADDRESS'- 3 seconds per pass 'MAT C&S'- .5 seconds per pass for 16K 'ROWPAT'- 2.5 minutes per pass
DATA (USER) MEMORY	Loads ADDRESS, MATC&S and ROWPAT. Runs only the selected diagnostic continuously.	'ADDRESS' - .3 seconds per pass 'MAT C&S' - 2 seconds per pass 'ROWPAT' - Size-dependent
REGISTERS	Loads REGISTERS, AUXILIARY REGISTERS and STACK. Runs only the selected diagnostic (continuous-run).	'REGISTERS' - .07 seconds per pass 'AUXILIARY' - .5 seconds per pass 'STACK' - 1 second per pass

6.2.5 SPECIAL FUNCTION KEY DEFINITIONS FOR BOOTSTRAP MENUS

SF KEY:	FUNCTION/MENU LOADED:	SF KEY:	FUNCTION/MENU LOADED:
00	BASIC-2 (310)	15	
01	BASIC-2 (B10)	16	USER MENU (310)
02	BASIC-2 (320)	17	USER MENU (B10)
03	BASIC-2 (B20)	18	USER MENU (320)
04	BASIC-2 (330)	19	USER MENU (B20)
05	BASIC-2 (B30)	20	
		21	
		22	
		23	
06		24	
		25	
		26	
07		27	
08	BASIC-2 (350)	28	F.S. MENU (310)
09	BASIC-2 (B50)	29	F.S. MENU (B10)
10	BASIC-2 (360)	30	F.S. MENU (320)
11	BASIC-2 (B60)	31	F.S. MENU (B20)
12	BASIC-2 (370)		
13	BASIC-2 (B70)		
14			

PROGRAMS LOADABLE FROM DIAGNOSTIC MENUS

SF KEY	USER DIAGNOSTICS MENU	FIELD SERVICE DIAGNOSTICS MENU
00	CPU	CPU
01	CONTROL MEMORY	C.M. ADD.
02	DATA MEMORY	C.M. MATC&S
03	n/a	C.M. ROWPAT
04	n/a	D.M. ADD.
05	n/a	D.M. MATC&S
06	n/a	D.M. ROWPAT
07	n/a	REGISTER
08	n/a	AUX. REGISTERS
09	n/a	STACK
10	n/a	n/a
14		
15	n/a	REGISTERS Diag. (chained)
16		
	n/a	n/a
28		
29		
30		
31		

6.3 SYSTEM DIAGNOSTIC DISPLAYS

6.3.1 CPU DIAGNOSTIC

This diagnostic is designed to test the instruction set of the MVP Central Processor. The test sequence is as follows:

a) Test Immediate Register instructions.
b) Test Register instructions.
c) Test Extended Register instructions.
d) Test Branch instructions.
e) Test Immediate Register instructions with Read/Write.
f) Test Register instructions with Read/Write.
g) Test Mini Instructions with Read/Write.
h) Return to step a).

If RESET is keyed during this program, the KEY SF'? message should be displayed.

Normal Display:

```
     CPU DIAG PASS LLLL
IMMED REG XX
REG INSTR XX
X-REG INSTR XX
MASK BR XX              where:  LLLL = Number of completed loops
REG BR XX                         XX = Microinstruction currently
IMMED R/W XX                           being tested (in HEX).
REG R/W XX
AUX/STACK R/W XX
```

Should the system be unable to execute a particular instruction, the CRT cursor will stop at XX of the failing instruction. Should the title fail to appear, any of the following could be at fault: ORI, AC, SB, SR, B, BT, BF, BNE, BLER, or BNR.

MVP CENTRAL PROCESSOR INSTRUCTION SET

Instruction Code:	Instr. Tested:	Instr. Class:
00	ORI	
01	XORI	
02	ANDI	
03	A	IMMEDIATE
04	DACI	REGISTER
05	DSCI	
06	ACI	
07	MI	
08	OR	
09	XOR	
0A	AND	
0B	SC	REGISTER
0C	DAC	
0D	DSC	
0E	AC	
0F	M	
10	SHIFT	
12	ORX	
13	XORX	
14	ANDX	
15	SCX	EXTENDED
16	DACX	REGISTER
17	DSCX	
18	ACX	
19	MX	
1A	SHIFT X	
1B	BF/BT	MASK BRANCH
1C	BNE/BEQ	
1D	BNR/BER	
1E	BLR	REGISTER
1F	BLRX	BRANCH
20	BLER	
21	BLERX	
43	ORI(R/W)	
44	XORI(R/W)	
45	ANDI(R/W)	
46	AI(R/W)	IMMEDIATE
47	DACI(R/W)	R/W
48	DSCI(R/W)	
49	ACI(R/W)	
4A	MI(R/W)	

Instruction Code:	Instr. Tested:	Instr. Class:
4B	OR(R/W)	
4C	XOR(R/W)	
4D	AND(R/W)	
4E	SC(R/W)	
4F	DAC(R/W)	
50	DSC(R/W)	REGISTER
51	AC(R/W)	R/W
52	M??(R/W)	
53	SHIFT(R/W)	
54	LPI(R/W)	
55	SR(R/W)	
56	TAP,TPA,XPA(R/W)-00	
57	-01	
58	-02	
59	-03	
5A	-04	
5B	-05	
5C	-06	
5D	-07	
5E	-08	
5F	-09	
60	-0A	
61	-0B	
62	-0C	
63	-0D	
64	-0E	
65	-0F	AUXILIARY
66	-10	&
67	-11	STACK R/W
68	-12	
69	-13	
6A	-14	
6B	-15	
6C	-16	
6D	-17	
6E	-18	
6F	-19	
70	-1A	
71	-1B	
72	-1C	
73	-1D	
74	-1E	
75	-1F	
76	STACK (R/W)	

6.3.2 CONTROL MEMORY DIAGNOSTICS

6.3.2.1 ADDRESSING

This diagnostic is designed to read from MVP Control Memory location 0800 (HEX) to the last location in Control Memory and vice versa, searching for a memory location which may have been changed by writing into some other location. This is accomplished in the following manner:

a) Flood memory with Hex 5A's ($0101\ 1010_2$).
b) Starting at location 0800 (Hex) and searching forward to the end of Control Memory, read each location and check for the 5A pattern. If a location verifies "O.K." when checked, write an A5 (1010 0101) at that same location.
c) Starting at the end of Control Memory (this does not include BOOTSTRAP addresses) and searching backward to Control Memory location 0800 (Hex), read each location and check for the A5 pattern. If a location verifies "O.K." when checked, write a 5A (Hex) at that same location.

When RESET is keyed during this program, the KEY SF'? message should be displayed.

6.3.2.2 MAT C&S

This diagnostic is designed to test from the end of the diagnostic program to the end of Control Memory, and is accomplished as follows:

a) The length of a random pattern to be written into all Control Memory locations is determined; this length is from 1 to 256 8-bit random characters.
b) The random pattern is written into a section of Control Memory.
c) The last-written section of memory is read, and then the random pattern is written into the next section of memory.
d) Repeat step c) until all Control Memory locations are filled with the random pattern.
e) Read the contents of the first memory section that was written into, and then verify that that the contents of every location in that section of memory is identical to the original random pattern.

f) Using the pattern in the first-written section of Control Memory as the standard to which the contents of other locations in Control Memory will be compared, read each remaining memory section and verify that each location contains the same, original random pattern.

g) Steps e) and f) are repeated five times (reread count); that accomplished, the test restarts at step a).

When RESET is keyed during this program, it will cause the KEY SF'? message to be displayed.

6.3.2.3 ROWPAT

This diagnostic performs a bit-by-bit test of Control Memory, searching for a bit location in a row or column common to the "Test Cell", which may have been changed when this "Test Cell" was written into. In order to understand the nature of this test, the following terms should be understood.

Test Cell - The bit location being tested in a memory chip (24 chips simultaneously).

Conflict Cell - The bit location in a memory chip being tested for conflict with the Test Cell.

Row - A row of addresses within the memory chip, one of which is the test cell row address.

Column - A column of addresses within the memory chip, one of which is the test cell column address.

Board Row - One of the three rows of 24 memory chips located on a Control Memory pc board.

Test Pattern - The pattern expected to be found in all other cells (conflict cells). Either 0 or 1 depending on which pass the program is executing.

Memory Test Area - From address 1000 to the end of memory if the program is in low memory, and from 0000 to 1000 if program is in high memory.

The diagnostic is performed as follows:

a) Flood the current memory test area with zeroes.
b) Read the current test cell for the flood pattern.
c) Compliment the flood pattern and write into the test cell.
d) Read the test cell for the test pattern.
e) Read the conflict cell for the flood pattern.
f) Repeat steps d) and e) making the conflict cell the next location within the column and then within the row.
g) Write the flood pattern at the test cell.
h) Repeat steps b) through g), making the test cell the next location within the row until the test cell has stepped through each memory location within that row.
i) Repeat steps b) through h) for each row within the memory test area.
j) Flood the current memory with ones (1's) and repeat steps a) through j).
k) Move the test program from low memory to high memory and repeat steps a) through j).
l) Move the test program from high to low memory.

When RESET is keyed during this program, it will cause the KEY SF'? message to be displayed.

NOTE: ERROR-MESSAGE INFORMATION FOR CONTROL MEMORY TESTS IS DOCUMENTED IN PARAGRAPH 6.3.4.1

6.3.3 DATA MEMORY (USER MEMORY) DIAGNOSTICS

6.3.3.1 ADDRESSING

Generally speaking, this diagnostic is designed to read from start to end of User Memory and vice-versa, searching for a memory location that may have been changed when writing into a different location. This addressing test is specifically accomplished as follows:

a) Flood memory with 5A's (0101 1010).

b) Starting at the beginning of User Memory and searching forward to the end, each location is read and checked for the 5A pattern. If the location verifies "O.K." when checked, an A5 (1010 0101) is written at that location.

c) Starting at the end and searching backward to the beginning of User Memory, each location is read and checked for the A5 pattern. If the location verifies "O.K." when checked, a 5A is written at that location.

When RESET is keyed during this program, the KEY SF' message should be displayed.

6.3.3.2 MAT C&S

This diagnostic is designed to test from start to end of User Memory, and is accomplished as follows:

1) Determine the length of a random pattern to be written to all of User Memory. The length is from 1 to 256 8-bit random characters.

2) Write the random pattern into a section of User Memory.

3) Read the last-written section of User Memory and write into the next section.

4) Repeat step 3 until all of User Memory is filled with the random pattern.

5) Read the contents of the first section of User Memory that was written and verify that it is correct by regenerating the pattern.

6) Using the pattern in the first-written section of memory as the original, read the remaining sections of memory and verify their accuracy against the first.

7) Repeat steps 5 and 6 five times (reread count) and and then repeat the entire procedure, starting at step 1, above.

When RESET is keyed during this program, the KEY SF'? message should be displayed.

6.3.3.3 ROWPAT

This diagnostic tests every User Memory bit location having a row or column address common to the row or column address of the test cell. Typically, one such bit location may have been changed when writing into the test cell. To better understand the nature of this test, the following terms must be understood.

Test Cell - The bit location being tested (16 chips simultaneously).

Conflict Cell - The bit location being tested for conflict with the Test Cell.

Row - A row of addresses within the memory chip; one particular location in the row is the test cell.

Column - A column of addresses within the memory chip; one particular location in the column is the test cell.

Chip Row - One of the four rows of 18 memory chips located on each Data (User) Memory board.

Test Pattern - The pattern expected to be found in the test cell. Either one or zero depending on which pass the program is executing.

Flood Pattern - The pattern expected to be found in all other cells (conflict cells). Either zero or one, depending on which pass the program is executing.

The diagnostic is performed as follows:

a) Flood all of User Memory with zeroes.
b) Read the current test cell for the flood pattern.
c) Compliment the flood pattern and write that into the test cell.
d) Read the test cell for the test pattern.
e) Read the conflict cell for the flood pattern.

f) Repeat steps d) and e), making the conflict cell the next location within the column, and then within the row.

g) Write the flood pattern at the test cell.

h) Repeat steps b) through g), making the test cell the next location within the row until the test cell has stepped through each memory location within the row.

i) Repeat steps b) through h) for each row in User Memory.

j) Flood all User Memory locations with one's and repeat steps b) through i).

When RESET is keyed during this program, the KEY SF'? message should be displayed.

NOTE:

ERROR-MESSAGE INFORMATION FOR DATA (USER) MEMORY TESTS IS DOCUMENTED IN PARAGRAPH 6.3.4.2

6.3.4 DIAGNOSTIC ERROR MESSAGE INFORMATION & IDENTIFICATION OF FAULTY RAMS

6.3.4.1 ERROR MESSAGE INFORMATION FOR CONTROL MEMORY TESTS

* If a failing Control Memory location is between 0000-1FFF or 4000-4FFF, replace the 6788 board in the MVP chassis Control Memory position #1. Otherwise, replace the 6788 pc in Control Memory position #2 (Ref. Figure ?)

* If an error is detected, the error message will be displayed under the same test name. The test will be restarted, and if another error occurs, that message will be displayed under the first error message. This procedure repeats until the screen is full. At this point, "CONTINUE" may be keyed to continue the test.

* Occasionally, MAT C&S will display two error messages on the same line when it cannot isolate the problem completely; the more likely error is displayed first.

* When the system detects a memory failure, one of the following error messages is displayed:

AECM -- Addressing Error in Control Memory
BECM -- Bit Error in Control Memory
PECM -- Parity Error in Control Memory
VECM -- Verify Error in Control Memory

EXPLANATIONS:

1) AECM aaaa bbbb xxxxxx

Where: aaaa = The address of the instruction in error
bbbb = The conflicting address
xxxxxx = An XOR of the expected and actually-read instruction

This error indicates that writing to Control Memory location bbbb seems to modify location aaaa. The "1" bits in the xxxxxx field of the display indicate which bit(s) have been modified. The error could also occur if a chip at location aaaa had a marginal failure.

2) BECM aaaa xxxxxx

Where aaaa = The address of the instruction in error
xxxxxx = An XOR of the instruction actually read from memory with the instruction that was expected to be there.

This error implies that a bit error was detected while reading Control Memory. The "1" bits in the xxxxxx field of the display indicate which bit(s) are incorrect.

3) PECM aaaa dddddd

Where aaaa = The address of the instruction with bad parity.
dddddd = The instruction located at aaaa. The instruction is reread when displayed and thus may not be the same as when the error occurred.

This error implies that bad parity was detected during execution of the diagnostic. Bad parity may be the result of:

a) Bits dropped
b) Bits picked up
c) Bad parity written
d) Bad parity-control logic

4) VECM aaaa

Where: aaaa = An address in the section of Control Memory that does not verify correctly.

6.3.4.2 ERROR MESSAGE INFORMATION FOR DATA MEMORY TESTS

* If the CPU has 6787 pc loading, and if the failing memory location is between 0000-7FFF, replace the 6787 in Data (User) Memory position #1; if not, change the 6787 in position #2.

* If the CPU has 7587 pc loading, and if the failing memory location is between 0000 of bank #1 and FFFF of bank #2, replace the 7587 in Data (User) Memory position #1; if not, change the 7587 in Data (User) Memory position #2.

* If an error is detected, the error message will be displayed under the test name. The test will then be restarted, and if another error occurs, that message will be displayed under the first error message. This procedure repeats until the screen is full. At this point, "CONTINUE" may be keyed to continue the test.

* If an error occurs, the message will be displayed on the screen unless "P" or "T" was keyed at the beginning of the diagnostic. "P" will print the errors on the printer selected by /215, and "T" will print the errors on device /204. Execution of the diagnostic will continue after the error message is printed.

* Occasionally, MAT C&S will display two error messages on the same line when it cannot isolate the problem completely; the more likely error is displayed first.

* When the system detects a memory failure, one of the following error messages should be displayed:

a) AEDM -- Addressing error in Data Memory (User Memory)
b) BEDM -- Bit error
c) PEDM -- Parity error
d) REDM -- Read error
e) VEDM -- Verify error

EXPLANATIONS:

a) AEDM ss.aaaa ss.bbbb xx

Where: ss = Memory bank containing the error (00 = bank #1; 40 = bank #2; 80 = bank #3; C0 = bank #4)
aaaa = Address of the data in error
bbbb = Conflicting address
xx = XOR of the expected and actually-read data.

This error indicates that writing to location bbbb seems to modify location aaaa. The "1" bits in the xx field of the display indicate which bits have been modified. The error could also occur if a chip at location aaaa had a marginal failure.

b) BEDM ss.aaaa xxyy

Where: ss = Memory bank containing the error (00 = bank #1; 40 = bank #2; 80 = bank #3; C0 = bank #4)
aaaa = Address of the data in error
xxyy = XOR of the data actually read from User/Data memory with the data that was expected to be there.
xx = Corresponds to the byte at location aaaa
yy = Corresponds to the byte at location aaaa+1

This error implies that a memory error was detected while reading User/Data Memory. The "1" bits in the xxyy field of the display indicate which bit(s) are not correct. If all the bits are zero, one of the two parity bits associated with the pair of bytes read is incorrect.

c) PEDM ss.aaaa

Where: ss = Memory bank containing the error (00 = bank #1; 40 = bank #2; 80 = bank #3; C0 = bank #4)
aaaa = Data memory address (i.e., the current value of the PC's) at the time of the error. This is probably, but not necessarily, the address of the memory location with bad parity.

This error implies that bad parity was detected during a read of 8-bit User/Data Memory.

Bad parity may be the result of:

1) Bits dropped
2) Bits picked up
3) Bad parity-check logic

This error should be serious enough to warrant the executing of a User/Data Memory diagnostic. However, it may be possible to attempt re-execution of the currently-loaded system program. If the error is reported again, a User/Data Memory diagnostic should be run to locate the bad memory chip.

NOTE:

In order to determine which bit is bad, a technician may ground L41 pin 3 on the 6789 board; this action disables parity-error logic. If this is performed, a different error message will be displayed.

d) REDM ss.aaaa xx

Where: ss = Memory bank containing the error (00 = bank #1; 40 = bank #2; 80 = bank #3; C0 = bank #4)
aaaa = Address of the data in error
xx = XOR of the data in memory with the data that was expected to be there.

This error implies that a memory error was detected while reading User/Data Memory. The "1" bits on the xx field of the display indicate which bits are not correct. If all the bits are zero, a bit in the other byte of the pair of bytes is incorrect.

e) VEDM ss.aaaa

Where: ss = Memory bank containing the error (00 = bank #1; 40 = bank #2; 80 = bank #3; C0 = bank #4)
aaaa = Address of the data in error

This error is reported to a system program being given control after loading, or when memory is verified in response to RESET or CLEAR being executed. The area of User/Data Memory used for storing constants (BASIC verb tables, math constants, messages) does not verify correctly.

The operator should attempt to reload the particular system system program. If the error recurs, however, the User/Data Memory Diagnostic should be run.

6.3.4.3 MEMORY DIAGNOSTIC INTERPRETATIONS USING THE MEMORY ERROR CHIP IDENTIFIER (MECI) PROGRAM

MECI is not a diagnostic, but it is a program that provides a means, other than using RAM-board layout charts, for locating RAM failures. MECI requests the exact configuration of Control and Data (User) Memory, then waits for the operator to key in an error message that occurred during a memory diagnostic or during the loading of BASIC-2. That accomplished, the program "points out" the failing RAM by displaying a graphic of the pc board with an 'X' at the location of the bad RAM.

The part number for the MECI program diskette is WL# 701-2452. The program is self-explanatory; however, the following stipulations apply.

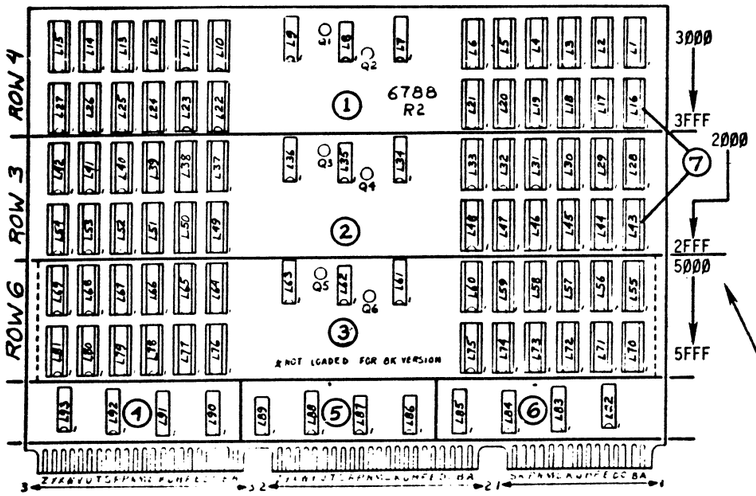
1) Hardware Requirement: 2200VP/MVP with 16K memory and an 80 x 24 CRT.
2) "RETURN" must be keyed after each field. Keying "RETURN" prior to the end of a field causes the next field to be displayed.
3) The operator must specify the disk file from which data will be compared against PECM data (if the error occurred while trying to load from disk). If no file is desired, key in spaces and then "RETURN"; the file name defaults to "BASIC-2 (@@)".
4) Press any non-SF key to clear display and enter a 'next' error; or, press any SF key to enter a different memory configuration. This is not valid when in the EDIT SYSTEM ERROR mode.
5) Note that User/Data Memory board #1 is close to the CPU logic boards, and board #2 is close to the CPU power supply. (Ref: Figure ?)
6) When in the EDIT SYSTEM ERROR mode, simply key in the error message that was displayed when the RAM fault was detected. Key "RETURN"; MECI will point out, in the display of terminal #1, which RAM has failed.

6.3.4.4 MEMORY DIAGNOSTIC INTERPRETATIONS BY DIAGRAM

If MECI is not available, the following charts will point out which RAM is failing. To use the charts:

CONTROL MEMORY DIAGNOSTIC INTERPRETATION

*=SAME HARDWARE ASSIGNMENTS ON BOTH BOARDS



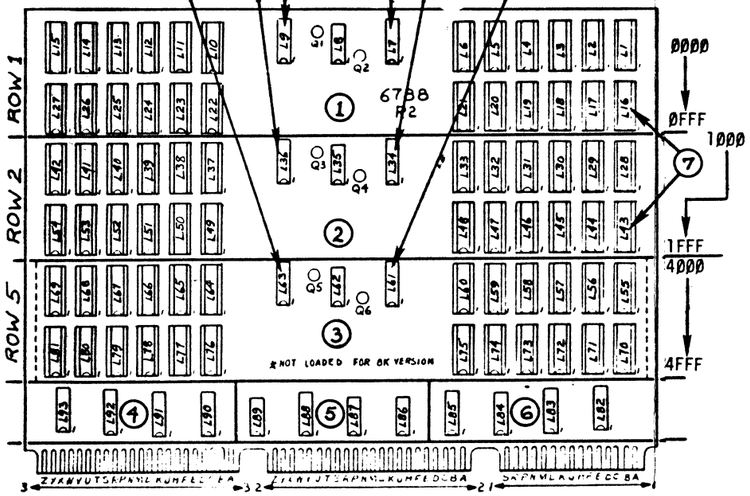
BOARD #2

HEX ADDRESSES IN CONTROL MEMORY

ADDRESS LINES A0-A5 FOR L1-L6,L10-L15,L16-L27

ADDRESS LINES A0-A5 FOR L28-L33,L37-L42,L43-L54

ADDRESS LINES A0-A5 FOR L55-L60,L64-L69,L70-L81



BOARD #1

HEX ADDRESSES IN CONTROL MEMORY

EXAMPLE DIAGNOSIS:

ERRORS DISPLAYED DURING CONTROL MEMORY DIAGNOSTIC:

SF#:	TEST:	RESULT DISPLAYED: MESSAGE	PASS #
01	ADDRESS 24	"ERROR BETWEEN 2BBF AND 2BC0 (004000)	#0000"
02	MAT C&S 24	"ERROR-PC'S=2BA0 (0D0D0D/0D4D0D) XOR=004000	#0000"
03	ROWPAT 24	"FAILURE AT PC'S 2BAD (000000/004000) XOR=004000	#0000"

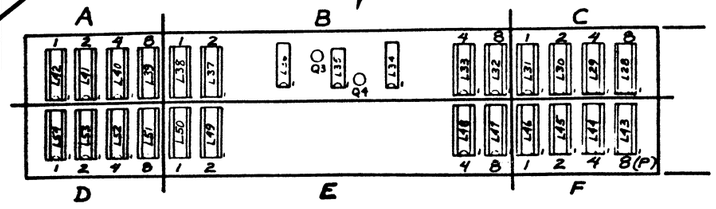
NOTE THAT IN EACH TEST,XOR YIELDS 004000 BETWEEN CONTROL MEMORY LOCATIONS 2BBF AND 2BC0, LOCATED IN ROW #3 (BOARD #2).

FAILING BIT IN ROW SECTION D

F E D C B A — ROW SECTIONS (SEE BELOW)

0 0 4 0 0 0

XOR RESULT



FROM BOARD FIGURES ABOVE:

(1) = CHIP ENABLES FOR ROWS 1&4 (4096x24 BITS EACH)

(2) = CHIP ENABLES FOR ROWS 2&3 (4096x24BITS EACH)

(3) = CHIP ENABLES FOR ROWS 5&6 (RAM NOT LOADED ON 8K BOARDS)

(4) = I/O BUFFER

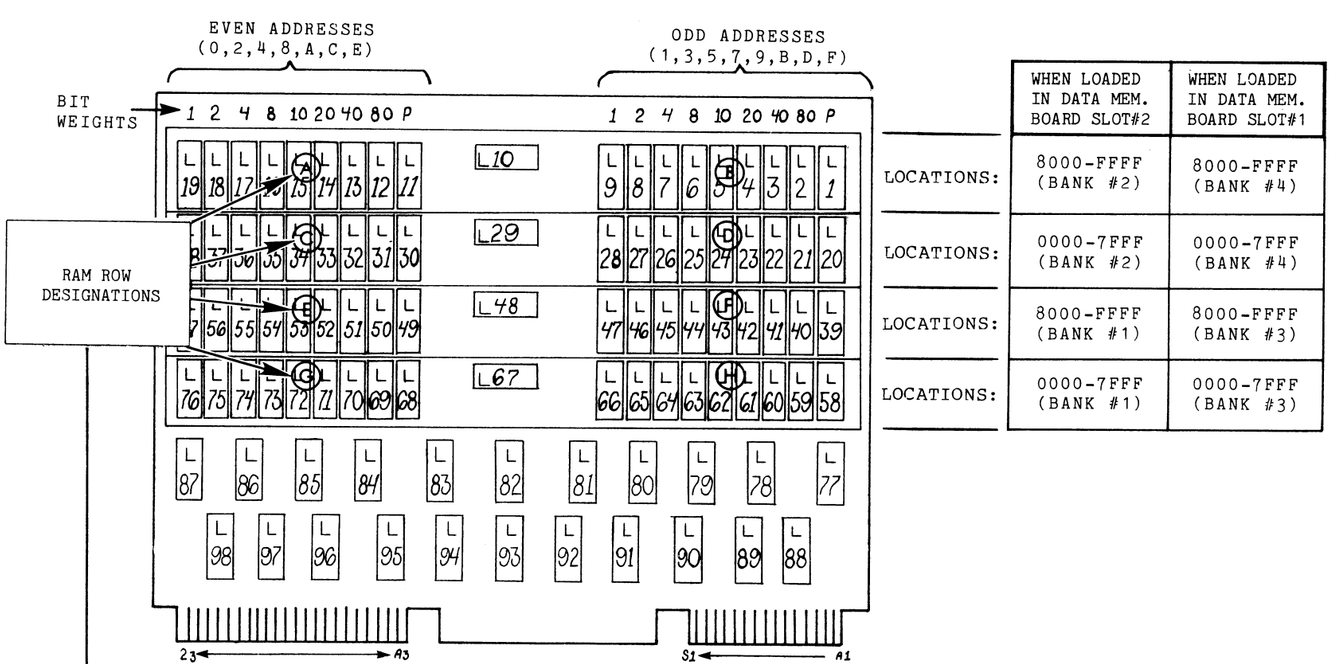
(5) = SELECT DECODER

(6) = I/O BUFFER

(7) = PARITY BIT(S)

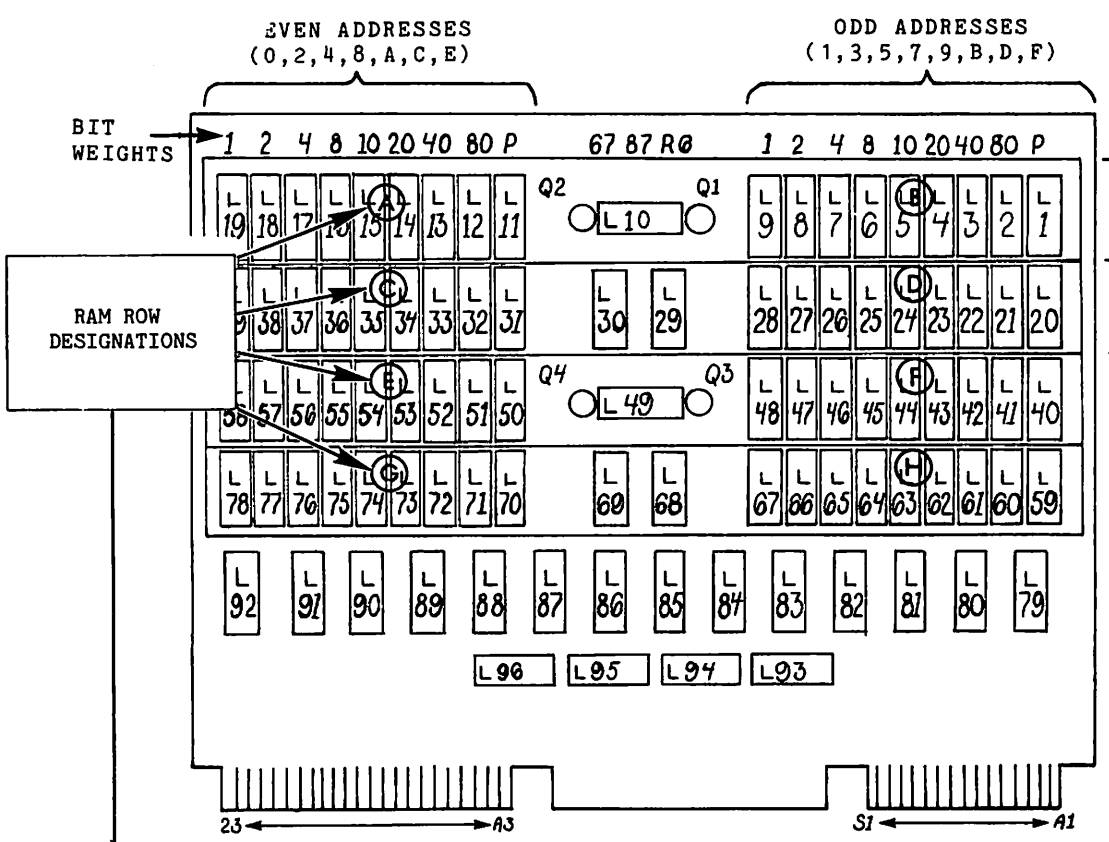
FIGURE 6-1

FIGURE 6-2 DATA MEMORY (6787) DIAGNOSTIC DIAGRAM



	WHEN LOADED IN DATA MEM. BOARD SLOT#2	WHEN LOADED IN DATA MEM. BOARD SLOT#1
LOCATIONS:	8000-FFFF (BANK #2)	8000-FFFF (BANK #4)
LOCATIONS:	0000-7FFF (BANK #2)	0000-7FFF (BANK #4)
LOCATIONS:	8000-FFFF (BANK #1)	8000-FFFF (BANK #3)
LOCATIONS:	0000-7FFF (BANK #1)	0000-7FFF (BANK #3)

BOARD NOMEN-CLATURE	ROWS LOADED WITH RAM ICs A	B	C	D	E	F	G	H	RAM SIZE:
6787					X	X	X	X	16K
6787-1	X	X	X	X	X	X	X	X	32K



HEX ADDRESS LOCATIONS & BANK NUMBERS

	WHEN LOADED IN DATA MEM. BOARD SLOT#1	WHEN LOADED IN DATA MEM. BOARD SLOT#2
LOCATIONS:	4000-5FFF (BANK #1)	COOO-DFFF (BANK #1)
LOCATIONS:	6000-7FFF (BANK #1)	EOOO-FFFF (BANK #1)
LOCATIONS:	0000-1FFF (BANK #1)	8000-9FFF BANK #1)
LOCATIONS:	2000-3FFF (BANK #1)	A000-BFFF (BANK #1)

BOARD NOMEN-CLATURE	ROWS LOADED WITH RAM ICs A	B	C	D	E	F	G	H	RAM SIZE
7587-1					X	X	X	X	64K
7587-2			X	X	X	X	X	X	96K
7587-3	X	X	X	X	X	X	X	X	128K

FIGURE 6-3 DATA MEMORY (7587) DIAGNOSTIC DIAGRAM

1) Find the appropriate configuration in chart #1
2) Find the bank # and address in the bank that corresponds with the bank and address that was displayed in the error message. This step points out which ROW of RAM in the two boards contains the failing chip.
3) Chart #2 points out which half of the row contains the faulty RAM, depending on whether the address of the error location is even or odd.
4) Any bits that are <u>on</u> (1) in the XOR field are bad.

6.3.5 REGISTER DIAGNOSTICS

6.3.5.1 GENERAL PURPOSE REGISTERS

This diagnostic is designed to test the F0-F7, CH, CL, PH, PL, SL and K registers in such a manner that it may be determined whether or not bits have gone bad, or whether a conflict in addressing (of registers) exists. It is accomplished in the following manner:

a) Flood all registers with all zeroes.
b) For each register:
    1. Set the test pattern to 00.
    2. Set the test register to the test pattern value.
    3. Verify that the test register holds the test pattern value.
    4. Verify that the other registers have not been changed.
    5. Add 01 to the test pattern value.
    6. Repeat steps 2 through 5 until test pattern equals 00.
    7. Repeat steps 1 through 6 until all registers have been tested. Note that the SH register is not tested, due to the ability of system hardware to change its bit status.

A check on register K is made prior to the occurrence of any test displays. Should REGISTER TEST fail to appear on the CRT, then register K may be failing.

When RESET is keyed during this program, the KEY SF'? message should be displayed.

When HALT/STEP is keyed during this program, the program will be interrupted only after an error has been detected and displayed. To resume execution after the program has halted, key HALT/STEP again.

Normal Display:

```
REGISTER TEST
# LLLL
```

where: LLLL = number of completed loops

6.3.5.2 GENERAL REGISTERS ERROR DISPLAYS

a)

```
REGISTER TEST
# FFFF
REGISTER TT AND CC ERROR (XX)
# LLLL
```

where: FFFF = Number of completed loops at time of error
TT = Name of register under test
CC = Name of conflict register
XX = Contents of register CC

This error is caused when testing register TT, register CC was found not to contain the expected.

b)

```
REGISTER TEST
# FFFF
REGISTER TT ERROR (XX)
# LLLL
```

This error is caused when the register under test fails to hold the test pattern.

6.3.5.3 AUXILIARY/STACK

This diagnostic is designed to check the Auxiliary registers to determine whether each Auxiliary register will:

a) Hold a particular pattern.
b) Have any effect on any other auxiliary register.
c) Have any effect on any stack level.

Two separate patterns are used by the routine:

a) Test pattern - One of 8 patterns (below) which is expected to be in the Auxiliary register under test.

1.	0000 0001	0000 0001
2.	0000 0010	0000 0010
3.	0000 0100	0000 0100
4.	0000 1000	0000 1000
5.	0001 0000	0001 0000
6.	0010 0000	0010 0000
7.	0100 0000	0100 0000
8.	1000 0000	1000 0000

b) Conflict pattern - Either all 0's or all 1's, depending on what pass the program is executing.

The tests are executed as follows:

a) All Auxiliary registers and the Stack are initialized with the conflict pattern.
b) The current test Auxiliary register is written with the current test pattern.
c) The test Auxiliary register is read as follows:

1. TPA - writes the test pattern.
2. PC's are complemented.
3. XPA - reads the test pattern.
4. PC's are checked against the expected pattern.

5. TAP - reads the complemented test pattern.
6. PC's are complemented again.
7. PC's are checked against the expected pattern.

d) The remaining Auxiliary registers and the stack are checked to determine whether or not they still contain the conflict pattern.

e) Steps b) through d) are repeated until all test patterns have been tested.

f) Steps b) through e) are repeated until all 32 Auxiliary registers have been tested.

g) The conflict pattern is complemented and steps a) through f) are repeated.

When RESET is keyed during this program, the KEY SF'? message should be displayed.

When HALT/STEP is keyed during this program, the program will be interrupted only after an error has been detected and displayed. To resume execution after program has halted, key HALT/STEP again.

NORMAL DISPLAY

```
AUXILIARY TEST
# LLLL
```

where: LLLL = number of completed loops

6.3.5.4 AUXILIARY/STACK ERROR DISPLAYS

a)

```
AUXILIARY TEST
# FFFF
AUX TT FAILURE (XXXX)
# LLLL
```

where: FFFF = Number of completed loops at time of error
TT = Auxiliary register under test
XXXX = XOR of expected and actual

This error occurs when the Auxiliary register under test is found not to contain the expected test pattern.

b)

```
AUXILIARY TEST
# FFFF
AUX TT AND AUX CC FAILURE (XXXX)
# LLLL
```

where: CC = Conflict register

This error is caused when Auxiliary register CC was found not to contain the expected test pattern.

c)

```
AUXILIARY TEST
# FFFF
STACK AND AUX TT FAILURE (XXXX)
# LLLL
```

This error is caused when a Stack level was found not to contain the expected test pattern.

6.3.5.5 STACK/AUXILIARY

This diagnostic is designed to check the Stack, to determine whether each Stack level will:

a) Hold a particular pattern.
b) Have an effect on any other Stack level.
c) Have an effect on any Auxiliary register.

When RESET is keyed during this program, the KEY SF'? message should be displayed.

When HALT/STEP is keyed during this program, the program will be interrupted only after an error has been detected and displayed. To resume execution after program has halted, key HALT/STEP again.

NORMAL DISPLAY

```
STACK TEST
# LLLL
```

where: LLLL = Number of completed loops

6.3.5.6 STACK/AUXILIARY ERROR DISPLAYS

a)

```
STACK TEST
# FFFF
STACK FAILURE (XXXX)
# LLLL
```

where: FFFF = Number of completed loops at time of error
XXXX = XOR of expected and actual

This error is caused when a Stack level fails to maintain the expected pattern.

b)

```
STACK TEST
# FFFF
AUX YY FAILURE (XXXX)
# LLLL
```

where: YY = Auxiliary register

This error is caused when a particular Auxiliary register fails to maintain the expected pattern.

6.4 BASIC-2 LANGUAGE DIAGNOSTIC DISPLAYS

This particular diagnostic will stop on any error relating to the BASIC-2 interpreter. The source of any BASIC-2 Interpreter malfunction may be traced to a fault (or faults) at any level of CPU hardware operation. The following displays will appear during a test run of the 2200VP BASIC Language diagnostic.

BASIC-2 DIAGNOSTIC

```
                    TESTING 2200VP BASIC-2
                          STATEMENTS
TESTING COM.....OKAY                TESTING COM(COM;COM).....OKAY
        COM CLEAR                           LET, IF/THEN/ELSE
        FOR/NEXT/STEP                       STR()
        DATA/READ/RESTORE                   DEFFN
        GOSUB/RETURN                        DEFFN'/GOSUB'
        ON GOTO/GOSUB                       RETURN CLEAR
```

```
                    TESTING 2200VP BASIC-2
                          ALPHANUMERICS
TESTING ALL, HEX.....OKAY           TESTING BIN.............OKAY
        LEN                                 NUM
        POS                                 VAL
        VER                                 CONCATENATION
        ADD(C)                              AND,OR,XOR
        BOOL                                DAC
        DSC                                 SUB(C)
```

```
                    TESTING 2200VP BASIC-2
                    MATHEMATICAL FUNCTIONS
TESTING #PI,RND......OKAY              TESTING INT.............OKAY
        SIN                                    COS
        TAN                                    ARCSIN
        ARCCOS                                 ARCTAN
        ABS,SGN                                LOG
        EXP                                    SQR
        LGT                                    FIX,MOD
        ROUND(X,Y)                             MAX,MIN
```

```
                    TESTING 2200VP BASIC-2
                      SCIENTIFIC MATRIX
TESTING MAT EQUALITY...OKAY            TESTING MAT ADD, SUB.....OKAY
        MAT CON,XER,IDN                        MAT SCALAR MULT
        MAT TRANSPOSE                          MAT MULT
        MAT INVERSE                            MAT REDIM
        MAT READ
```

```
                    TESTING 2200VP BASIC-2
                      COMMERCIAL MATRIX
TESTING MAT CONVERT....OKAY            TESTING MAT MOVE.........OKAY
        MAT SORT                               MAT COPY
        MAT MERGE                              MAT SEARCH
```

```
                    TESTING 2200VP BASIC-2
                         GENERAL I/O
TESTING $IF ON.........OKAY              TESTING $TRAN.............OKAY
        $GIO
```

```
                    TESTING 2200VP BASIC-2
                         GENERAL I/O
        SPACK                                    SUNPACK
INTERNAL FORMAT.......OKAY               INTERNAL FORMAT..........OKAY
DELIMITER FORMAT                         DELIMITER FORMAT
FIELD FORMAT                             FIELD FORMAT
MISCELLANEOUS
```

6.5 2236D AND 2236MXD DIAGNOSTIC PROCEDURES

Refer to Module Repair Guides 3, 3.1, and 3.2.

NOTES:

NOTES:

SECTION 7

SYSTEM-LEVEL MAINTENANCE, ADJUSTMENTS, AND TROUBLESHOOTING

This section contains preventive maintenance, adjustment, and troubleshooting procedures for the 2200MVP system. Only the CPU and the 2236D Interactive Terminals are given detailed treatment here. All available peripherals are fully documented in other Wang or OEM manuals. See the preface of this manual for a listing of these publications.

7.1 PREVENTIVE MAINTENANCE

To ensure trouble-free operation the 2200MVP must have periodic preventive maintenance, consisting of inspecton, cleaning, and adjustments. The PM procedures for the CPU and the 2236D Terminals are given in this section.

The following preventive maintenance routines should be performed once every six to twelve months. This preventive maintenance schedule assumes a clean operating environment and a normal operating time during the standard five-day, 40 hour weeks. A dusty environment or any substantial increase in system operating time will require that the preventive maintenance be scheduled at closer intervals. In addition, these maintenance routines should be performed during each unscheduled service call.

7.1.1 CENTRAL PROCESSING UNIT

The following preventive maintenance procedure should be performed every six to twelve months.

1. Check the unit cooling fan for proper operation.

2. Clean the CPU according to the following procedure:

   a. Remove the top and bottom covers from the CPU.
   b. Remove the I/O controllers.

c. Use a soft-bristle brush to remove dust from the inside of the CPU.
d. Remove each printed circuit board from the CPU and clean the finger connectors, using an eraser.
e. Using an eraser, clean the finger connectors of each I/O controller, and then reinstall the controllers in the CPU.
f. Use a mild detergent and a soft cloth or sponge to remove dirt and grime from the CPU cabinetry. Do not use abrasive or corrosive chemicals.
g. Replace the top and bottom covers to the CPU and tighten them securely.

3. Check the power supply for voltage and ripple according to the procedure given in section 7.3.2. Adjust if necessary.

4. Run the Diagnostics discussed in section 6, as needed, to confirm proper operation of the CPU circuitry.

7.1.2 2236D INTERACTIVE TERMINALS

The following preventive maintenance procedure should be performed every six to twelve months.

1. Check the unit cooling fan for proper operation.

2. Clean the 2236D terminal according to the following procedure:

a. Remove the top cover from the unit.
b. Use a soft-bristle brush to remove dust and dirt from inside the unit (especially from the CRT and Flyback).
c. Use a soft cloth and a mild detergent to clean the face of the CRT. Do not use an abrasive cleanser.
d. Use a soft-bristle brush to remove dust and dirt from the keyboard.
e. Clean the outside covers of the unit with a soft cloth or sponge and a mild detergent.

f. Return the top cover and tighten securely.

3. Check the power supply voltage and ripple according to the procedure given in section 7.3.3. Adjust if necessary.

4. Check the unit for proper operation.

7.1.3 PREVENTIVE MAINTENANCE FOR SYSTEM PERIPHERALS

Each model printer, plotter, disk drive, and tape drive has its own preventive maintenance schedule and procedure, which is documented in a specific maintenance publication for that model. For a summary of these publications, see the 2200MVP System-Level Documentation list in the preface of this manual.

7.2 SYSTEM-LEVEL PREVENTIVE MAINTENANCE

7.2.1 LUBRICATION

No lubrication is required in 2200MVP CPU or the 2236D Terminals. Other system peripherals, especially those containing moving parts, may have special lubrication requirements. See specific maintenance manuals for instructions.

7.2.2 SYSTEM ECN'S

Ensure that the 2200MVP system is kept up-to-date by verifying and installing all required ECN's.

7.3 ADJUSTMENTS

Adjustments, particularly electrical adjustments, should be performed only when the parameter measured proves to be out of tolerance. Do not make electrical or mechanical adjustments indiscriminately. Before making any adjustments, be certain that the measuring instruments are properly calibrated.

7.3.1 RECOMMENDED TEST EQUIPMENT/TOOL LIST

1. Digital Voltmeter, with an accuracy of at least ± 1% of full scale (or of reading) and 1 mv resolution factor. Analog Multimeters have accuracy and resolution factors that are unacceptable for certain critical measurements.
   Acceptable Type/Equivalent: FLUKE #8000A

2. Multimeter, 20,000 ohms/volt (minimum); 2% or better full scale accuracy; for less critical measurements.
   Acceptable Type/Equivalent: TRIPLETT VOM #630NA

3. Oscilloscope, with two X1 probes and two X10 probes.
   Acceptable Type/Equivalent: TEKTRONIX #465

4. Allen wrench Set.

5. Plastic alignment screwdriver for video display adjustments.

6. Torque driver (Utica, TS-100).

7. Hex nut driver set.

8. Heavy duty screwdriver with well-insulated handle, for discharging video display anode voltage.

9. Insulated heavy-gauge ground wire with insulated alligator clips, for use with item 8, above.

10. Small screwdriver with insulated shank, used mostly for voltage adjustments.

NOTE:

In addition to the above list, many system peripherals will require special tools and test equipment for adjustment and maintenance.

7.3.2 CPU VOLTAGE ADJUSTMENT PROCEDURE

1. Turn the system power OFF.

2. Remove the top cover of the CPU.

3. Turn the system power ON.

4. Check DC voltages with a digital voltmeter for the specified values, as listed in Table 7-2. Adjust the trimpots where indicated in Figure 7-1 to obtain correct voltage levels where necessary.

IMPORTANT:

Be sure to connect the COMMON lead of the voltmeter to a ± 0V connection, NOT the chassis or I/O controller rail. Erroneous readings will result if chassis ground is used as the voltmeter reference. The oscilloscope ground clip should also be attached to ± 0V, NOT chassis ground.

5. Using an oscilloscope with an X1 probe, measure the ripple at the points indicated in Table 7-2. AC ripple should not exceed the limits specified. If any voltage or ripple measurement is out of specification, troubleshoot the CPU power supply.

6. Note that when increasing RAM capacity by field conversion, or when adding extra I/O capabilities to the CPU, all voltages must be rechecked and readjusted when necessary.

NOTE:

The CPU regulator board will be one of the types shown in Figures 7-1 and 7-2. The standard MVP chassis uses the 6797 board, and the MVP-A uses the 7397 board. These boards are not interchangable. For the location of the regulator board in the CPU chassis, see Figure 1-8.

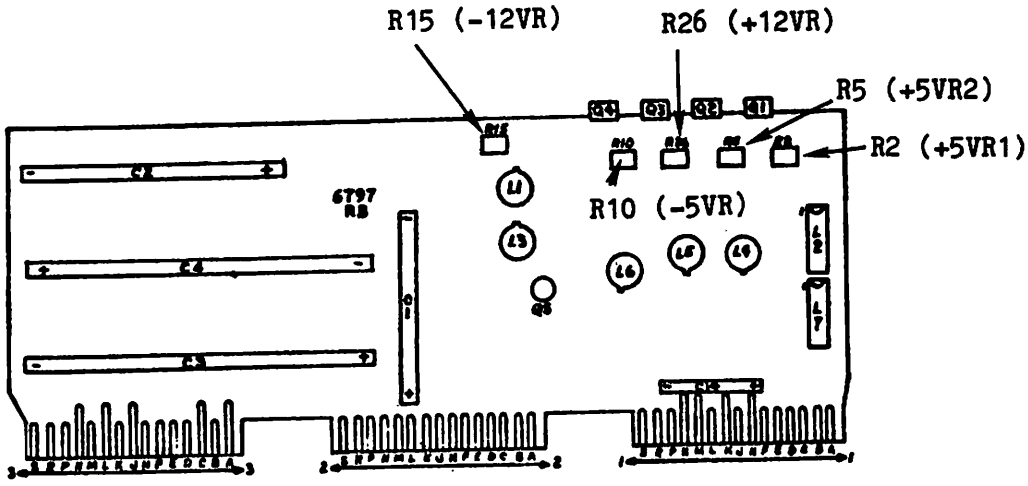


FIGURE 7-1 6797 REGULATOR BOARD

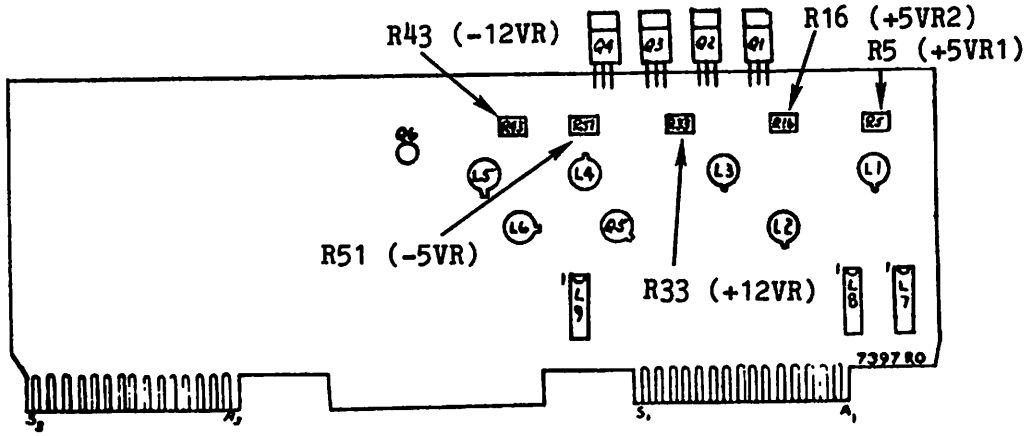


FIGURE 7-2 7397 REGULATOR BOARD

TABLE 7-2 CPU VOLTAGE REGULATOR ADJUSTMENTS

LOCATION	VOLTAGE	LIMITS	ADJUST		RIPPLE
			6797	7397	
Pin J_1	+5VR1	+4.95 vdc to +5.05 vdc	R2	R5	15 mvp-p
Pin L_1	+5VR2	+4.95 vdc to +5.05 vdc	R5	R16	15 mvp-p
Pin M_1	+12VR	+11.95 vdc to +12.05 vdc	R26	R33	15 mvp-p
Pin N_1	-12VR	-11.95 vdc to -12.05 vdc	R15	R43	35 mvp-p
Pin S_1	-5VR	-4.95 vdc to -5.05 vdc	R10	R51	25 mvp-p

7.3.3 2236D ADJUSTMENTS

7.3.3.1 2236D VOLTAGE ADJUSTMENT PROCEDURE

1. Turn the unit power OFF.

2. Remove the top cover of the terminal.

3. Turn the unit power ON.

4. Check DC voltages with a digital voltmeter for the specified values, as listed in Table 7-3. Adjust the trimpots where indicated in Figure 7-3 to obtain correct voltage levels where necessary. Be sure to connect the COMMON lead of the voltmeter to a ± 0V connection, not the chassis, or erroneous readings will result.

5. Using an oscilloscope with an X1 probe, measure the ripple at the points indicated in Table 7-3. AC ripple should not exceed the limits specified. Be sure to connect the oscilloscope ground clip to ± 0V, not to chassis ground. If any voltage or ripple measurement is out of specification, troubleshoot the CPU power supply.

6. A similar procedure should be followed for each peripheral unit having a self-contained power supply.

TABLE 7-3 2236D VOLTAGE REGULATOR ADJUSTMENTS

LOCATION	VOLTAGE	LIMITS	ADJUST	RIPPLE
7067 Pins S/15	+5VR	+4.95 vdc to +5.10 vdc	R4	20 mvp-p
7067 Pin 12	-5VR	-4.90 vdc to +5.10 vdc	R19	15 mvp-p
7067 Pins F/6	+12VR	+11.80 vdc to +12.20 vdc	R10	50 mvp-p
7067 Pins H/7	-12VR	-11.80 vdc to -12.20 vdc	R16	50 mvp-p

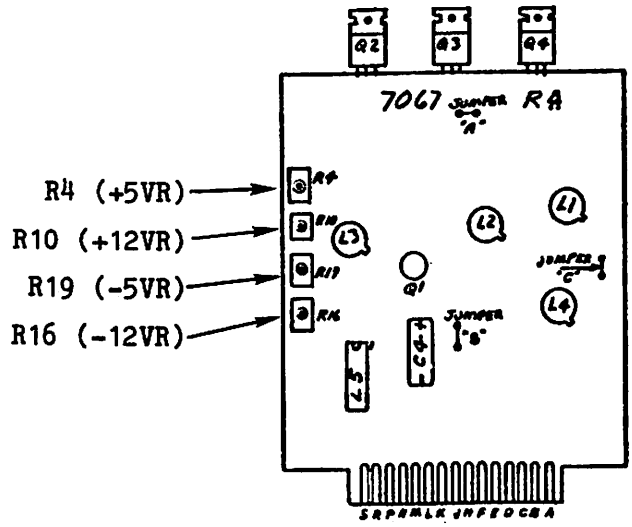


FIGURE 7-3 7067 REGULATOR BOARD

7.3.3.2 VIDEO DISPLAY UNIT ADJUSTMENTS

CAUTION:

No work should be attempted on an exposed Video Display Chassis by anyone not familiar with servicing procedures and precautions.

7.3.3.2.1 SAFETY WARNING

1. A good practice, when working inside any electronic chassis, is to use only one hand. This will avoid the possibility of carelessly putting one hand on chassis or ground and the other on an electrical connection, causing severe electrical shock.

2. Extreme care should be used in handling the cathode ray tube; rough handling may cause implosion, due to atmospheric pressure. Do not nick or scratch the CRT or subject it to any undue pressure.

3. Avoid prolonged exposure at close range to unshielded areas of the cathode ray tube. Possible danger or personal injury from unnecessary exposure to X-ray radiation may result.

7.3.3.2.2 MOTOROLA DISPLAY CHASSIS

1. Remove the cover of the 2236D Interactive Terminal.

2. Connect a voltmeter to pin 22 of the video PCB and adjust Regulator, R74 (see CAUTION below), for a meter reading of +73.0 vdc $\pm$ 1.0 vdc. See Figure 7-4.

CAUTION:

Do not adjust the regulator control through its total range or damage to the display unit may result.

3. Remove the video input cable from the display chassis. Connect a jumper from chassis ground to the center conductor of the input connector.

4. Connect a X10 oscilloscope probe to Q3 collector and adjust Video Bias, R10, for +30 vdc. If Q3 oscillates while adjusting R10, temporarily connect a capacitor having a value from .05 uf to .68 uf @ 25V between Q2 base and ground.

5. Remove the shorting jumper and capacitor (step 4) and reconnect the video cable.

6. Enter the following program in the 2200MVP:

```
1 PRINT "HO";
2 GO TO 1
RUN
EXECUTE
```

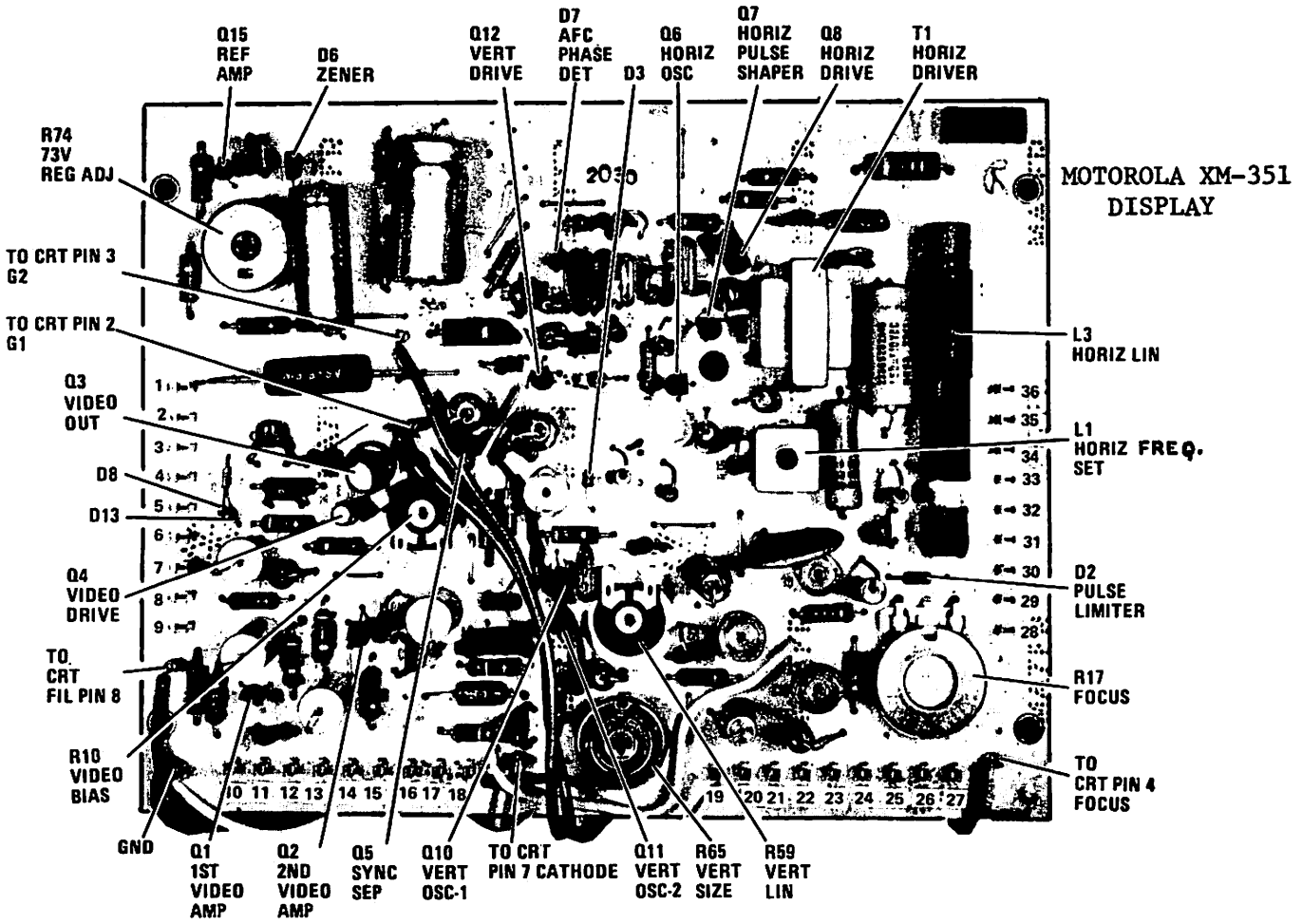


FIGURE 7-4 MOTOROLA VIDEO DISPLAY BOARD

The display should fill with alternate HO characters.

7. Set horizontal hold and vertical hold controls to midrange.

8. Adjust horizontal oscillator coil (L1) for horizontal sync. If an 80 x 24 controller is installed in a system, the horizontal oscillator coil (L1) on the Motorola Video Display Chassis must be adjusted very carefully for a stable display. This adjustment has a limited range of stability with the 80 x 24 display, and must be set in the middle of this stable range. Be sure to turn the power off and on several times after adjusting the coil to be sure horizontal sync is achieved; otherwise another service call will be required to readjust L1.

9. Adjust Vertical Size, R65, for a vertical height of 8.5 inches (21.6 cm).

10. Adjust Width, L4, for 10 inches (25.4 cm) horizontal deflection.

11. Adjust Vertical Linearity, R52, for characters of equal height.

12. Adjust the centering tabs on the CRT yoke for a centered display. Be sure the tabs are at least 90° from each other.

13. Repeat steps 8 through 12 until proper horizontal deflection, vertical deflection, and centering raster are achieved.

14. Adjust Focus, R17, for best overall focus.

7.3.3.2.3 WANG DISPLAY CHASSIS

1. Connect a digital voltmeter to the +12V test point (Point A in Figures 7-5 or 7-6; reference chassis ground).

2. For models with a power supply module, adjust the +12VR on the 7255 for +12.00 vdc ± .10 vdc. See Figure 7-6.

3. For models without a power supply module, adjust the +12V regulator card (7067 PC board) for +12 vdc ± .10 vdc.

4. Connect an oscilloscope to pin M (Point M in Figure 7-5). Adjust the Dynamic Focus coil (Z1) for an amplitude of 300V p-p as observed on the oscilloscope. Disconnect the oscilloscope.

5. Enter a program in the system to display a screen filled with the characters "HO".

6. Set both horizontal hold (R33) and vertical hold (R15) to the middle of the stable display range.

7. Adjust the vertical size (R24) for a vertical height of 8.5 inches (21.6 cm) on the 12" display.

8. Adjust the vertical linearity (R18) for character rows of equal height.

9. Repeat steps 7 and 8 until both requirements can be met.

10. Adjust the width coil (Z2) for 10 inches (25.4 cm) of horizontal deflection on the 12" display.

11. Adjust the horizontal phasing (R35) for characters centered horizontally on the raster (turn the brightness up sufficiently to observe the raster).

12. Adjust the focus (R28) for the best overall focus.

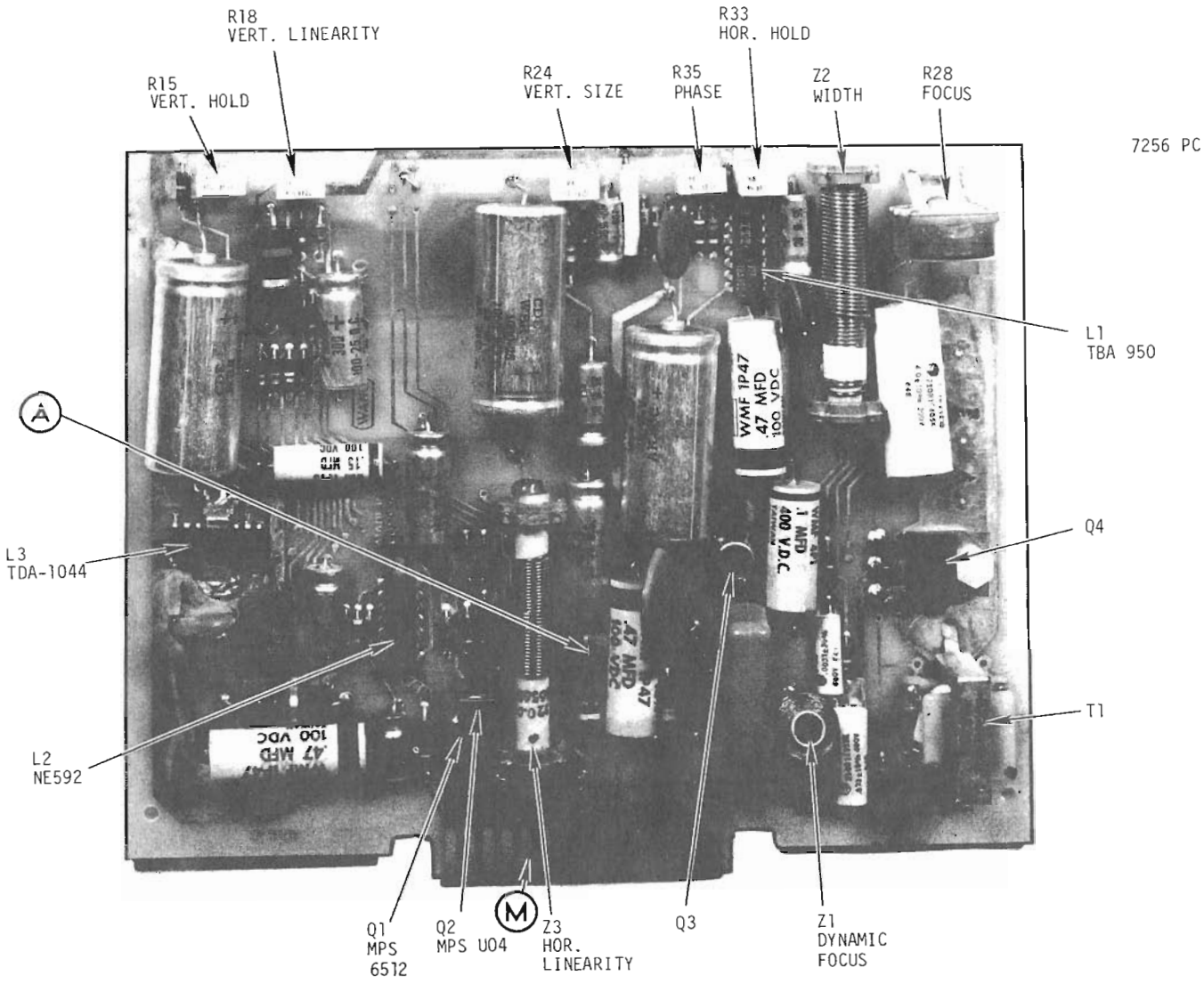


FIGURE 7-5 WANG VIDEO DISPLAY BOARD

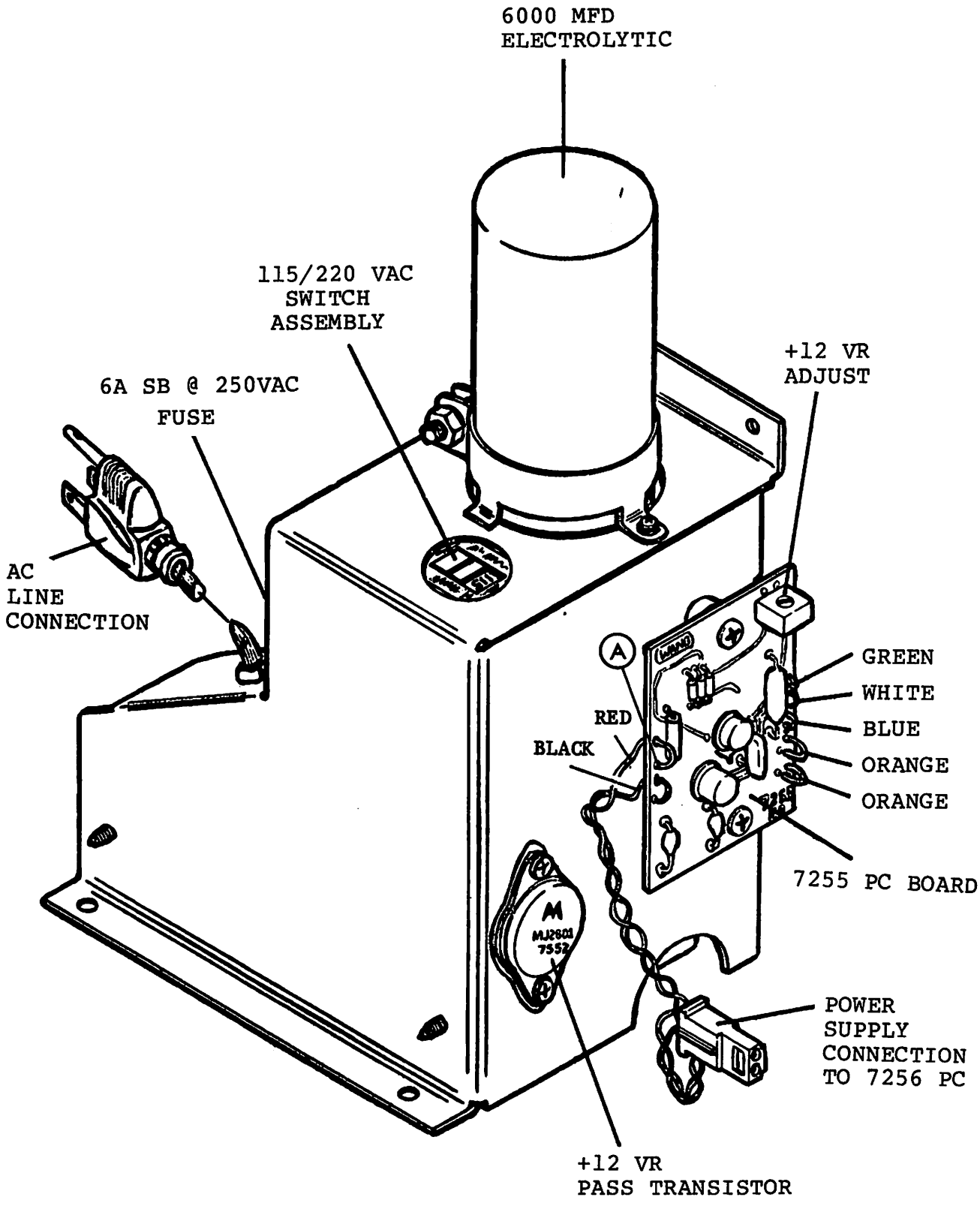


FIGURE 7-6 POWER SUPPLY MODULE FOR WANG DISPLAYS

7.4 TROUBLESHOOTING THE 2200MVP

This section provides troubleshooting aids that will be helpful in identifying the more common system faults. Use a logical approach to troubleshoot the system: observe the problem symptoms carefully, and then isolate the problem by logical deduction.

NOTE:
Be certain to verify or install all required ECN's.

7.4.1 THE CENTRAL PROCESSING UNIT

From a system standpoint, troubleshooting the CPU involves a relatively simple procedure. The following steps should be performed.

1. Remove all peripheral controllers from the CPU. Check the address switch settings. Ensure that all cables from peripherals to controllers are secured. Replace only the 2236MXD and the disk controllers(s). Check all voltages for proper levels. If the problem persists, continue with ROUTINE A (in Section 7.4.3). Otherwise continue with step 2.

2. If the problem persists, replace each board presently in the CPU (and I/O) with a known good board (same revision if possible) until the problem disappears (never rule out the possibility of mutiple problems). If the problem still persists, there may be a software problem.

3. Once the problem has been removed, run all System and BASIC-2 Diagnostics. If any further errors are discovered from these diagnostics, follow the procedures outlined in the 2200MVP Troubleshooting Flowchart (Section 7.4.3). Otherwise, continue with step 5.

4. Replace only the suspected bad peripheral controller with a known good one in the CPU. If the problem recurs and appears to be in the peripheral, troubleshoot that peripheral according to the procedures given in the specific maintenance manual for that peripheral. A list of these manuals in given in the preface of this manual.

5. Plug all peripheral controllers into the CPU and recheck all voltages. Run all system and peripheral diagnostics to ensure that the system operates properly in its final configuration.

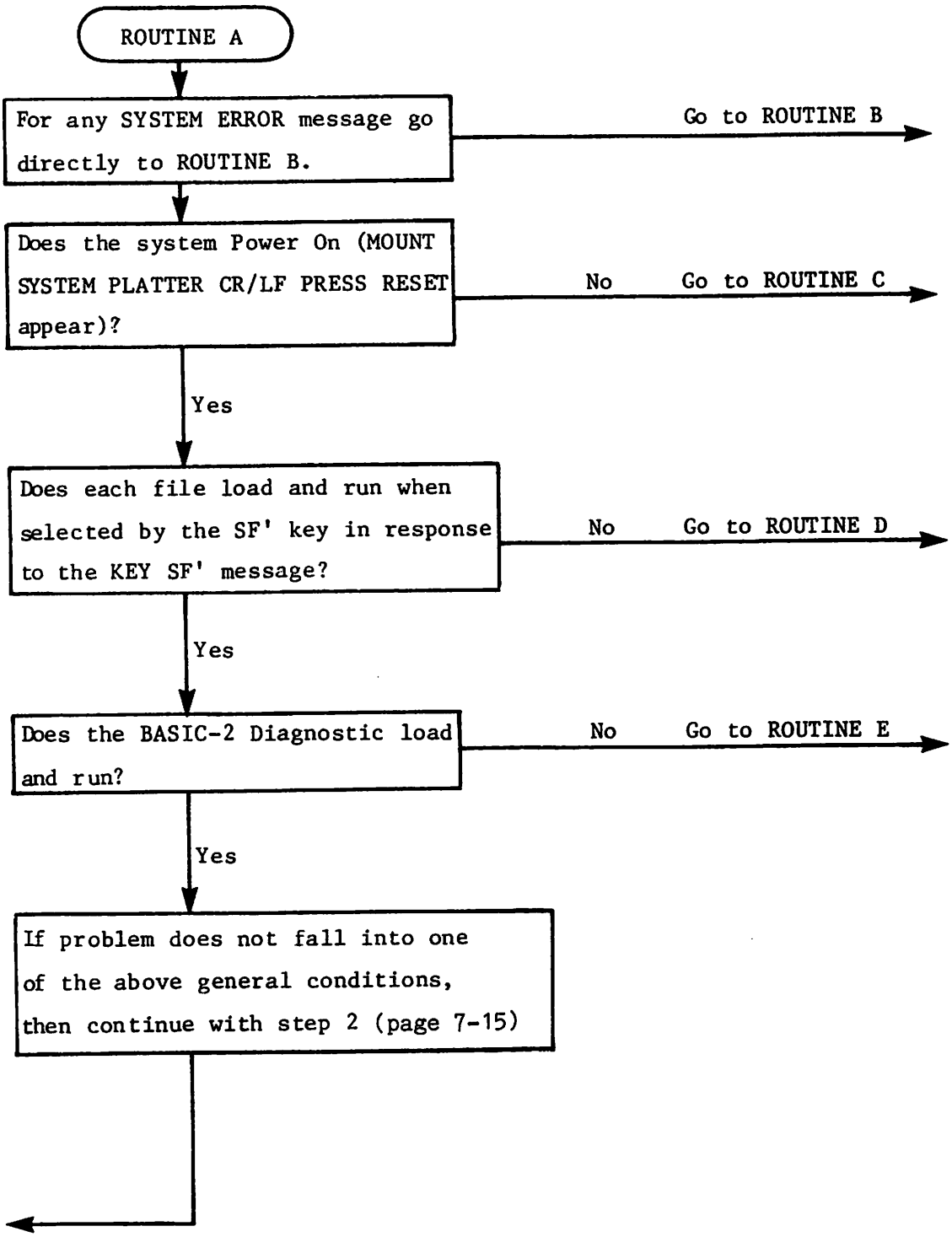
7.4.2 THE SYSTEM PERIPHERALS

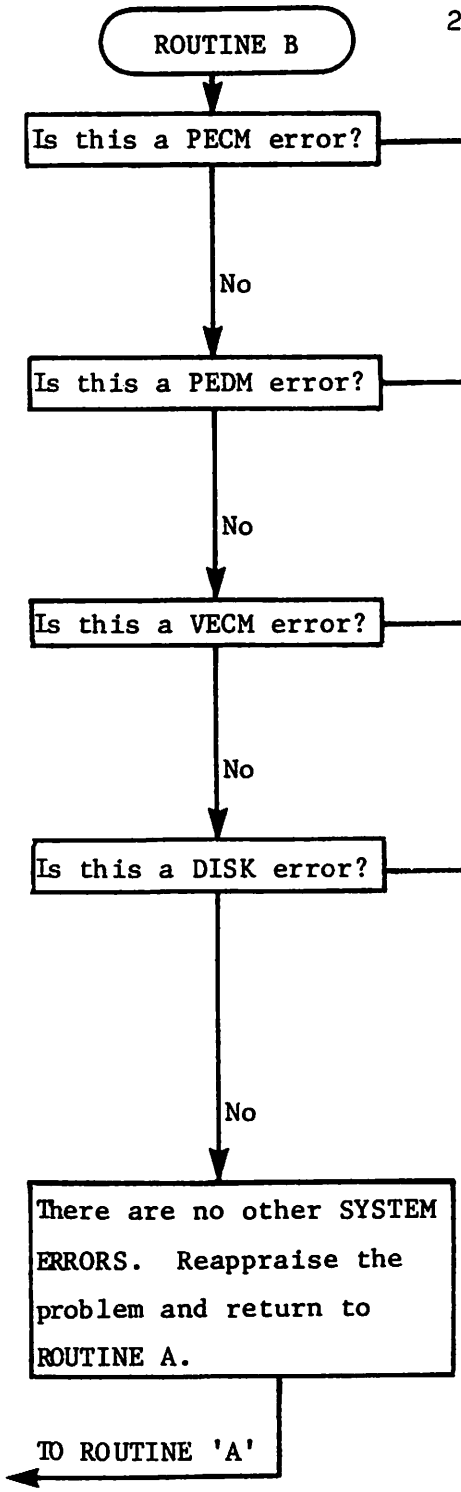
Because of the wide range of peripherals available to the 2200MVP System, it would be impractical to present here a full troubleshooting procedure for each. All available peripherals are fully documented in their own maintenance publications. The unit maintenance manual is generally the most helpful document for troubleshooting the peripheral. In addition, many peripherals have Module Repair Guides (MRGs) which give special procedures, test routines, and diagnostics to aid in repairing the individual PC boards in the units.

For a summary of these maintenance publications, see the 2200MVP System-Level Documentation list in the preface of this manual.

7.4.3 2200MVP TROUBLESHOOTING FLOWCHART

The 2200MVP Troubleshooting Flowchart, starting on the next page, presents a logical approach to troubleshooting the system.


ROUTINE A
For any SYSTEM ERROR message go directly to ROUTINE B.
Go to ROUTINE B
Does the system Power On (MOUNT SYSTEM PLATTER CR/LF PRESS RESET appear)?
No
Go to ROUTINE C
Yes
Does each file load and run when selected by the SF' key in response to the KEY SF' message?
No
Go to ROUTINE D
Yes
Does the BASIC-2 Diagnostic load and run?
No
Go to ROUTINE E
Yes
If problem does not fall into one of the above general conditions, then continue with step 2 (page 7-15)

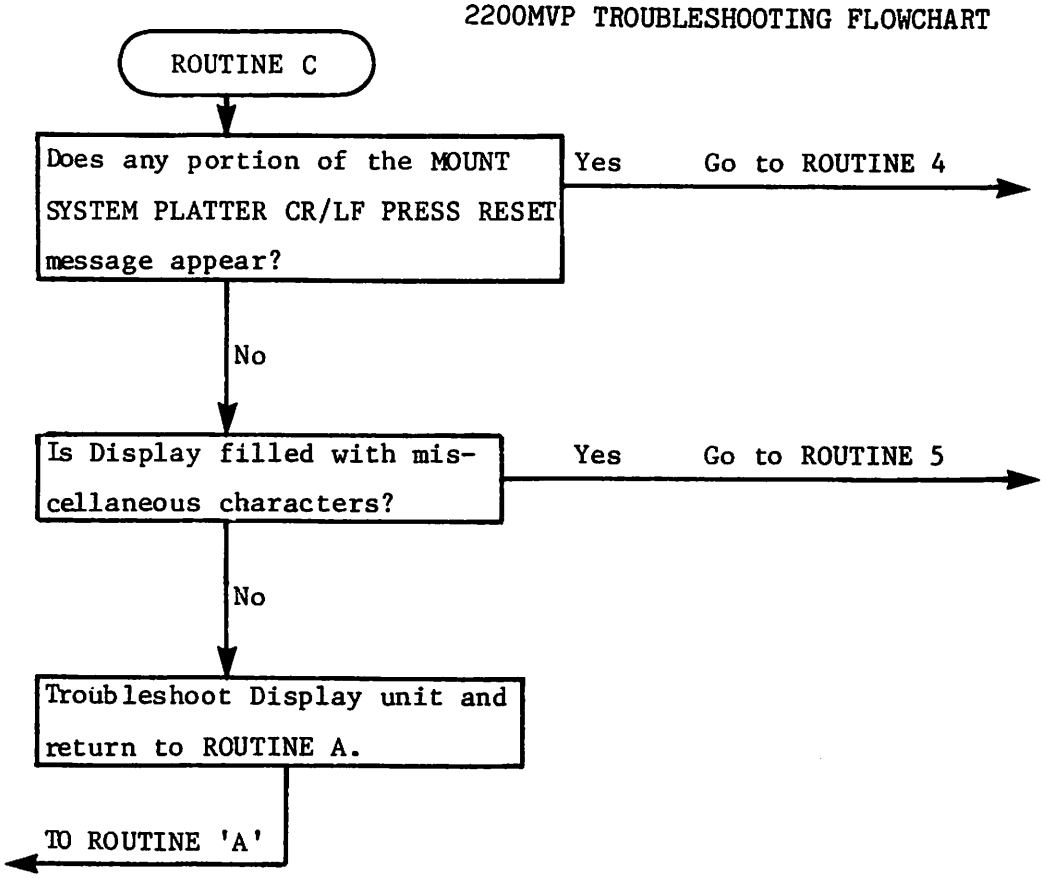


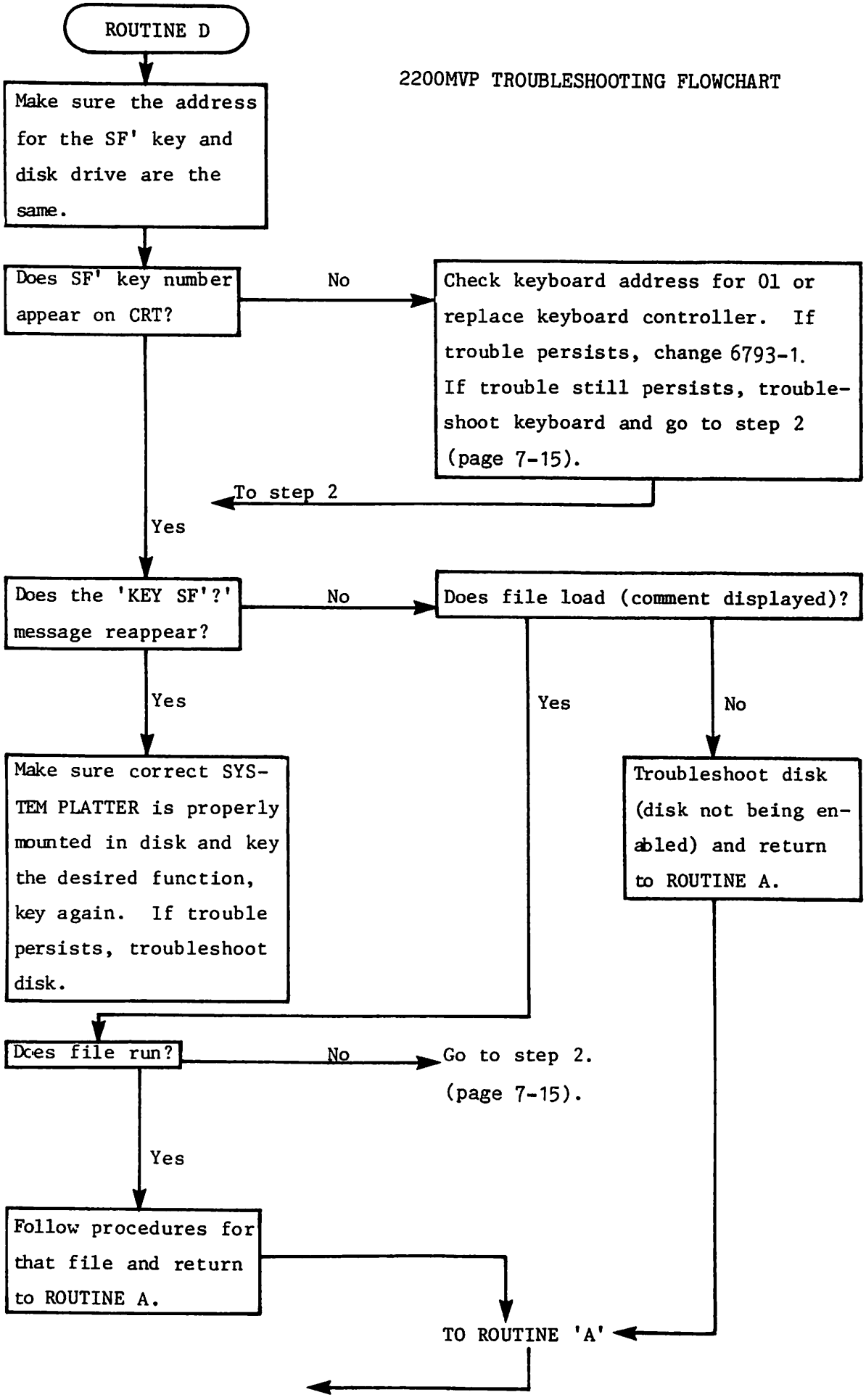
Note the failing location and go to ROUTINE 1.

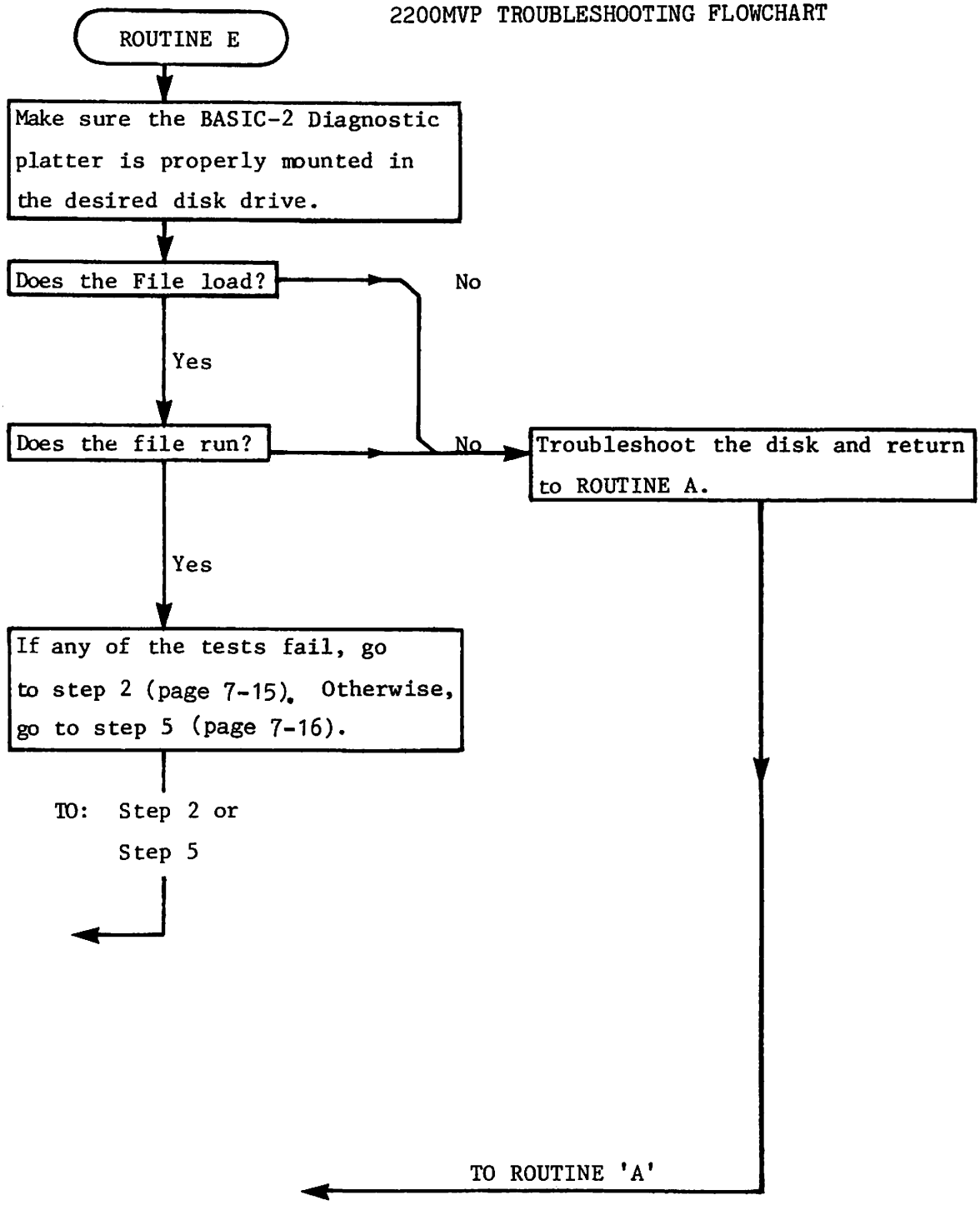
Note the failing location and go to ROUTINE 2.

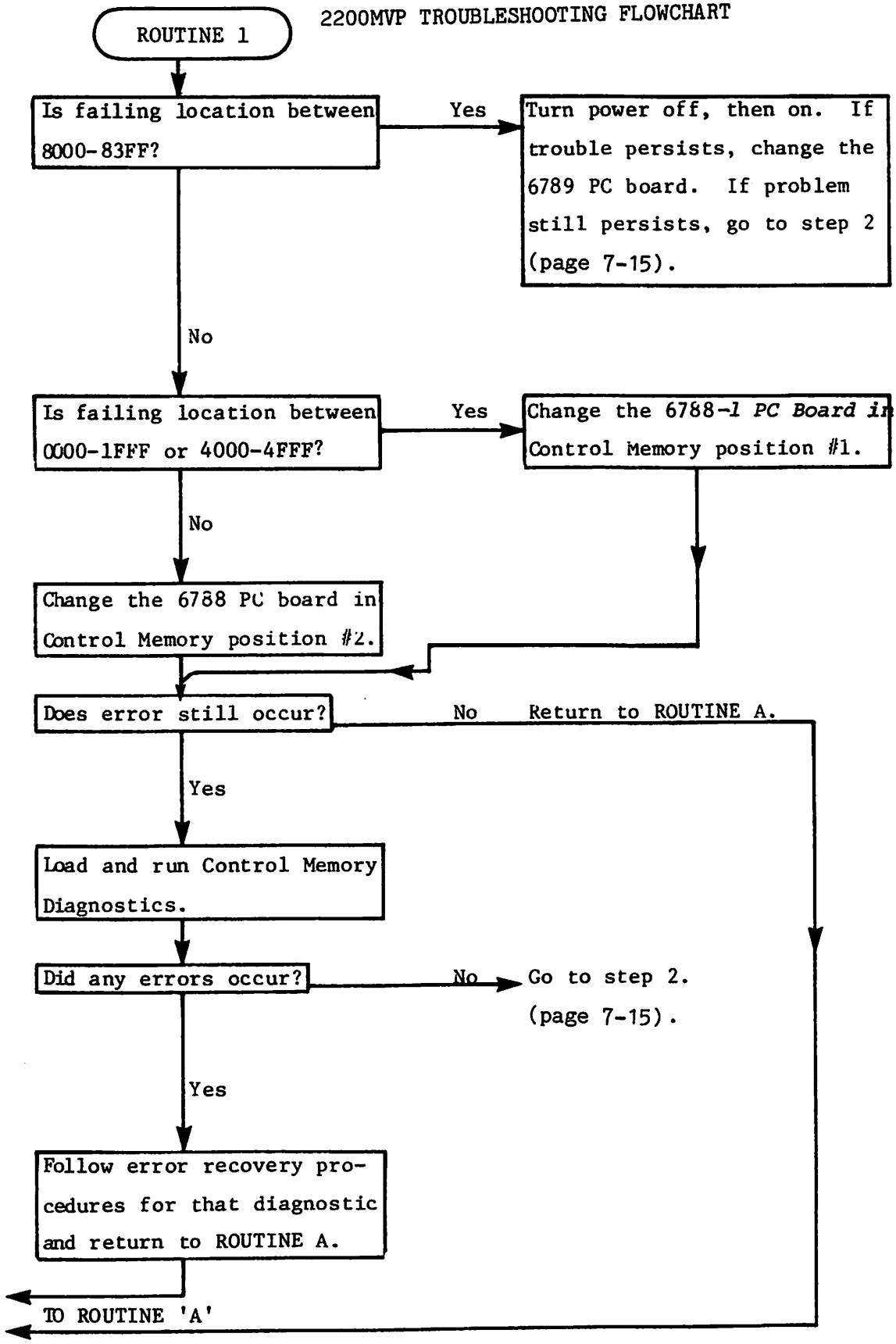
Note the failing location and go to ROUTINE 3.

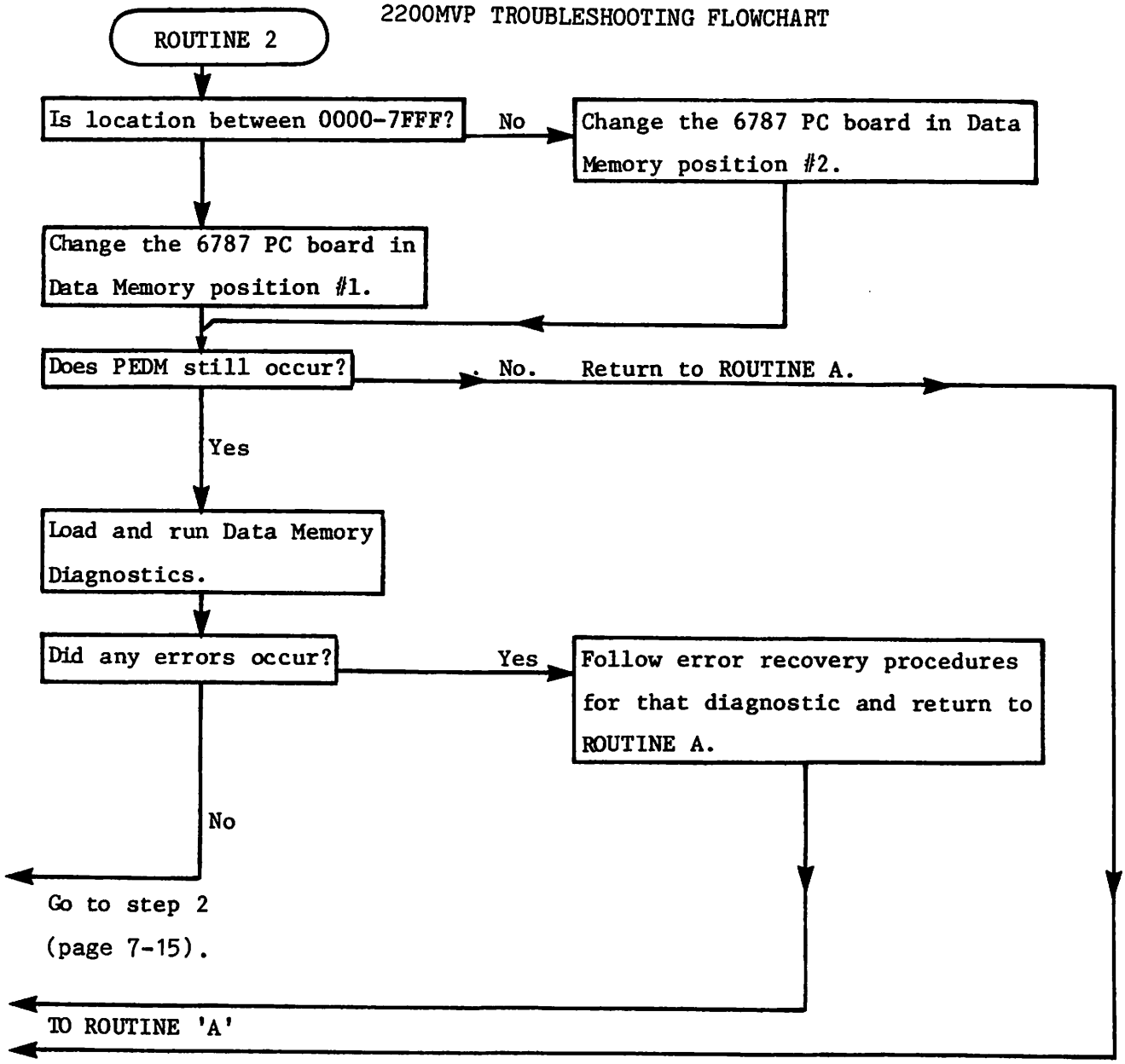
Note error number and follow the recovery procedures for that error. If error persists, go to step 2 (page 7-15).

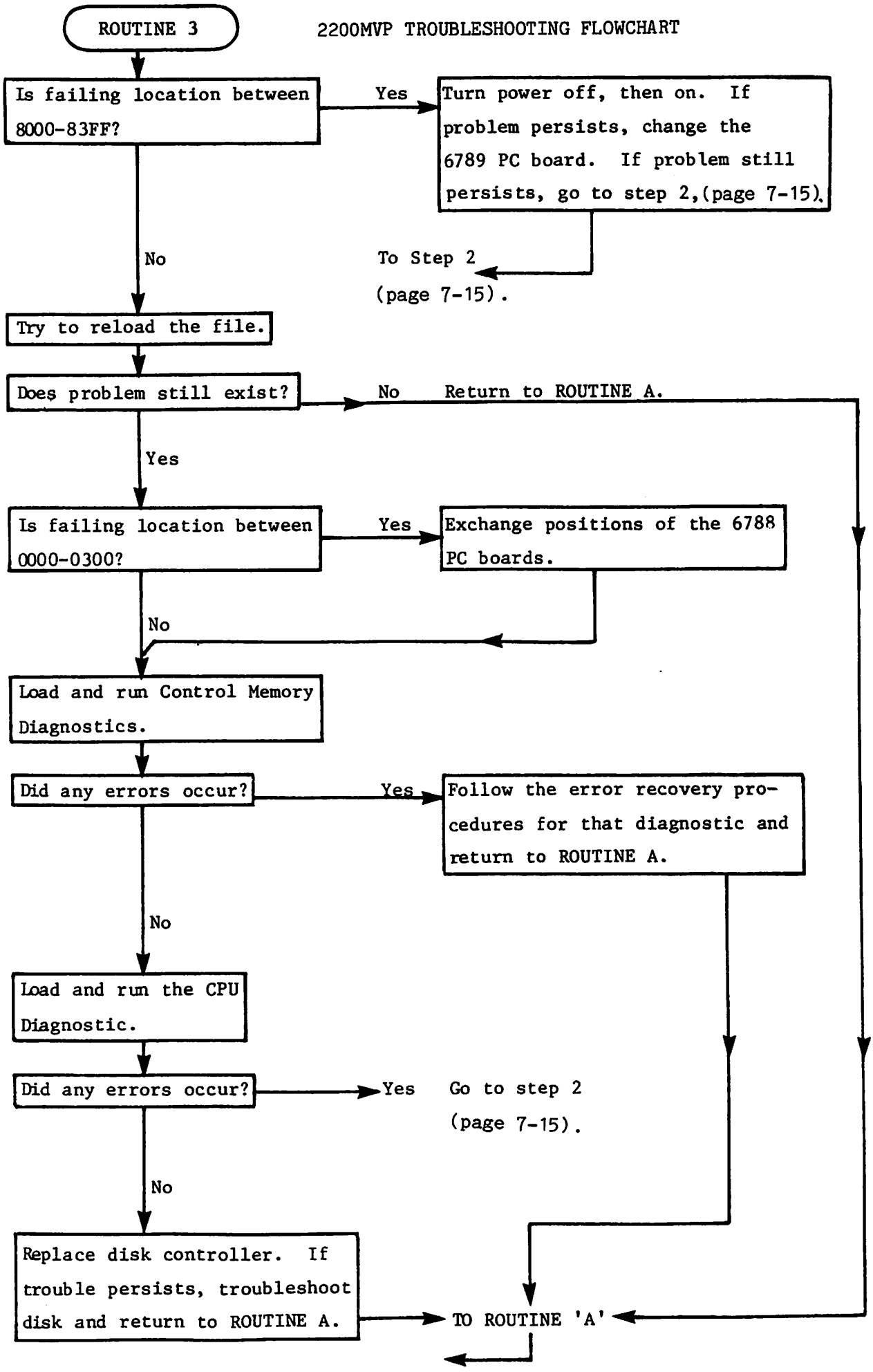

ROUTINE C
Does any portion of the MOUNT SYSTEM PLATTER CR/LF PRESS RESET message appear?
Yes
Go to ROUTINE 4
No
Is Display filled with miscellaneous characters?
Yes
Go to ROUTINE 5
No
Troubleshoot Display unit and return to ROUTINE A.
TO ROUTINE 'A'


ROUTINE D
Make sure the address for the SF' key and disk drive are the same.
Does SF' key number appear on CRT?
No
Check keyboard address for 01 or replace keyboard controller. If trouble persists, change 6793-1. If trouble still persists, troubleshoot keyboard and go to step 2 (page 7-15).
To step 2
Yes
Does the 'KEY SF'?' message reappear?
No
Does file load (comment displayed)?
Yes
Yes
No
Make sure correct SYSTEM PLATTER is properly mounted in disk and key the desired function, key again. If trouble persists, troubleshoot disk.
Troubleshoot disk (disk not being enabled) and return to ROUTINE A.
Does file run?
No
Go to step 2. (page 7-15).
Yes
Follow procedures for that file and return to ROUTINE A.
TO ROUTINE 'A'

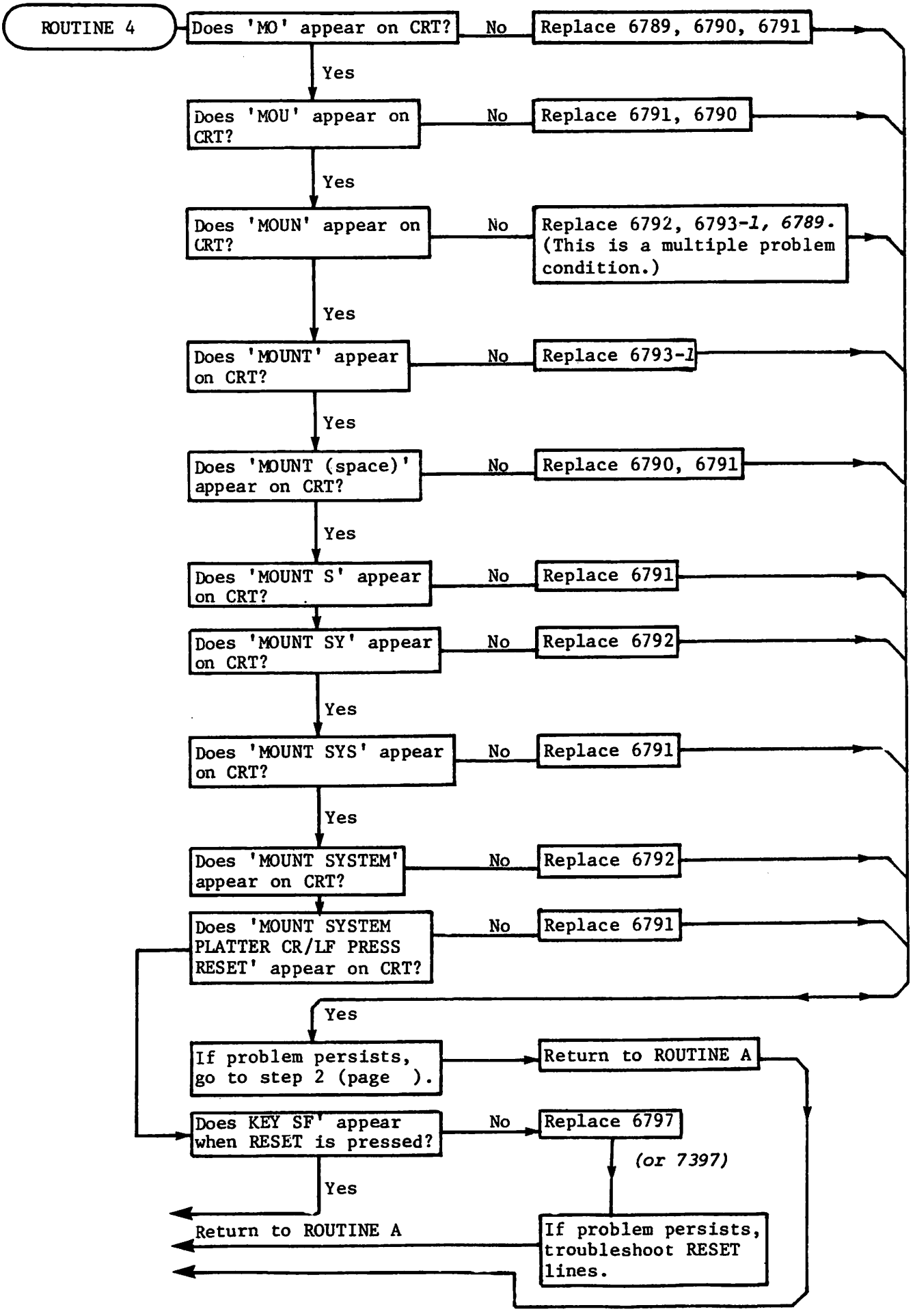

ROUTINE E
Make sure the BASIC-2 Diagnostic platter is properly mounted in the desired disk drive.
Does the File load?
No
Yes
Does the file run?
No
Troubleshoot the disk and return to ROUTINE A.
Yes
If any of the tests fail, go to step 2 (page 7-15). Otherwise, go to step 5 (page 7-16).
TO: Step 2 or
Step 5
TO ROUTINE 'A'

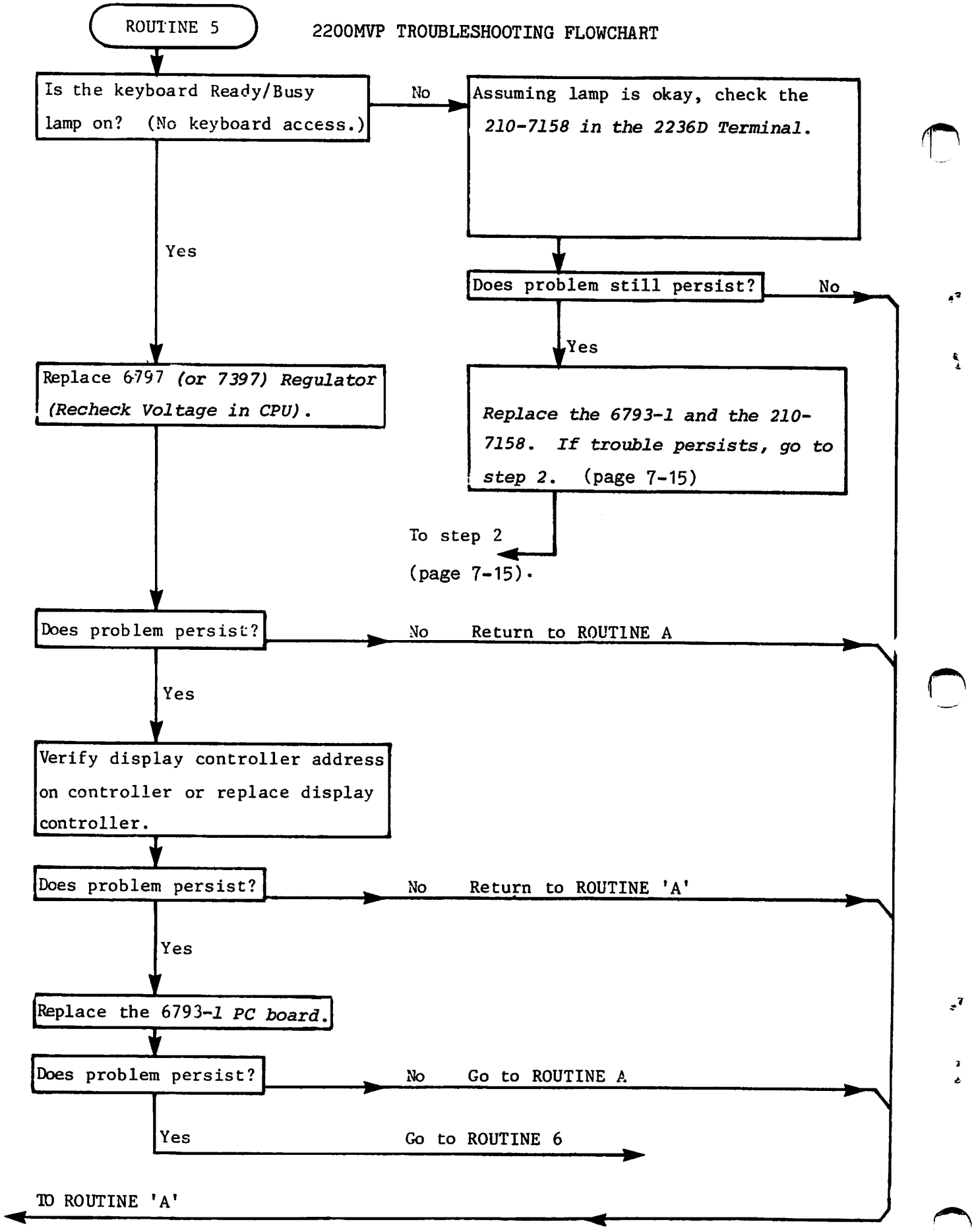

2200MVP TROUBLESHOOTING FLOWCHART
ROUTINE 1
Is failing location between 8000-83FF?
Yes
Turn power off, then on. If trouble persists, change the 6789 PC board. If problem still persists, go to step 2 (page 7-15).
No
Is failing location between 0000-1FFF or 4000-4FFF?
Yes
Change the 6788-1 PC Board in Control Memory position #1.
No
Change the 6788 PC board in Control Memory position #2.
Does error still occur?
No
Return to ROUTINE A.
Yes
Load and run Control Memory Diagnostics.
Did any errors occur?
No
Go to step 2. (page 7-15).
Yes
Follow error recovery procedures for that diagnostic and return to ROUTINE A.
TO ROUTINE 'A'

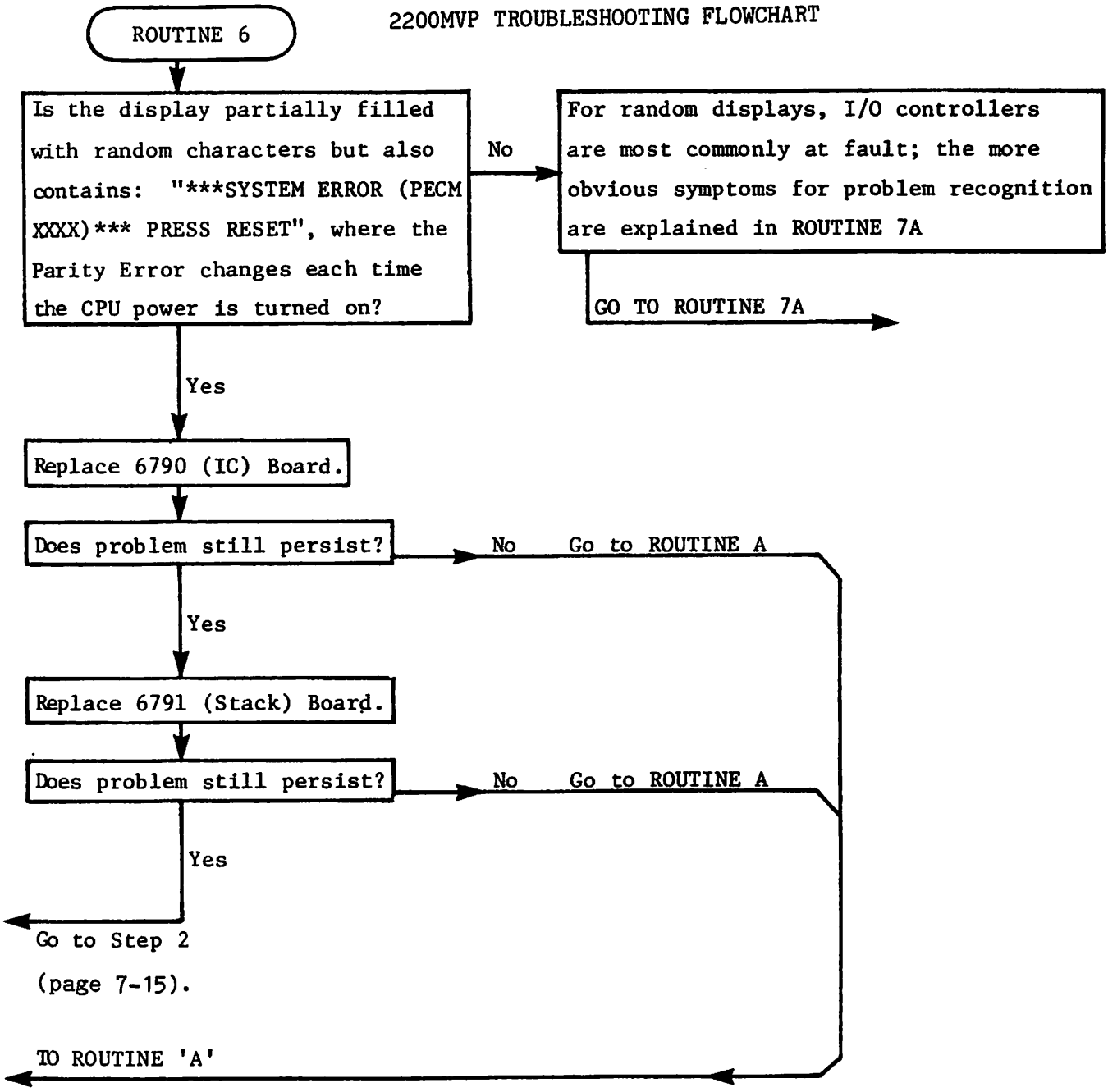

ROUTINE 2
Is location between 0000-7FFF?
No
Change the 6787 PC board in Data Memory position #2.
Change the 6787 PC board in Data Memory position #1.
Does PEDM still occur?
No. Return to ROUTINE A.
Yes
Load and run Data Memory Diagnostics.
Did any errors occur?
Yes
Follow error recovery procedures for that diagnostic and return to ROUTINE A.
No
Go to step 2 (page 7-15).
TO ROUTINE 'A'

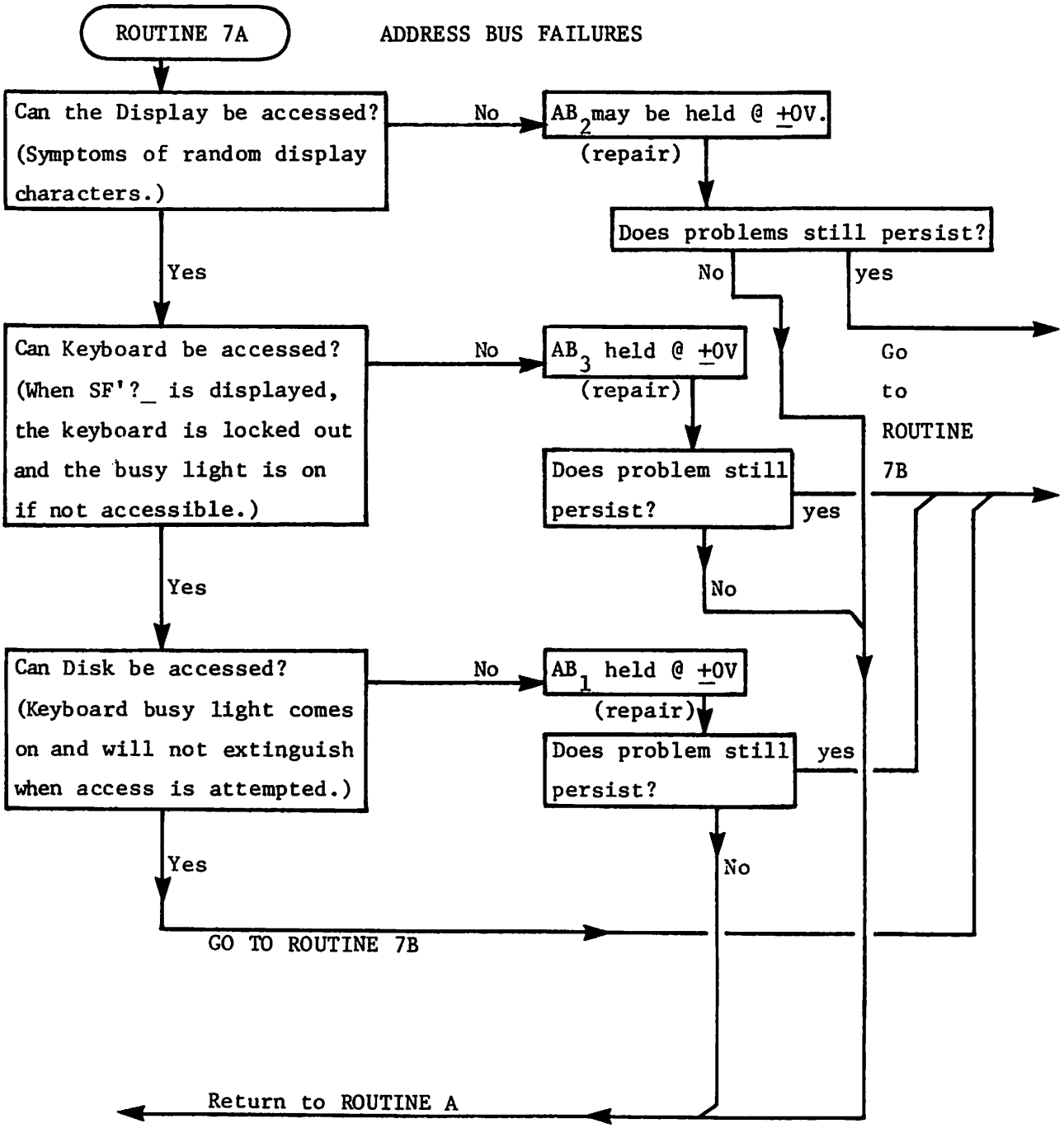

ROUTINE 3
2200MVP TROUBLESHOOTING FLOWCHART
Is failing location between 8000-83FF?
Yes
Turn power off, then on. If problem persists, change the 6789 PC board. If problem still persists, go to step 2,(page 7-15).
No
To Step 2 (page 7-15).
Try to reload the file.
Does problem still exist?
No
Return to ROUTINE A.
Yes
Is failing location between 0000-0300?
Yes
Exchange positions of the 6788 PC boards.
No
Load and run Control Memory Diagnostics.
Did any errors occur?
Yes
Follow the error recovery procedures for that diagnostic and return to ROUTINE A.
No
Load and run the CPU Diagnostic.
Did any errors occur?
Yes
Go to step 2 (page 7-15).
No
Replace disk controller. If trouble persists, troubleshoot disk and return to ROUTINE A.
TO ROUTINE 'A'

2200MVP TROUBLESHOOTING FLOWCHART

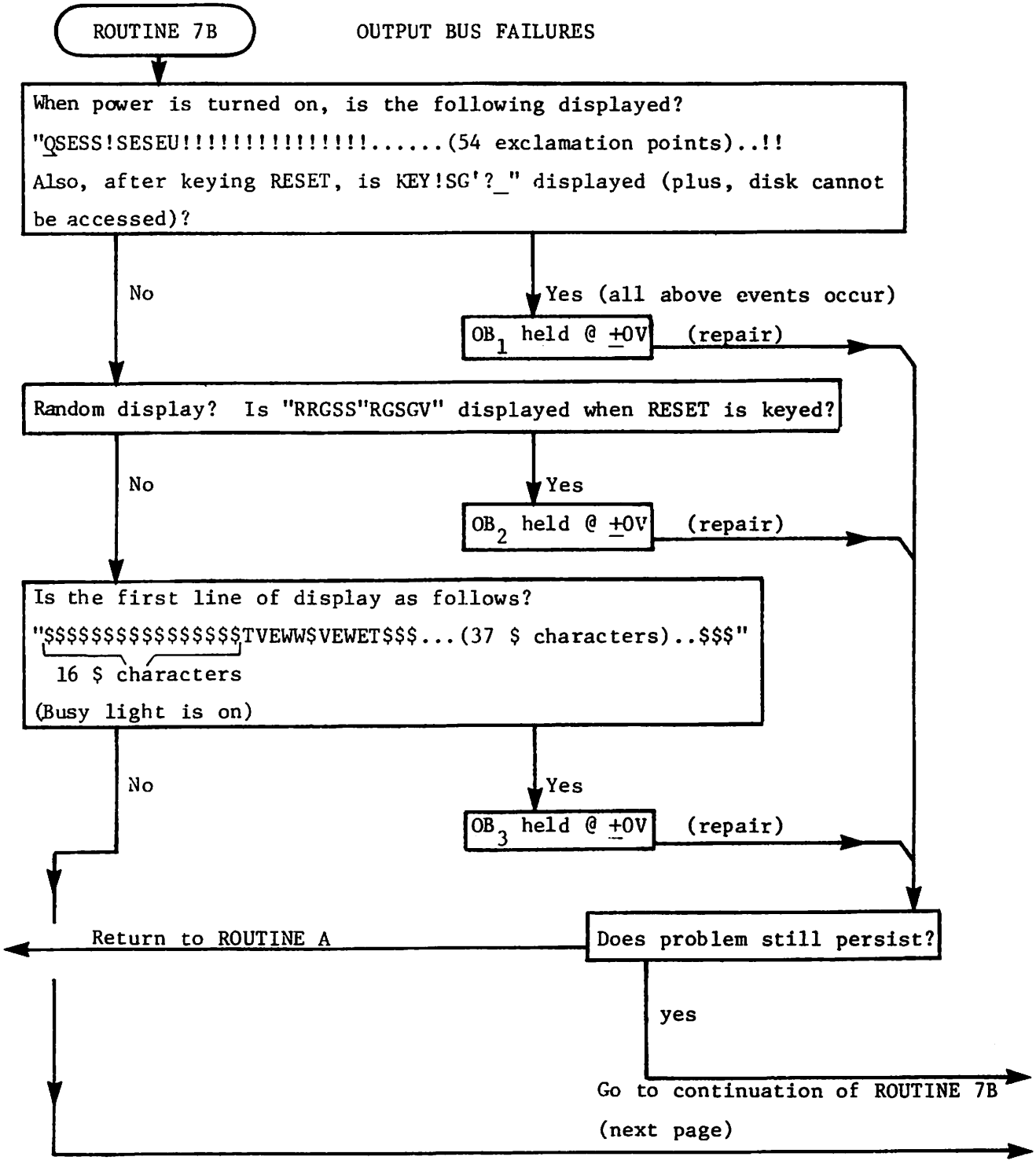



ROUTINE 5
2200MVP TROUBLESHOOTING FLOWCHART
Is the keyboard Ready/Busy lamp on? (No keyboard access.)
No
Assuming lamp is okay, check the 210-7158 in the 2236D Terminal.
Yes
Does problem still persist?
No
Yes
Replace 6797 (or 7397) Regulator (Recheck Voltage in CPU).
Replace the 6793-1 and the 210-7158. If trouble persists, go to step 2. (page 7-15)
To step 2 (page 7-15).
Does problem persist?
No
Return to ROUTINE A
Yes
Verify display controller address on controller or replace display controller.
Does problem persist?
No
Return to ROUTINE 'A'
Yes
Replace the 6793-1 PC board.
Does problem persist?
No
Go to ROUTINE A
Yes
Go to ROUTINE 6
TO ROUTINE 'A'

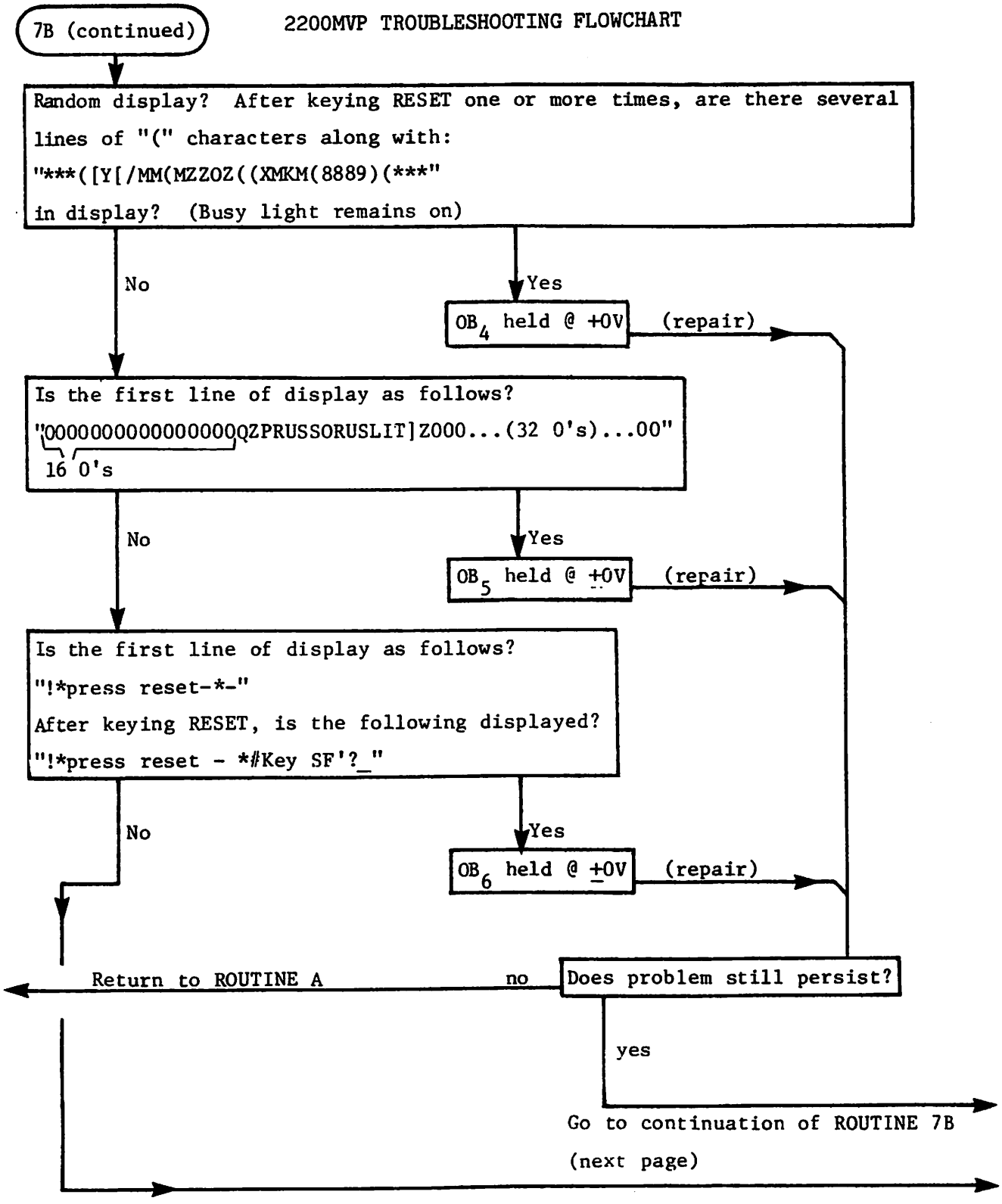

ROUTINE 6
Is the display partially filled with random characters but also contains: "***SYSTEM ERROR (PECM XXXX)*** PRESS RESET", where the Parity Error changes each time the CPU power is turned on?
No
For random displays, I/O controllers are most commonly at fault; the more obvious symptoms for problem recognition are explained in ROUTINE 7A
GO TO ROUTINE 7A
Yes
Replace 6790 (IC) Board.
Does problem still persist?
No Go to ROUTINE A
Yes
Replace 6791 (Stack) Board.
Does problem still persist?
No Go to ROUTINE A
Yes
Go to Step 2
(page 7-15).
TO ROUTINE 'A'

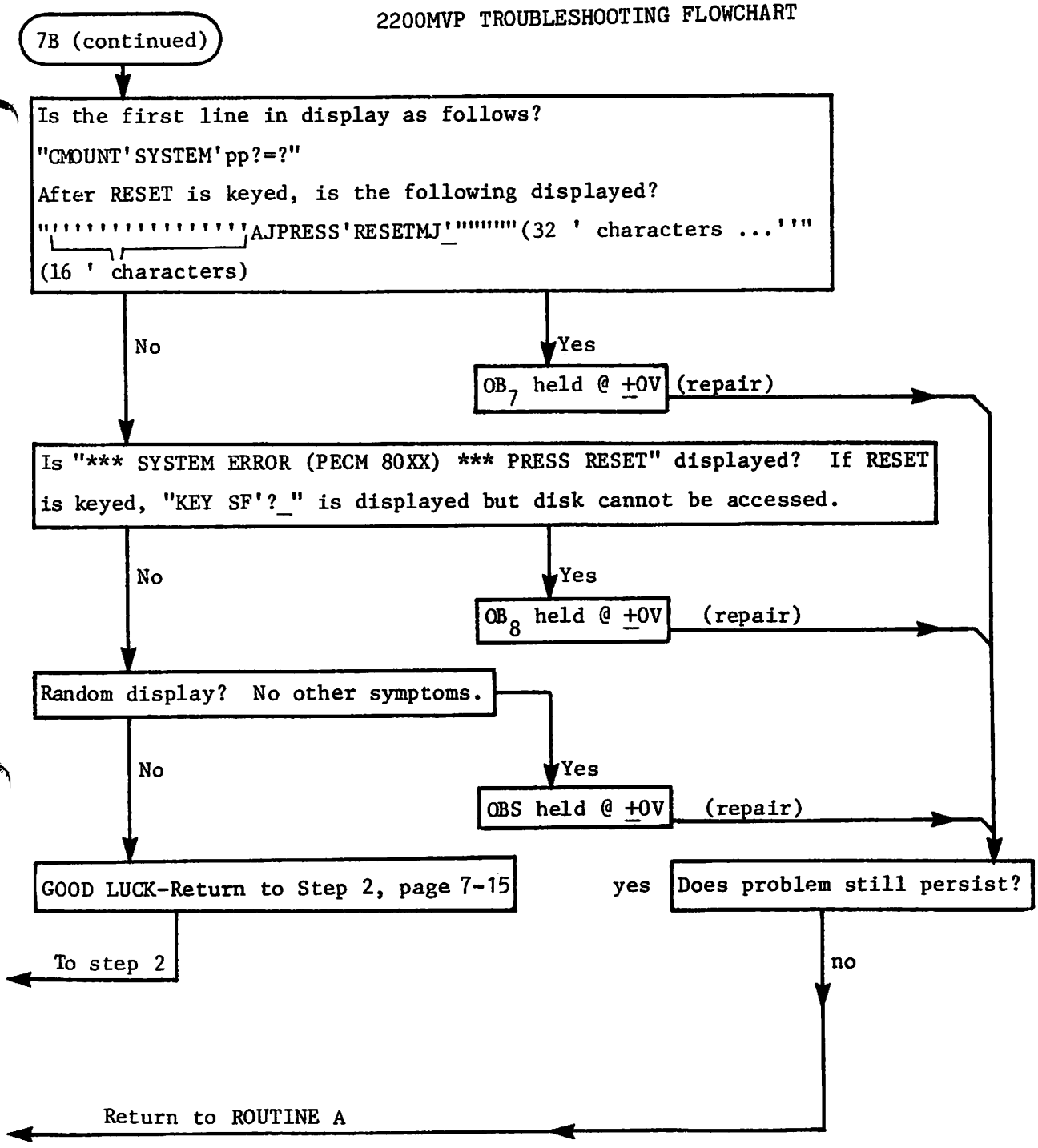


2200MVP TROUBLESHOOTING FLOWCHART



2200MVP TROUBLESHOOTING FLOWCHART


7B (continued)
Random display? After keying RESET one or more times, are there several lines of "(" characters along with:
"***([Y[/MM(MZZOZ((XMKM(8889)(***"
in display? (Busy light remains on)
No
Yes
OB4 held @ +0V
(repair)
Is the first line of display as follows?
"0000000000000000QZPRUSSORUSLIT]Z000...(32 0's)...00"
16 0's
No
Yes
OB5 held @ +0V
(repair)
Is the first line of display as follows?
"!*press reset-*-"
After keying RESET, is the following displayed?
"!*press reset - *#Key SF'?_"
No
Yes
OB6 held @ +0V
(repair)
Return to ROUTINE A
no
Does problem still persist?
yes
Go to continuation of ROUTINE 7B
(next page)


7B (continued)
Is the first line in display as follows?
"CMOUNT'SYSTEM'pp?=?"
After RESET is keyed, is the following displayed?
"'''''''''''''''AJPRESS'RESETMJ'""""""(32 ' characters ...'""
(16 ' characters)
No
Yes
OB7 held @ ±0V (repair)
Is "*** SYSTEM ERROR (PECM 80XX) *** PRESS RESET" displayed? If RESET is keyed, "KEY SF'?_" is displayed but disk cannot be accessed.
No
Yes
OB8 held @ ±0V (repair)
Random display? No other symptoms.
No
Yes
OBS held @ ±0V (repair)
GOOD LUCK-Return to Step 2, page 7-15
yes
Does problem still persist?
To step 2
no
Return to ROUTINE A

NOTES:

SECTION 8
UPGRADES/CONVERSIONS

8.1 VP TO MVP CONVERSIONS

8.1.1 CENTRAL PROCESSING UNIT

a) Replace 6793 board with 6793-1.
b) Replace 6788A #1 board with 6788-1A.
c) Install 2236MXD controller (address set to '00').

8.1.2 2270 TO 2270A-D CONVERSION

a) Remove the 210-7018A Disk Microprocessor.
b) Modify the 220-3011 Disk Cable and 220-0066-3 cable as described in Appendix A of Service Bulletin 82 (if necessary). Be sure pin 11 of the 220-0066-4 cable is NOT connected to the fingerboard.
c) Install the 210-7218C Disk Microprocessor, being sure to reconnect all cables.
d) Adjust the power supply regulators and phase-locked loop.

8.1.3 2270A TO 2270A-D CONVERSION

ECN 9617:

a) Remove PROMS L91 and L92.
b) Insert PROM 378-2256 in L92.
c) Insert PROM 378-2257 in L91.

8.1.4 2236 TO 2236D CONVERSION

a) Remove 210-7292A CPU.
b) Insert 210-7292-1A CPU.

8.1.5 2236MXC TO 2236MXD CONVERSION

a) Remove 177-2236-1 MXC Controller.
b) Replace with 177-3236-1 MXD Controller.

8.2 MVP to MVP-A CONVERSION

When system upgrades are made by adding more peripherals and controllers, it may also be necessary to upgrade the standard MVP to an MVP-A to accommodate the extra current demand; the MVP-A makes 20 amps available to the I/O. Use the guidelines set forth in section 3.6 to determine the need for an MVP-A conversion.

a) Exchange the MVP chassis for an MVP-A chassis, WL# 270-0451 (50Hz) or WL# 270-0452 (60 Hz).
b) Replace the standard 210-6797 regulator with a 210-7397 regulator.
c) A conversion kit (WL# 200-0322) is available containing the MVP-A chassis and the 210-7397 regulator.

8.3 2200MVP EXPANDED MEMORY

The 2200MVP is now available with an expanded data memory capability. This provision for greater memory (up to 256K) is made possible by the use of 16K RAMS (377-0345) in a new 210-7587 PCB. To accomodate the memory increase the Bootstrap PROMS, Operating System, diagnostics, and system hardware have to be changed. An explanation of these changes follows.

8.3.1 BOOSTSTRAP PROMS

2200 VP/MVP Bootstrap Release 2.2 has been incorporated by ECN #9772. For a system to operate with an expanded memory, this ECN must be performed. The old PROMS on the 210-6789 must be replaced with the following:

378-2045R1 = L27
378-2046R1 = L28
378-2047R1 = L29

NOTE:
The 2270A diskette drive must have ECN #9617 installed (new PROMS 378-2256, 378-2257).

8.3.2 OPERATING SYSTEM

The MVP Operating System must be at revision 5 or higher (WL# 701-2294E).

8.3.3 DIAGNOSTICS

The system diagnostics contained on the Operating System diskette, which are essentially the same as the older diagnostics, have the added capability to test systems with expanded memory.

8.3.4 HARDWARE CHANGE

To allow for the use of the 210-7587 and the 16K RAMS in existing MVP systems, the following hardware change must be made.

NOTE:

Because all changes are downward compatible (the current VP/MVP will work with them), all PC boards should be modified to facilitate their replacement. The 6798 motherboard needs to be updated only if a 7587 memory board is to be installed in the unit.

210-6790 [5]

1. Change C4 to .0033 uf (300-1909). C4 is located on the schematic at coordinates I3.

2. Add a wire from L51 pin 7 to connector X_3.

3. Add a wire from L51 pin 9 to connector 20_3.

4. Cut the etch between L18A pin 9 and connector 12_2.

5. Add a wire from L49 pin 9 to connector 12_2.

6. Add a wire from L49 pin 10 to L28 pin 6.

7. Add a wire from L49 pin 11 to L39 pin 8.

8. Change the E-REV level from 4 to 5.

210-6791 [3]

1. Insert a 7427 (376-0125) into location L21A. Pin 1 should be located toward the bottom of the board. Connect pin 7 to ±0V and pin 14 to +5V.

2. Cut the etch connected to L53 pin 2 at pin 2.

3. Add a wire from L32 pin 13 to L53 pin 2.

4. Add a wire from L32 pin 12 to connector H_2.

5. Add a wire from L32 pin 12 to L21A pin 12.

6. Jumper L21A pins 3 and 13 together.

7. Add a wire from L32 pin 11 to L21A pin 6.

8. Add a wire from L21A pin 1 to L41 pin 2.

9. Add a wire from L21A pin 2 to L41 pin 6.

10. Add a wire from L21A pin 13 to L41 pin 7.

11. Add a wire from L21A pin 4 to L22 pin 4.

12. Add a wire from L21A pin 5 to L22 pin 6.

13. Add a wire from L22 pin 3 to connector 8_2.

14. Add a wire from L22 pin 5 to connector 1_3.

15. Add a 2.2K resistor (330-3022-4B) between L22 pin 3 and +5V.

16. Add a 2.2K resistor between L22 pin 5 and +5V.

17. Change the E REV level from 2 to 3.

210-6793-1 [2]

1. Add a wire from L39 pin 3 to L35 pin 10.

2. Add a wire from L39 pin 4 to connector R_3.

3. Add a wire from L39 pin 5 to L35 pin 6.

4. Add a wire from L39 pin 6 to connector H_3.

5. Change the E-REV level from 1 to 2.

210-6798 [3]

For access to the motherboard, remove the bottom access panel by removing the feet on the underside of unit. All modifications described below can be performed without removing the motherboard from the chassis. See Figure 1-8 for the location of PC boards in the CPU chassis.

1. Add a wire from 6793-H_3 to 6791-8_2 to 6787 (DM1) - M_2 to 6787 (DM2)-M_2.

2. Add a wire from 6793-R_3 to 6791-1_3 to 6787 (DM1)-N_2 to 6787 (DM2)-N_2.

3. Add a wire from 6791-H_2 to 6787 (DM1)-L_2 to 6787 (DM2)-L_2.

4. Add a wire from 6790-20_3 to 6788 (CM1)-N_2.

5. Add a wire from 6790-X_3 to 6788 (CM1)-R_2.

6. Add a wire from 6788 (CM1)-E_2 to 6788 (CM2)-E_2.

7. Add a wire from 6790-12_2 to 6787 (DM1)-J_2 to 6787 (DM2)-J_2.

8. Add a wire from 6788 (CM2)-2_3 to 6787 (DM1)-K_2 to 6787 (DM2)-K_2.

9. Add a wire from 6787 (DM1)-14_2 to 6787 (DM2)-R_2.

10. Add a wire from 6787 (DM1)-S_2 to $\pm$0V.

11. Add a wire from 6790-C_2 to 6788 (CM1)-S_2.

12. Add a wire from 6790-17_2 to 6788 (CM1)-16_2.

13. Add a wire from 6790-16_2 to 6788 (CM1)-15_2.

14. Change the E-REV level from 2 to 3.

8.3.5 CONVERSION KITS

The conversion kit contains only the data memory boards necessary for the upgrade. The customer chassis must be upgraded, and updated CPU boards (6790, 6791 and 6793-1) must be installed. It is recommended that only the customer chassis be updated at the customer site. The CPU boards should be updated and checked with the additional memory prior to the installation. Upon installation, swap the CPU boards and bring the non-updated boards back to the CE office for updating. After updating they can be used for the next conversion.

NOTES:

NOTES:

APPENDIX A

2236D CHARACTER SET

CONTROL CODES					
HEX	ACTION	HEX	ACTION	HEX	
00	NULL	06	CURSOR OFF	0A	CURSOR↓
01	HOME CURSOR	07	AUDIBLE TONE	0C	CURSOR↑
03	CLEAR SCREEN, HOME CURSOR	08	BACKSPACE	0D	CARRIAGE RETURN
05	CURSOR ON	09	NON-DESTRUCTIVE SPACE		

CHARACTERS							
HEX	CHAR	HEX	CHAR	HEX	CHAR	HEX	CHAR
10	â	30	0	50	P	70	p
11	ê	31	1	51	Q	71	q
12	î	32	2	52	R	72	r
13	ô	33	3	53	S	73	s
14	û	34	4	54	T	74	t
15	ä	35	5	55	U	75	u
16	ë	36	6	56	V	76	v
17	ï	37	7	57	W	77	w
18	ö	38	8	58	X	78	x
19	ü	39	9	59	Y	79	y
1A	à	3A		5A	Z	7A	z
1B	è	3B	;	5B	[	7B	¢
1C	ù	3C	<	5C	\	7C	£
1D	Ä	3D	=	5D	]	7D	¤
1E	Ö	3E	>	5E	^	7E	¥
1F	Ü	3F	?	5F	_	7F	₧
20	SPACE	40	@	60	`	80	NULL
21	!	41	A	61	a	81	♦
22	"	42	B	62	b	82	▶
23	#	43	C	63	c	83	◀
24	$	44	D	64	d	84	°
25	%	45	E	65	e	85	±
26	&	46	F	66	f	86	²
27	'	47	G	67	g	87	³
28	(	48	H	68	h	88	´
29	)	49	I	69	i	89	¹
2A	*	4A	J	6A	j	8A	^
2B	+	4B	K	6B	k	8B	■
2C	,	4C	L	6C	l	8C	¼
2D	-	4D	M	6D	m	8D	½
2E	.	4E	N	6E	n	8E	¸
2F	/	4F	O	6F	o	8F	¶

APPENDIX B

2200MVP ERROR CODES

Error Code: NONRECOVERABLE ERRORS

Misc. Errors:

A01	memory exceeded (overlap: text & symbol table)
A02	memory exceeded (overlap: text & value stack)
A03	not enough memory (LISTDC, MOVE, COPY)
A04	stack overflow (operator stack)
A05	line too long
A06	program protected
A07	illegal immediate mode statement
A08	statement not legal here
A09	program not resolved

Syntax Errors:

S10	missing left parenthesis
S11	missing right parenthesis
S12	missing equal sign
S13	missing comma
S14	missing asterisk
S15	missing angle brackets
S16	missing letter
S17	missing hex digit
S18	missing relation operator
S19	missing required word
S20	expected end of statement
S21	missing line number
S22	illegal PLOT argument
S23	missing literal string
S24	illegal expression or missing variable
S25	missing numeric scalar variable
S26	missing array variable
S27	missing numeric array
S28	missing alpha array
S29	missing alpha variable

Program Errors:

P32	starting address greater than ending address
P33	line number conflict
P34	illegal value
P35	no program
P36	underfined line number or CONTINUE illegal
P37	underfined special function subroutine
P38	underfined FN function
P39	FN nested too deep
P40	NEXT without FOR
P41	RETURN without GOSUB

P42	illegal image
P43	illegal matrix operand
P44	matrix not square
P45	operand dimensions not compatible
P46	illegal microcommand
P47	missing buffer variable
P48	illegal device specification
P49	interrupt table full
P50	illegal dimensions or variable length
P51	variable or value too short
P52	variable or value too long
P53	noncommon variables already defined
P54	common variable required
P55	undefined array
P56	illegal subscripts
P57	illegal STR () arguments
P58	illegal field/delimiter specification
P59	illegal redimension

Error Code: RECOVERABLE ERRORS

Computation Errors:

C60	underflow
C61	overflow
C62	division by zero
C63	zero divided by zero, or zero raised to zero power
C64	zero raised to negative power
C65	negative number raised to noninteger power
C66	SQR of negative power
C67	LOG of zero
C68	LOG of negative power
C69	argument too large

Execution Errors:

X70	insufficient data
X71	value exceeds format
X72	singular matrix
X73	illegal INPUT data
X74	wrong variable type
X75	illegal number
X77	invalid partition reference

Disk Errors:

D80	file not open
D81	file full
D82	file not in catalog
D83	file already catalogued
D84	file not scratched
D85	index full
D86	catalog end error
D87	no end file
D88	wrong record type
D89	sector address beyond EOF

I/O Errors:

I90	disk hardware error (X'C0' not rec'd)
I91	disk hardware error
I92	disk hardware error (timeout)
I93	disk format error
I94	format key engaged
I95	seek error
I96	CRC error
I97	LRC error
I98	illegal sector address
I99	read-after-write error

APPENDIX C

CPU MOTHERBOARD (6798)

MNEMONICS

AB1-AB8	I/O Address Bus Lines $_{1-8}$
A Bus Ø-7	'A' Bus Lines $_{0-7}$
ABS	Address Bus Strobe
ALU CLK	'C' Bus Latch Clock
B	Unconditional Branch
B Bus Ø-7	'B' Bus Lines $_{0-7}$
BLK-CA	Block Carry
BRANCH	Conditional Branch
CØ-7	ALU Output Lines to 'C' Bus
CA	Carry Borrow Bit
CA Ø-11	Control Memory Address Lines $_{0-11}$
C Bus Ø-7	'C' Bus Lines $_{0-7}$
CBS	Control Bus Strobe
$CDI_{Ø-23}$	Control Memory Data Input Lines $_{0-23}$
$CDO_{Ø-23}$	Control Memory Data Output Lines $_{0-23}$
CE	Chip Enable
CEN	Carry Enable
CIO	Control Input/Output
CNTD	Count Down PC's
CPB	Central Processor Busy
DI Ø-17	Data Memory Data Input Lines $_{Ø-17}$
DIP	Data Memory Input Parity (DI 8 & 17)
DMPI	Data Memory Parity Inhibit
$DMS_{1,2}$	Data Memory Select
$DO_{Ø-17}$	Data Memory Output Lines $_{Ø-17}$
HALT	HALT/STEP Input
IB 1-9	I/O Input Bus Lines
IBS	Input Bus Strobe
ICC Ø-15	Instruction Counter Bits
I/O CLK	I/O Clock to I/O Controllers
LHPC	Load High Order PC
LLPC	Load Low Order PC

LOP	Long Operation
LPI	Load PC's Immediate
MARCLK	Memory Address Refresh Clock
MS_{1-6}	Control Memory Select $_{1-6}$
OB_{1-8}	I/O Output Bus Lines $_{1-8}$
OBS	Ouput Bus Strobe
PARITY OFF	Simulator Function
PCCC	PC Counter Clock
PECM	Parity Error Control Memory
PEDM	Parity Error Data Memory
PH Ø-7	PH Register Bits $_{Ø-7}$
PINC	PC Increment
PL Ø-7	PL Register Bits $_{Ø-7}$
POR	Power-ON Reset
PRMS	Calculator Prime
R Ø-22	Instruction Bits $_{Ø-22}$
$RA_{Ø-5}$	Data Memory Refresh Address $_{Ø-5}$
R/B	I/O Ready/Busy
REF	Refresh
REFCLK	Refresh Clock
RESET	Hardware Trap to 8001_{16}
ROMS	Enable BOOTSTRAP PROMs
R/W_1	Read/Write Data Memory Bits Ø-8
R/W_2	Read/Write Data Memory Bits 9-17
R/W CM	Control Memory Read/Write
SØ-S7	Stack Bits $_{Ø-7}$
SB	Subroutine Branch
SHØ	Carry Flag
SR	Subroutine Return
STOP	Simulator Function
SWITCHES	Simulator Function
$T_{Ø-16}$	System Timing Clocks $_{Ø-16}$
TAP	Transfer Auxiliary to PC's
TCMDR	Control Memory Data Read
TSP	Transfer Stack to PC's
WPB	Simulator Function
XOP	Extended Operation
XPA	Exchange PC's and Auxiliary

APPENDIX D

2200MVP SIGNAL RUN LIST

Signal	Source DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
$\overline{AB_1}$	REG						D_1		D_1
$\overline{AB_2}$	REG						4_1		5_1
$\overline{AB_3}$	REG						6_1		6_1
$\overline{AB_4}$	REG						E_1		E_1
$\overline{AB_5}$	REG						7_1		F_1
$\overline{AB_6}$	REG						T_3		6_3
$\overline{AB_7}$	REG						16_3		7_3
$\overline{AB_8}$	REG						17_3		8_3
A Bus Ø	REG		S_2			Y_2	B_3		
A Bus 1	REG		14_2			20_2	3_3		
A Bus 2	REG		R_2			X_2	A_3		
A Bus 3	REG		13_2			B_3	2_3		
A Bus 4	REG		P_2			18_2	Z_2		
A Bus 5	REG		M_2			17_2	20_2		
A Bus 6	REG		K_2			U_2	U_2		
A Bus 7	REG		14_1			6_2	D_2		
$\overline{ABS}$	REG						8_1		J_1
ALUCLK	ALU					W_2	W_2		
$\overline{B}$	ST			V_2	U_2				
B Bus Ø			Z_2			L_3	10_3		
B Bus 1			21_2			K_3	K_3		
B Bus 2			20_2			9_3	9_3		
B Bus 3			18_2			J_3	J_3		
B Bus 4			V_2			8_3	8_3		
B Bus 5			U_2			7_3	7_3		
B Bus 6			16_2			5_3	D_3		
B Bus 7			15_2			4_3	4_3		
$\overline{BLK-CA}$	ALU					10_2	10_2		
BRANCH	ALU			9_2		5_2			
CØ	ALU					16_2	16_2		
C1	ALU					S_2	S_2		
C2	ALU					R_2	R_2		
C3	ALU					12_2	12_2		
C4	ALU					11_2	11_2		

Signal	Source DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
C5	ALU					M_2	M_2		
C6	ALU					K_2	K_2		
C7	ALU					H_2	H_2		
CA	ALU					8_2	8_2		
CA Ø	IC	10_2	7_2	6_2					
CA 1	IC	P_2	H_2	H_2					
CA 2	IC	L_2	6_2	5_2					
CA 3	IC	11_2	9_2	7_2					
CA 4	IC	M_2	F_2	F_2					
CA 5	IC	9_2	5_2	4_2					
CA 6	IC	20_2	11_2	12_2					
CA 7	IC	V_2	L_2	M_2					
CA 8	IC	X_2	N_2	P_2					
CA 9	IC	19_2	10_2	11_2					
CA 10	IC	21_2		13_2					
CA 11	IC	W_2		N_2					
C Bus Ø					18_2		17_2		
C Bus 1					15_2		15_2		
C Bus 2					14_2		14_2		
C Bus 3					13_2		13_2		
C Bus 4					P_2		P_2		
C Bus 5					N_2		N_2		
C Bus 6					L_2		L_2		
C Bus 7					J_2		J_2		
$\overline{\text{CBS}}$	REG						20_3		5_3
CDI_{0-23}									
CDO Ø	CM	20_3	L_3		L_3				
CDO 1	CM	19_3	K_3		H_3				
CDO 2	CM	18_3	J_3		F_3				
CDO 3	CM	M_3	E_3		E_3				
CDO 4	CM	L_3	D_3		D_3				
CDO 5	CM	10_3	3_3		C_3				
CDO 6	CM	C_2	E_2		D_2				
CDO 7	CM	B_2	D_2		4_2				
CDO 8	CM	A_2	C_2		B_2				

Signal	Source	DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
CDO 9	CM		10_1	1_2		A_2				
CDO 10	CM		K_1	A_2		R_1				
CDO 11	CM		J_1	N_1		P_1				
CDO 12	CM		X_3	11_3		16_3				
CDO 13	CM		W_3	7_3		10_3				
CDO 14	CM		V_3	6_3		21_2				
CDO 15	CM		N_3	5_3		20_2				
CDO 16	CM		11_3	4_3				5_3		
CDO 17	CM		K_3	C_3		Y_2		Y_2		
CDO 18	CM		3_2	4_2		E_1		L_1		
CDO 19	CM		2_2	3_2		F_2		F_2		
CDO 20	CM		1_2	2_2		6_2		6_2		
CDO 21	CM		L_1	B_2		E_2		E_2		
CDO 22	CM		9_1	R_1		5_2		5_2		
CDO 23	CM		8_1	13_1				1_2		
$\overline{CE}$	ALU	11_1	U_2				T_2			
CEN	ALU						9_2	9_2		
$\overline{CIO}$	ST					5_1		5_1		
CNTD	IC				10_1	10_1				
$\overline{CPB}$	REG							19_3		4_3
DI Ø	ALU	16_3					16_3			
DI 1	ALU	17_3					17_3			
DI 2	ALU	S_3					R_3			
DI 3	ALU	T_3					S_3			
DI 4	ALU	U_3					19_3			
DI 5	ALU	15_3					15_3			
DI 6	ALU	14_3					14_3			
DI 7	ALU	P_3					P_3			
DI 8	ALU	13_3					13_3			
DI 9	MB	13_1					16_3			
DI 10	MB	P_1					17_3			
DI 11	MB	12_1					R_3			
DI 12	MB	6_1					S_3			
DI 13	MB	5_1					19_3			

Signal	Source	DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
DI 14	MB	E_1					15_3			
DI 15	MB	F_1					14_3			
DI 16	MB	4_1					P_3			
DI 17	MB	D_1					13_3			
$\overline{\text{DMPI}}$	REG				2_2			2_2		
DMS 1	ST	10_3				20_3				
DMS 2	ST	10_3				X_3				
DO Ø	DM	19_3		T_3						
DO 1	DM	20_3		U_3						
DO 2	DM	V_3		17_3						
DO 3	DM	W_3		18_3						
DO 4	DM	18_3		S_3						
DO 5	DM	X_3		19_3						
DO 6	DM	11_3		9_3						
DO 7	DM	M_3		H_3						
DO 8	DM	12_3		10_3						
DO 9	DM	M_1		11_1						
DO 10	DM	L_1		10_1						
DO 11	DM	10_1		L_1						
DO 12	DM	H_1		7_1						
DO 13	DM	8_1		J_1						
DO 14	DM	J_1		8_1						
DO 15	DM	K_1		9_1						
DO 16	DM	7_1		H_1						
DO 17	DM	9_1		K_1						
$\overline{\text{HALT}}$	I/O							K_1		K_1
$\overline{\text{IB 1}}$	I/O							P_1		15_1
$\overline{\text{IB 2}}$	I/O							B_2		S_1
$\overline{\text{IB 3}}$	I/O							4_2		14_1
$\overline{\text{IB 4}}$	I/O							12_1		R_1
$\overline{\text{IB 5}}$	I/O							C_2		N_1
$\overline{\text{IB 6}}$	I/O							11_1		P_1
$\overline{\text{IB 7}}$	I/O							A_2		L_1
$\overline{\text{IB 8}}$	I/O							M_1		M_1
$\overline{\text{IB 9}}$	I/O							10_1		2_3

Signal	Source	DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
$\overline{\text{IBS}}$	I/O							F_3		1_3
ICC Ø	IC				14_3	14_3				
ICC 1	IC				15_3	15_3				
ICC 2	IC				13_3	13_3				
ICC 3	IC				B_3	A_3				
ICC 4	IC				R_3	R_3				
ICC 5	IC				P_3	P_3				
ICC 6	IC				N_3	N_3				
ICC 7	IC				12_3	12_3				
ICC 8	IC				K_3	K_3				
ICC 9	IC				9_3	9_3				
ICC 10	IC				J_3	J_3				
ICC 11	IC				8_3	8_3				
ICC 12	IC				5_3	5_3				
ICC 13	IC				4_3	4_3				
ICC 14	IC				3_3	3_3				
ICC 15	IC				2_3	2_3				
I/O CLK	ALU						11_3			L_3
$\overline{\text{LHPC}}$	IC				11_1	11_1				
$\overline{\text{LLPC}}$	IC				M_1	M_1				
LOP	ST			T_2	U_2	T_2		T_2		
$\overline{\text{LPI}}$	ST				9_1	9_1	9_1			
$\overline{\text{MARCLK}}$	ALU	R_3		14_3	H_3		F_3			
$\overline{\text{MS 1}}$	IC		18_2		E_2					
$\overline{\text{MS 2}}$	IC		T_2		D_2					
$\overline{\text{MS 3}}$	IC		17_2		C_2					
$\overline{\text{MS 4}}$	IC		18_2		17_2					
$\overline{\text{MS 5}}$	IC		T_2		T_2					
$\overline{\text{MS 6}}$	IC		17_2		16_2					
$\overline{\text{OB1}}$	REG		1_3					6_3		A_3
$\overline{\text{OB2}}$	REG		Z_2					11_3		B_3
$\overline{\text{OB3}}$	REG		R_1					M_3		C_3
$\overline{\text{OB4}}$	REG		12_1					12_3		D_3

Signal	Source	DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
$\overline{OB5}$	REG		11_1					14_3		J_3
$\overline{OB6}$	REG		6_1					13_3		H_3
$\overline{OB7}$	REG		5_1					P_3		F_3
$\overline{OB8}$	REG		4_1					N_3		E_3
$\overline{OBS}$	REG							H_1		H_1
PCCC	IC				8_1	8_1				
PECM	MC			17_2	18_2	16_2				
PEDM	MC			J_2	3_2			3_2		
PH Ø	ST	9_3	M_1			19_3	20_3			
PH 1	ST	8_3	F_1			22_2	3_3			
PH 2	ST	K_3	E_1			W_3	X_3			
PH 3	ST	J_3	D_1			18_3	E_3			
PH 4	ST	F_3	T_3			W_2	2_3			
PH 5	ST	C_3	S_3			11_2	14_2			
PH 6	ST	5_3	R_3			R_2	Z_2			
PH 7	ST		2_3			M_2	L_2			
PINC	IC				K_1	K_1				
PL Ø	ST		16_3	R_3		T_3	T_3			
PL 1	ST	6_3	15_3			S_2	V_2			
PL 2	ST	D_3	14_3			12_2	15_2			
PL 3	ST	2_3	B_3			9_2	N_2			
PL 4	ST	14_1	A_3			1_2	F_2			
PL 5	ST	A_3	22_2			7_2	J_2			
PL 6	ST	B_3	P_1			10_2	P_2			
PL 7	ST	H_3	N_1			X_2	A_3			
POR	PSR				W_2	V_2		V_2	E_1	
$\overline{PRMS}$	PSR		E_3						B_1	3_3
RØ	MC			P_3			1_3	1_3		
R1	MC			13_3			22_2	22_2		
R2	MC			16_3	16_3		18_3	18_3		
R3	MC			15_3	T_3		V_3	V_3		
R4	MC			Y_2	Z_2		M_3	S_3		
R5	MC			1_3	E_3		N_3	15_3		
R6	MC			22_2	1_3		21_2	21_2		

Signal	Source	DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
R7	MC			A_3	D_3		C_3	C_3		
R8	MC			2_3	F_3			E_3		
R9	MC			19_2	20_2			18_2		
R10	MC			X_2	Y_2			X_2		
R11	MC			N_3	L_3			L_3		
R12	MC			20_3	18_3					
R13	MC			X_3	19_3					
R14	MC			W_3	W_3		W_3	W_3		
R15	MC			V_3	U_3		U_3	U_3		
R16	MC			F_3	6_3	6_3	6_3			
R17	MC			M_3	10_3					
R18	MC			4_1	4_1		4_1			
R19	MC			12_3			12_3			
R20	MC			5_1	5_1		5_1			
R21	MC			E_1	E_1		E_1			
R22	MC			D_1	D_1		D_1			
RA Ø	IC	E_3			J_2					
RA 1	IC	7_3			K_2					
RA 2	IC	3_3			8_2					
RA 3	IC	R_1			10_2					
RA 4	IC	1_3			14_2					
RA 5	IC	4_3			R_2					
$\overline{R}$/B	I/O							X_3		K_3
$\overline{REF}$	ALU	L_3	Y_2		B_2		B_2			
REFCLK	IC				15_2		13_2			
$\overline{RESET}$	PSR				S_2				D_1	
$\overline{ROMS}$	IC			W_2	X_2		11_1			
$\overline{R}$/W1	MC	N_3		B_3						
$\overline{R}$/W2	MC	N_1		12_2						
$\overline{R}$/W (CM)	IC		K_2		F_1					
SØ	ST				7_3	7_3				
S1	ST				11_3	11_3				
S2	ST				M_3	M_3				
S3	ST				S_3	S_3				

Signal	Source DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
S4	ST			17_3	17_3				
S5	ST			V_3	V_3				
S6	ST			A_3	Z_2				
S7	ST			C_3	B_3				
$\overline{SB}$	ST			19_2	17_2				
SH0	REG					7_2	7_2		
$\overline{SR}$	ST			21_2	19_2	19_2			
$\overline{T1}$	ALU			14_1	14_1	14_1	14_1		
$\overline{T2}$	ALU				12_1	12_1		F_1	
$\overline{T3}$	ALU		P_1	N_2	N_1	N_1	N_1		
$\overline{T4}$	ALU		M_1	P_1	4_1	P_1			
$\overline{T5}$	ALU			1_2		1_2			
$\overline{T6}$	ALU		F_1		F_1	F_1	F_1		
$\overline{T7}$	ALU			12_1		M_1			
$\overline{T8}$	ALU			A_2		A_2			
$\overline{T9}$	ALU	4_2			2_2	2_2			
$\overline{T10}$	ALU				C_2	C_2			
$\overline{T11}$	ALU				3_2	3_2			
$\overline{T12}$	ALU			13_1	13_1	13_1	13_1		
$\overline{T13}$	ALU					4_2			
$\overline{T14}$	ALU					D_2			
$\overline{T15}$	ALU					E_2			
$\overline{T16}$	ALU			R_1		R_1	R_1		
$\overline{TAP}$	ST			H_1	H_1				
$\overline{TCMDR}$	ALU		6_1		J_1	J_1	J_1		
$\overline{TSP}$	ST			7_1	7_1				
XOP	ST		12_1	L_1	L_1				
$\overline{XPA}$	ST			6_1	6_1				

Signal	Source	DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
+5VR1	PSR			2_1				2_1	8_1	2_1
				B_1				B_1	J_1	B_1
				21_3				21_3		14_3
				Y_3				Y_3		R_3
+5VR2	PSR	2_1	2_1		2_1	2_1	2_1		10_1	
		B_1	B_1		B_1	B_1	B_1		L_1	
		21_3	21_3		21_3	21_3	21_3			
		Y_3	Y_3		Y_3	Y_3	Y_3			
-5VR	PSR	3_1	3_1	3_1	3_1	3_1	3_1	3_1	15_1	
		C_1	C_1	C_1	C_1	C_1	C_1	C_1	S_1	
+12VR	PSR	15_1	15_1	15_1	15_1	15_1	15_1	15_1	11_1	15_3
		S_1	S_1	S_1	S_1	S_1	S_1	S_1	M_1	S_3
-12VR	PSR								12_1	12_3
									N_1	N_3
$\pm$0V		1_1	1_1	1_1	1_1	1_1	1_1	1_1	13_1	3_1
		A_1	A_1	A_1	A_1	A_1	A_1	A_1	P_1	C_1
		22_3	22_3	22_3	22_3	22_3	22_3	22_3	14_1	13_3
		Z_3	Z_3	Z_3	Z_3	Z_3	Z_3	Z_3	R_1	P_3
				8_3						

MB0080-A M U L T I - L E V E L B I L L OF M A T E R I A L AS OF RUN DATE: 07/16/79

ASSEMBLY PART NUMBER 177-3012- - -
ASSEMBLY DESCRIPTION 2200MVP-8 CPU 32K MEM

POSITION IN STRUCTURE	LEGEND 1 2 3	COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY
1	IN	187-3014- - -	2200MVP-16 CPU 64K MEM		1.0000
2	P IN	210-7587-1A- -	PCA 2200MVP 64KX9 BIT DATA MEMORY	E11526	1.0000
3	IN	209-7587-1 - -	PCA 2200MVP 64KX9 BIT DATA MEM NC		1.0000
2	P FS	279-0313- - -	2200MVP/VP COMMON MECH ASSY 60HZ		1.0000
3	IN	210-6789-A - -	PCA 2200VP MEMORY INTERFACE BD		1.0000
4	IN	209-6789- - -	PCA 2200VP MEMORY INTERFACE BD		1.0000
3	IN	210-6790- - -	PCA 2200VP INSTRUCTION COUNTER BD		1.0000
3	IN	210-6791- - -	PCA 2200VP STACK BOARD		1.0000
3	IN	210-6792- - -	PCA 2200VP ALU		1.0000
3	IN	210-6793-1 - -	PCA 2200MVP REGISTER BOARD	E10639	1.0000
3	IN	210-7397- - -	PCA 2200VP REG W/CURRENT FOLD BK	E10274	1.0000
3	P IN	210-7588-A - -	PCA 2200VP/MVP 16X24 BIT MEM CNTL	E11598	1.0000
4	IN	209-7588- - -	PCA 2200VP/MVP 16X24 BIT MEM CNTL		1.0000
3	IN	270-0355- - -	2200VP CPU CHASSIS (9I/O)		1.0000
4	IN	210-7498- - -	PCA 2200VPA/MVPA MOTHERBOARD	E10274	1.0000
4	IN	270-0356- - -	HEATSINK ASSY(2200VP)	E10389	1.0000
5	IN	270-3066- - -	HEATSINK HARNESS(2200VP)C6482-126		1.0000
4	IN	270-3065- - -	TRANSFORMER HARNESS(VP 60HZ)6482125		1.0000
1	P IN	210-7587-1A- -	PCA 2200MVP 64KX9 BIT DATA MEMORY	E12201	1.0000-
2	IN	209-7587-1 - -	PCA 2200MVP 64KX9 BIT DATA MEM NC		1.0000
1	P IN	210-7587-1B- -	PCA 2200MVP 32K X 9BIT MVP DATA MEM	E12201	1.0000
2	IN	209-7587-1 - -	PCA 2200MVP 64KX9 BIT DATA MEM NC		1.0000
1	IN	615-1478- - -	LABEL,2200MVP 115V 50HZ B6611-239	E10392	1.0000
1	IN	615-1491- - -	LBL,2200MVP 115V 60HZ B6611-240	E10392	1.0000

MB0080-A M U L T I - L E V E L B I L L OF M A T E R I A L AS OF RUN DATE: 05/10/79

ASSEMBLY PART NUMBER 177-3014- - -
ASSEMBLY DESCRIPTION 2200MVP-16 CPU 64K MEM

POSITION IN STRUCTURE	LEGEND 1	2	3	COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY
1		IN		187-3014- - -	2200MVP-16 CPU 64K MEM		1.0000
2	P	IN		210-7587-1A- -	PCA 2200MVP 64KX9 BIT DATA MEMORY	E11526	1.0000
3		IN		209-7587-1 - -	PCA 2200MVP 64KX9 BIT DATA MEM NC		1.0000
2		IN		210-7588-A - -	PCA 2200VP/MVP 28X24 CNTL MEM	E11598	1.0000
3		IN		209-7588- - -	PCA 2200VP/MVP 28X24 CNTL MEM		1.0000
2	P	FS		279-0313- - -	2200MVP/VP COMMON MECH ASSY 60HZ		1.0000
3		IN		210-6789-A - -	PCA 2200VP MEMORY INTERFACE BD		1.0000
4		IN		209-6789- - -	PCA 2200VP MEMORY INTERFACE BD		1.0000
3		IN		210-6790- - -	PCA 2200VP INSTRUCTION COUNTER BD		1.0000
3		IN		210-6791- - -	PCA 2200VP STACK BOARD		1.0000
3		IN		210-6792- - -	PCA 2200VP ALU		1.0000
3		IN		210-6793-1 - -	PCA 2200MVP REGISTER BOARD	E10639	1.0000
3		IN		210-7397- - -	PCA 2200VP REG W/CURRENT FOLD BK	E10274	1.0000
3		IN		210-7588-A - -	PCA 2200VP/MVP 28X24 CNTL MEM	E11598	1.0000
4		IN		209-7588- - -	PCA 2200VP/MVP 28X24 CNTL MEM		1.0000
3		IN		270-0355- - -	2200VP CPU CHASSIS (9I/O)		1.0000
4		IN		210-7498- - -	PCA 2200VPA/MVPA MOTHERBOARD	E10274	1.0000
4		IN		270-0356- - -	HEATSINK ASSY(2200VP)	E10389	1.0000
5		IN		270-3066- - -	HEATSINK HARNESS(2200VP)C6482-126		1.0000
4		IN		270-3065- - -	TRANSFORMER HARNESS(VP 60HZ)6482125		1.0000
1		IN		615-1478- - -	LABEL,2200MVP 115V 50HZ B6611-239	E10392	1.0000
1		IN		615-1491- - -	LBL,2200MVP 115V 60HZ B6611-240	E10392	1.0000

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ASSEMBLY PART NUMBER 177-3108- - -
ASSEMBLY DESCRIPTION 2200 MVP-8A CPU 32K MEM 9 I/O

POSITION IN STRUCTURE	LEGEND 1 2 3	COMPONENT PART NUMBER	DESCRIPTION		E C N
1	P IN	210-7587-1A- -	PCA 2200MVP 64KX9 BIT DATA MEMORY		E12201
2	IN	209-7587-1 - -	PCA 2200MVP 64KX9 BIT DATA MEM NC		
1	P IN	210-7587-1B- -	PCA 2200MVP 32K X 9BIT MVP DATA MEM		E11526
2	IN	209-7587-1 - -	PCA 2200MVP 64KX9 BIT DATA MEM NC		
1	IN	615-1533- - -	LABEL # 2200 MVPA 60HZ	B6611-295	E11498
1	IN	615-1536- - -	LABEL # 2200 MVPA 50HZ	B6611-296	E11498

MB0080-A M U L T I - L E V E L B I L L OF M A T E R I A L AS OF RUN DATE: 05/10/79

ASSEMBLY PART NUMBER 187-3112- - -
ASSEMBLY DESCRIPTION 2200 MVP-12A CPU 48K MEM 9 I/O

POSITION IN STRUCTURE	LEGEND 1 2 3	COMPONENT PART NUMBER	DESCRIPTION		E C N	QUANTITY PER ASSY
1	IN	187-3112- - -	2200 MVPA CPU 9 I/O 48K MEM		E10974	1.0000
1	IN	615-1533- - -	LABEL # 2200 MVPA 60HZ	B6611-295	E11498	1.0000
1	IN	615-1536- - -	LABEL # 2200 MVPA 50HZ	B6611-296	E11498	1.0000

MB0080-A M U L T I - L E V E L B I L L OF M A T E R I A L AS OF RUN DATE: 05/10/79

ASSEMBLY PART NUMBER 177-3116- - -
ASSEMBLY DESCRIPTION 2200 MVP-16A CPU 64K MEM 9 I/O

POSITION IN STRUCTURE	LEGEND 1 2 3	COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY
1	IN	187-3116- - -	2200 MVPA CPU 9 I/O 64K MEM	E10974	1.0000
2	P IN	210-7587-1A- -	PCA 2200MVP 64KX9 BIT DATA MEMORY		1.0000
3	IN	209-7587-1 - -	PCA 2200MVP 64KX9 BIT DATA MEM NC		1.0000
2	P IN	279-0354- - -	2200 MVP-A COMMON MECH ASSY 60HZ		1.0000
3	IN	210-6789-A - -	PCA 2200VP MEMORY INTERFACE BD		1.0000
4	IN	209-6789- - -	PCA 2200VP MEMORY INTERFACE BD		1.0000
3	IN	210-6790- - -	PCA 2200VP INSTRUCTION COUNTER BD		1.0000
3	IN	210-6791- - -	PCA 2200VP STACK BOARD		1.0000
3	IN	210-6792- - -	PCA 2200VP ALU		1.0000
3	IN	210-6793-1 - -	PCA 2200MVP REGISTER BOARD		1.0000
3	IN	210-7397- - -	PCA 2200VP REG W/CURRENT FOLD BK		1.0000
3	IN	210-7588-A - -	PCA 2200VP/MVP 28X24 CNTL MEM	E11598	1.0000
4	IN	209-7588- - -	PCA 2200VP/MVP 28X24 CNTL MEM		1.0000
3	IN	270-0452- - -	2200 MVPA/VPA CPU CHASS 9 I/O 60HZ		1.0000
4	IN	210-7498- - -	PCA 2200VPA/MVPA MOTHERBOARD		1.0000
4	IN	270-0564- - -	HEATSINK ASSY 2200 MVPA/VPA		1.0000
5	IN	270-3121- - -	MVPA PWR SUP HTSNK HARN D6482-378	E10329	1.0000
4	IN	270-3120- - -	XMFR HARNESS MVPA 60 HTZ D6482-341	E11393	1.0000
1	IN	615-1533- - -	LABEL # 2200 MVPA 60HZ B6611-295	E11498	1.0000
1	IN	615-1536- - -	LABEL # 2200 MVPA 50HZ B6611-296	E11498	1.0000

MB0080-A M U L T I - L E V E L B I L L OF M A T E R I A L AS OF RUN DATE: 05/10/79

ASSEMBLY PART NUMBER 177-3124- - -
ASSEMBLY DESCRIPTION 2200 MVP-24A CPU 96K MEM 9 I/O

POSITION IN STRUCTURE	LEGEND 1 2 3	COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY
1	IN	187-3124- - -	2200 MVPA CPU 9 I/O 96K MEM		1.0000
2	IN	210-7587-3B- -	PCA 2200MVP 96K X 9BIT MVP DATA MEM	E11262	1.0000
3	IN	209-7587-3 - -	PCA 2200MVP 128KX9 BIT DATA MEM NC		1.0000
2	P IN	279-0354- - -	2200 MVP-A COMMON MECH ASSY 60HZ		1.0000
3	IN	210-6789-A - -	PCA 2200VP MEMORY INTERFACE BD		1.0000
4	IN	209-6789- - -	PCA 2200VP MEMORY INTERFACE BD		1.0000
3	IN	210-6790- - -	PCA 2200VP INSTRUCTION COUNTER BD		1.0000
3	IN	210-6791- - -	PCA 2200VP STACK BOARD		1.0000
3	IN	210-6792- - -	PCA 2200VP ALU		1.0000
3	IN	210-6793-1 - -	PCA 2200MVP REGISTER BOARD		1.0000
3	IN	210-7397- - -	PCA 2200VP REG W/CURRENT FOLD BK		1.0000
3	IN	210-7588-A - -	PCA 2200VP/MVP 28X24 CNTL MEM	E11598	1.0000
4	IN	209-7588- - -	PCA 2200VP/MVP 28X24 CNTL MEM		1.0000
3	IN	270-0452- - -	2200 MVPA/VPA CPU CHASS 9 I/O 60HZ		1.0000
4	IN	210-7498- - -	PCA 2200VPA/MVPA MOTHERBOARD		1.0000
4	IN	270-0564- - -	HEATSINK ASSY 2200 MVPA/VPA		1.0000
5	IN	270-3121- - -	MVPA PWR SUP HTSNK HARN D6482-378	E10329	1.0000
4	IN	270-3120- - -	XMFR HARNESS MVPA 60 HTZ D6482-341	E11393	1.0000
1	IN	615-1533- - -	LABEL # 2200 MVPA 60HZ B6611-295		1.0000
1	IN	615-1536- - -	LABEL # 2200 MVPA 50HZ B6611-296		1.0000

MB0060-A M U L T I - L E V E L B I L L OF M A T E R I A L AS OF RUN DATE: 05/10/79

ASSEMBLY PART NUMBER 177-3132- - -
ASSEMBLY DESCRIPTION 2200 MVP-32A CPU 128K MEM 9 I/O

POSITION IN STRUCTURE	LEGEND 1 2 3	COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY
1	IN	187-3164- - -	2200 MVPA CPU 9 I/O 256K		1.0000
2	P IN	210-7587-3A- -	PCA 2200MVP 128KX9 BIT DATA MEMORY		2.0000
3	IN	209-7587-3 - -	PCA 2200MVP 128KX9 BIT DATA MEM NC		1.0000
2	P IN	279-0354- - -	2200 MVP-A COMMON MECH ASSY 60HZ		1.0000
3	IN	210-6789-A - -	PCA 2200VP MEMORY INTERFACE BD		1.0000
4	IN	209-6789- - -	PCA 2200VP MEMORY INTERFACE BD		1.0000
3	IN	210-6790- - -	PCA 2200VP INSTRUCTION COUNTER BD		1.0000
3	IN	210-6791- - -	PCA 2200VP STACK BOARD		1.0000
3	IN	210-6792- - -	PCA 2200VP ALU		1.0000
3	IN	210-6793-1 - -	PCA 2200MVP REGISTER BOARD		1.0000
3	IN	210-7397- - -	PCA 2200VP REG W/CURRENT FOLD BK		1.0000
3	IN	210-7588-A - -	PCA 2200VP/MVP 28X24 CNTL MEM	E11598	1.0000
4	IN	209-7588- - -	PCA 2200VP/MVP 28X24 CNTL MEM		1.0000
3	IN	270-0452- - -	2200 MVPA/VPA CPU CHASS 9 I/O 60HZ		1.0000
4	IN	210-7498- - -	PCA 2200VPA/MVPA MOTHERBOARD		1.0000
4	IN	270-0564- - -	HEATSINK ASSY 2200 MVPA/VPA		1.0000
5	IN	270-3121- - -	MVPA PWR SUP HTSNK HARN D6482-378	E10329	1.0000
4	IN	270-3120- - -	XMFR HARNESS MVPA 60 HTZ D6482-341	E11393	1.0000
1	P IN	210-7587-3A- -	PCA 2200MVP 128KX9 BIT DATA MEMORY		1.0000-
2	IN	209-7587-3 - -	PCA 2200MVP 128KX9 BIT DATA MEM NC		1.0000
1	IN	615-1533- - -	LABEL # 2200 MVPA 60HZ B6611-295	E11498	1.0000
1	IN	615-1536- - -	LABEL # 2200 MVPA 50HZ B6611-296	E11498	1.0000

MB00B0-A M U L T I - L E V E L B I L L OF M A T E R I A L AS OF RUN DATE: 05/10/79

ASSEMBLY PART NUMBER 177-3148- - -
ASSEMBLY DESCRIPTION 2200 MVP-4PA CPU 192K MEM 9 I/O

POSITION IN STRUCTURE	LEGEND 1	2	3	COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY
1		IN		187-3164- - -	2200 MVPA CPU 9 I/O 256K	E10974	1.0000
2	P	IN		210-7587-3A- -	PCA 2200MVP 128KX9 BIT DATA MEMORY		2.0000
3		IN		209-7587-3 - -	PCA 2200MVP 128KX9 BIT DATA MEM NC		1.0000
2	P	IN		279-0354- - -	2200 MVP-A COMMON MECH ASSY 60HZ		1.0000
3		IN		210-6789-A - -	PCA 2200VP MEMORY INTERFACE BD		1.0000
4		IN		209-6789- - -	PCA 2200VP MEMORY INTERFACE BD		1.0000
3		IN		210-6790- - -	PCA 2200VP INSTRUCTION COUNTER BD		1.0000
3		IN		210-6791- - -	PCA 2200VP STACK BOARD		1.0000
3		IN		210-6792- - -	PCA 2200VP ALU		1.0000
3		IN		210-6793-1 - -	PCA 2200MVP REGISTER BOARD		1.0000
3		IN		210-7397- - -	PCA 2200VP REG W/CURRENT FOLD BK		1.0000
3		IN		210-7588-A - -	PCA 2200VP/MVP 28X24 CNTL MEM	E11598	1.0000
4		IN		209-7588- - -	PCA 2200VP/MVP 28X24 CNTL MEM		1.0000
3		IN		270-0452- - -	2200 MVPA/VPA CPU CHASS 9 I/O 60HZ		1.0000
4		IN		210-7498- - -	PCA 2200VPA/MVPA MOTHERBOARD		1.0000
4		IN		270-0564- - -	HEATSINK ASSY 2200 MVPA/VPA		1.0000
5		IN		270-3121- - -	MVPA PWR SUP HTSNK HARN D6482-378	E10329	1.0000
4		IN		270-3120- - -	XMFR HARNESS MVPA 60 HTZ D6482-341	E11393	1.0000
1	P	IN		210-7587-3A- -	PCA 2200MVP 128KX9 BIT DATA MEMORY	E10974	1.0000-
2		IN		209-7587-3 - -	PCA 2200MVP 128KX9 BIT DATA MEM NC		1.0000
1		IN		615-1533- - -	LABEL # 2200 MVPA 60HZ B6611-295	E11498	1.0000
1		IN		615-1536- - -	LABEL # 2200 MVPA 50HZ B6611-296	E11498	1.0000

M80080-A M U L T I - L E V E L B I L L OF M A T E R I A L AS OF RUN DATE: 05/10/79

ASSEMBLY PART NUMBER 177-3164- - -
ASSEMBLY DESCRIPTION 2200 MVP-64A CPU 256K MEM 9 I/O

POSITION IN STRUCTURE	LEGEND 1 2 3	COMPONENT PART NUMBER	DESCRIPTION		E C N	QUANTITY PER ASSY
1	IN	187-3164- - -	2200 MVPA CPU 9 I/O 256K		E10974	1.0000
2	P IN	210-7587-3A- -	PCA 2200MVP 128KX9 BIT DATA MEMORY			2.0000
3	IN	209-7587-3 - -	PCA 2200MVP 128KX9 BIT DATA MEM NC			1.0000
2	P IN	279-0354- - -	2200 MVP-A COMMON MECH ASSY 60HZ			1.0000
3	IN	210-6789-A - -	PCA 2200VP MEMORY INTERFACE BD			1.0000
4	IN	209-6789- - -	PCA 2200VP MEMORY INTERFACE BD			1.0000
3	IN	210-6790- - -	PCA 2200VP INSTRUCTION COUNTER BD			1.0000
3	IN	210-6791- - -	PCA 2200VP STACK BOARD			1.0000
3	IN	210-6792- - -	PCA 2200VP ALU			1.0000
3	IN	210-6793-1 - -	PCA 2200MVP REGISTER BOARD			1.0000
3	IN	210-7397- - -	PCA 2200VP REG W/CURRENT FOLD BK			1.0000
3	IN	210-7588-A - -	PCA 2200VP/MVP 28X24 CNTL MEM		E11598	1.0000
4	IN	209-7588- - -	PCA 2200VP/MVP 28X24 CNTL MEM			1.0000
3	IN	270-0452- - -	2200 MVPA/VPA CPU CHASS 9 I/O 6CHZ			1.0000
4	IN	210-7498- - -	PCA 2200VPA/MVPA MOTHERBOARD			1.0000
4	IN	270-0564- - -	HEATSINK ASSY 2200 MVPA/VPA			1.0000
5	IN	270-3121- - -	MVPA PWR SUP HTSNK HARN	D6482-378	E10329	1.0000
4	IN	270-3120- - -	XMFR HARNESS MVPA 60 HTZ	D6482-341	E11393	1.0000
1	IN	615-1533- - -	LABEL # 2200 MVPA 60HZ	B6611-295	E11498	1.0000
1	IN	615-1536- - -	LABEL # 2200 MVPA 50HZ	B6611-296	E11498	1.0000

MB0080-A M U L T I - L E V E L B I L L OF M A T E R I A L AS OF RUN DATE: 05/10/79

ASSEMBLY PART NUMBER 177-3236-D - -
ASSEMBLY DESCRIPTION 2236D WK/ST 80X24 TRANS TERMINAL

POSITION IN STRUCTURE	LEGEND 1 2 3		COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY
1	IN		187-3236-D - -	2236D WK/ST 80X24 TRANS TERMINAL		1.0000
2	IN		210-7158-A - -	PCA 2236 80X24 CRT/PTR 60HZ		1.0000
3	IN		209-7158- - -	PCA 2236 80X24 CRT/PTR 60HZ		1.0000
4	IN		220-1068- - -	CABLE,CRT BD (7058)(E)B6482-86	EC7027	1.0000
2	IN		210-7292-1A- -	PCA 2236MXD INTERACV TERM WS ELEC		1.0000
3	IN		209-7292-1 - -	PCA 2236MXD INTERACV TERM WS ELEC		1.0000
2	IN		220-2236-25- -	2236 DIRECT CABLE ASSY	EC9918	1.0000
2	P FS		279-0314- - -	2236D COMMON MECH ASSY		1.0000
3	IN		210-7156- - -	PCA 928 PS REG FOR MOTOROLA MONITOR	EC8365	1.0000
3	IN		220-1143- - -	WIRE & LUG ASSY TYPE P065 D6482-12	EC9294	1.0000
3	IN		270-0373- - -	12" MONITOR II & PWR SUP ASM II	EC9775	1.0000
4	IN		270-0371- - -	POWER SUPPLY II,12" MONITOR(PRELIM)		1.0000
5	P FS	*	210-7455- - -	PCA 9/12 MONITOR WANG MON PS REG		1.0000
6	IN		220-1107- - -	12" CRT POWER SUPLY CABLE B6482-141		1.0000
4	IN	*	270-0372- - -	12" MONITOR ASM II (LESS PWR SUP)		1.0000
5	IN	*	210-7456- - -	PCA 12" MONITOR ELEC	EC8373	1.0000
5	IN		220-0160- - -	BRIGHTNESS POT CABLE ASSY C6482-140		1.0000
5	IN		270-3068- - -	12" CRT HARNESS ASSY D6482-139		1.0000
5	IN		270-3092- - -	YOKE ASSY (12" MONITOR) B6482-246		1.0000
5	IN		270-3104- - -	12"FLYBACK XFORMER HARN C6482-327	EC9723	1.0000
3	IN		270-0400-1 - -	2236 WORK ST CHASSIS ASSY	EC8561	1.0000
4	IN		210-7293- - -	PCA 2236 INTERACTIVE TERM WS MB		1.0000
5	IN		220-3014- - -	24 COND 14"FLAT CABLE C-6482-79	PATREL	1.0000
4	IN		220-1076- - -	POWER CORD ASSY(F CHAS)B6482-95		1.0000
4	IN		220-1101- - -	P054 WIRE&LUG ASSY(E CHAS)6482-12		1.0000
4	IN		220-1143- - -	WIRE & LUG ASSY TYPE P065 D6482-12	EC9931	1.0000
4	IN		220-1180- - -	WIRE & LUG ASSY TYPE P077 D6482-12	EC9931	1.0000
4	IN	*	270-0346-1 - -	WS POWER SUPPLY ASSY.		1.0000
5	IN		220-1042- - -	P022 WIRE & LUG ASSY(2LCRT)D6482-12		1.0000
5	IN		220-1074- - -	CABLE PS/MB(F CHASSIS)B6482-91		1.0000
5	IN		220-1077- - -	P043 WIRE & LUG ASSY(F CHAS)B648296		1.0000
5	IN		220-1094- - -	P048 WIRE & LUG ASSY B		1.0000
3	WC		279-0352- - -	928 WK/ST COVER ASSY	EC9905	1.0000
3	IN		279-1015- - -	928WZ BASE ASSY(ALUM TAPE) 6841-30	EC8153	1.0000
1	IN		615-1468- - -	LBL,2236 WK/ST 115V 50HZ B6611-272	E10392	1.0000
1	IN		615-1485- - -	LBL,2236 WK/ST 115V 60HZ B6611-271	E10392	1.0000

MB0080-A M U L T I - L E V E L B I L L OF M A T E R I A L AS OF RUN DATE: 05/10/79

ASSEMBLY PART NUMBER 177-3236-E - -
ASSEMBLY DESCRIPTION 2236 INTERACTIVE TERM WK/ST

POSITION IN STRUCTURE	LEGEND 1 2 3		COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY
1	IN		187-3236-E - -	2236E INTERACTIVE TERM WK/ST		1.0000
2	IN		210-7592-A - -	PCA 2236E SINGLE BD TERM ELEC		1.0000
3	IN		209-7592- - -	PCA 2236E SINGLE BD TERM ELEC		1.0000
4	IN		220-1103- - -	CRT BRD (W2)(COAX)B6482-122	E11192	1.0000
2	IN		220-3039- - -	24 PIN FLAT CABLE ASSY(18")C6482-79		1.0000
2	IN		279-0359- - -	2236E INTERACTIVE TERM COMMON ASSY		1.0000
3	IN		220-1143- - -	WIRE & LUG ASSY TYPE P065 D6482-12		1.0000
3	IN		270-0373- - -	12" MONITOR II & PWR SUP ASM II		1.0000
4	IN		270-0371- - -	POWER SUPPLY II,12" MONITOR(PRELIM)		1.0000
5	P FS	*	210-7455- - -	PCA 9/12 MONITOR WANG MON PS REG		1.0000
6	IN		220-1107- - -	12" CRT POWER SUPLY CABLE B6482-141		1.0000
4	IN	*	270-0372- - -	12" MONITOR ASM II (LESS PWR SUP)		1.0000
5	IN	*	210-7456- - -	PCA 12" MONITOR ELEC	EC8373	1.0000
5	IN		220-0160- - -	BRIGHTNESS POT CABLE ASSY C6482-140		1.0000
5	IN		270-3068- - -	12" CRT HARNESS ASSY D6482-139		1.0000
5	IN		270-3092- - -	YOKE ASSY (12" MONITOR) B6482-246		1.0000
5	IN		270-3104- - -	12"FLYBACK XFORMER HARN C6482-327	EC9723	1.0000
3	IN		270-0576- - -	2236 E WORK ST CHASSIS		1.0000
4	IN		220-1076- - -	POWER CORD ASSY(E CHAS)B6482-95		1.0000
4	IN		220-1101- - -	P054 WIRE&LUG ASSY(E CHAS)6482-12		1.0000
4	IN		220-1301- - -	CABLE SPEAKER 2236E B6482-462	E11322	1.0000
4	IN		220-1302- - -	CABLE POT B6482-466	E11322	1.0000
4	IN		270-3139- - -	TRANSFORMER HARNESS D6482-467	E11322	1.0000
3	WC		279-0352- - -	928 WK/ST COVER ASSY		1.0000
3	IN		279-1015- - -	928WZ BASE ASSY(ALUM TAPE) 6841-30		1.0000

MB0080-A M U L T I - L E V E L B I L L OF M A T E R I A L AS OF RUN DATE: 06/20/79

ASSEMBLY PART NUMBER 177-3236-DE- -
ASSEMBLY DESCRIPTION 2236DE WK/ST 80X24

POSITION IN STRUCTURE	LEGEND 1	2	3	COMPONENT PART NUMBER	DESCRIPTION	E C N	QUANTITY PER ASSY
1		IN		187-3236-DE- -	2236-DE INTERACTIVE TERM WK/ST		1.0000
2		IN		210-7592-A - -	PCA 2236E SINGLE BD TERM ELEC		1.0000
3		IN		209-7592- - -	PCA 2236E SINGLE BD TERM ELEC		1.0000
4		IN		220-1103- - -	CRT BRD (W2)(COAX)B6482-122	E11192	1.0000
2		IN		220-3039- - -	24 PIN FLAT CABLE ASSY(18")C6482-79		1.0000
2		IN		270-0579- - -	HEATSINK ASSY 2236E		1.0000
2	P	IN		279-0359- - -	2236E INTERACTIVE TERM COMMON ASSY		1.0000
3		IN		220-1143- - -	WIRE & LUG ASSY TYPE P065 D6482-12		1.0000
3		IN		270-0373- - -	12" MONITOR II & PWR SUP ASM II		1.0000
4		IN		270-0371- - -	POWER SUPPLY II,12" MONITOR(PRELIM)		1.0000
5	P	FS	*	210-7455- - -	PCA 9/12 MONITOR WANG MON PS REG		1.0000
6		IN		220-1107- - -	12" CRT POWER SUPLY CABLE B6482-141		1.0000
4		IN	*	270-0372- - -	12" MONITOR ASM II (LESS PWR SUP)		1.0000
5		IN	*	210-7456- - -	PCA 12" MONITOR ELEC	EC8373	1.0000
5		IN		220-0160- - -	BRIGHTNESS POT CABLE ASSY C6482-140		1.0000
5	P	IN		270-3068- - -	12" CRT HARNESS ASSY D6482-139		1.0000
5	P	IN		270-3092- - -	YOKE ASSY (12" MONITOR) B6482-246		1.0000
5	P	IN		270-3104- - -	12"FLYBACK XFORMER HARN C6482-327	EC9723	1.0000
3		IN		270-0576- - -	2236 E WORK ST CHASSIS		1.0000
4		IN		220-1076- - -	POWER CORD ASSY(F CHAS)B6482-95		1.0000
4		IN		220-1101- - -	P054 WIRE&LUG ASSY(E CHAS)6482-12		1.0000
4		IN		220-1301- - -	CABLE SPEAKER 2236E B6482-462	E11322	1.0000
4		IN		220-1302- - -	CABLE POT B6482-466	E11322	1.0000
4		IN		270-3139- - -	TRANSFORMER HARNESS D6482-467	E11322	1.0000
3		IN		279-1015- - -	928WZ BASE ASSY(ALUM TAPE) 6841-30		1.0000
3		IN		279-4116- - -	2236 DE COVER ASSY	E11811	1.0000

APPENDIX F

ELECTRICAL SCHEMATICS AND DRAWINGS

This appendix provides electrical schematics for the 2200MVP CPU, the 2236D Interactive Terminal, and the I/O controllers for the peripherals. Cable assembly drawings are also included. Below is a complete listing of the drawings provided.

DRAWING NUMBER	DESCRIPTION
2200MVP CENTRAL PROCESSING UNIT	
E6787	Data Memory (16K/32K x 9 Bits)
D7587	Data Memory (128K x 9 Bits)
E6788	Control Memory (8K/12K x 24 Bits)
E6789	Memory Control
E6790	Instruction Counter
E6791	Stack & Program Counter
E6792	ALU
E6793-1	Registers & I/O
D6797	Regulator (without Current Foldback)
D7397	Regulator (with Current Foldback)
E6798	MVP Motherboard
E7498	MVP-A Motherboard
D6482-125	MVP Transformer Harness
D6482-341	MVPA Transformer Harness
C6482-126	MVP Heatsink Harness
C6482-378	MVPA Heatsink Harness
E6819-100	MVP/MVPA Chassis
E6819-999	Interconnection Diagram
2236D INTERACTIVE TERMINAL	
D7067	Regulator (without current foldback)
D7156	Regulator (with current foldback)
E7158	Printer & Display I/O
E7292-1	CPU
D7293	Motherboard
D7256	12" Monitor Electronics (Wang)
B7258	Blanking CKT (Wang Monitor)
D7455	12" Monitor P.S. Reg. (Wang)
D7456	12" Monitor Electronics
7229	Wang Keyboard Electronics
6621-090	Keyboard & Bearing Plate
N/A	Motorola Video PCB Schematic
N/A	Motorola Interconnection Diagram
C35-1852	Keytronic Keyboard

DRAWING NUMBER	DESCRIPTION
	I/O CONTROLLERS
D6541-2	22C03 Disk Controller
D6561	22C01 Character Printer Controller
E6730	2227B Telecommunications Controller
E6786	2230MXB Multiplexer Slave Controller
D7042	22C11 Disk/Printer Controller
D7079	22C02 Matrix Printer Controller
E7141	2209A Tape Drive Controller (Motherboard)
E7142	2209A Tape Drive Controller (Daughterboard)
E7223	2227B/2228B Telecommunications Controller Motherboard
E7224	2228B Telecommunications Controller
E7287	2230MXA Multiplexer Controller
F7290-1	2236MXD Controller (Motherboard)
F7291-1	2236MXD Controller (Daughterboard)
D7342	22C11 Disk/Printer Controller
D7486	22C12 Disk Microprocessor (Motherboard)
D7487	22C12/22C13 Disk Microprocessor (Daughterboard)
D7488	22C13 Disk Microprocessor (Motherboard)
D7686	22C12 Disk Microprocessor (Motherboard)
D7688	22C13 Disk Microprocessor (Motherboard)
	I/O CABLE ASSEMBLIES
C6422-129	Printer Cable for 2221W Matrix Printer (WL #220-0105); for 2263 Chain Train Printer (WL #220-0105); for 2231W Matrix Printer (WL# 220-0105-1); for 2282 Graphic CRT (WL #220-0105-2)
C6472-61	I/O Cable Assembly for 2260B Series Drive (WL #220-0066); for 2270A-D Diskette Drive (WL #220-0066-4)
C6482-16	2224 Extension Cable for 2280 Phoenix Drive (WL #220-0138)
C6482-55	CP & Printer Cable for 2221M Printer MUX (WL #220-0130); for 2221M Printer MUX (WL #220-0131)

DRAWING NUMBER	DESCRIPTION
	I/O CABLE ASSEMBLIES (continued)
D6482-112	Inter-Disk Cable for 2260B-2 Disk Drive (WL #220-0151)
C6482-135	I/O Cable for 2271/2271P Writer & Plotter (WL #220-0156); for 2251 Matrix Printer (WL #220-0156)
C6482-143	I/O Cable for 2281/2281P Writer & Plotter (WL #220-0161)
D6482-165	I/O Cable for 2209A Tape Drive (WL #220-0168)
D6482-188	30 Pair Flat Cable for 2280 Phoenix Drive (WL #220-3032)
C6482-189	26 Conductor Shielded Cable for 2280 Phoenix Drive (WL #220-3033-5)
D6482-192	I/O Cable for 2261W Matrix Printer (WL #220-0171)
C6482-220	RS-232-C Cable for 2236D Terminal (WL #220-2236-25)
C6482-226	I/O Cable for 2201L Printer (WL #220-0181)
B6482-320	36 Conductor Cable for 2260BC Series Drives (WL #220-3066)

PROPERTY OF WANG AND SHALL NOT BE RE-COPIED OR USED AS A BASIS FOR MANUFACTURE OR SALE OF APPARATUS OR DEVICES WITHOUT PERMISSION.

DO NOT SCALE

HOLE LEGEND

	HOLE DIA.	TOL
DRILLED OR PUNCHED HOLE TOLERANCES	.0135 to .125	± .003
	.126 to .250	± .004
	.251 to .500	± .005

IDENT	DESCRIPTION	QTY.
A		

+5VR ⑫,⑭ ±0V

.1uf 50V C87 C88 C89 C90 C91 C92 C93 C94 C95 C96 C97

18uf 15V TA C98 C99 ⑮,⑯

18uf 15V TA C100 ⑮ +12.7V ±0V

74298 B1 QB A2 QC B2 QD C1 SD A3 SH C2 A4 D1 L93 D2 A1 A2 WS CLK

74295 D1 QD Q2 QC Q1 QA C2 QB B1 L95 B2 A2 WS CLK

74298 D1 WS A1 QD B1 QA C1 QB D2 QC A2 L96 B2 C2 CLK

L97 74175 L98 74175 L99 74175 L100 74175

R1 1K 5% +5VR

L98 74175 PR1 PR2 D1 D2 CK1 Q1 CK2 Q2 CLR1 CLR2

L90 74LS368 MAR CLK

L95 9321

L96 74175

L97 74175

L98 74175

L99 74175

L100 74175

R/W ⑪ R/W1 ⑪ R/W2 ⑪

L81 74LS368 L84 7400 L85 74LS368 L86 74LS368 L87 74LS368 L88 74LS368 L89 74LS368 L90 74LS368 L91 74LS368 L92 74LS368

L81 74LS368 L84 7400 L85 74LS368 L86 74LS368 L87 74LS368 L88 74LS368 L89 74LS368 L90 74LS368 L91 74LS368 L92 74LS368

CE ⑪ REF ⑬ DMS (1,2) ⑫

R33 10Ω 5% R34 10Ω 5% R35 10Ω 5% R36 10Ω 5% R37 10Ω 5% R38 10Ω 5% R9 10Ω 5% R10 10Ω 5%

C75 270pf C76 10Ω 5% 270pf C78 .1uf C79 270pf C80 270pf

MPS 3640 Q1 Q2 Q3 Q4

E 2A1A CX, BX, L10/75322 2V 1V Vcc2 CX2 BX2

L49/75322 E 1A 2A CX1 BX1

C73 18uf 15V C77 18uf 15V

+12V ⑤1 ±0V

L82 74175 L83 74175 L84 74175 L85 74175

L86 74175 L87 74175 L88 74175 L89 74175

R4 1K 5% +5VR

L39/TMS4050 L38/TMS4050 L37/TMS4050 L36/TMS4050 L35/TMS4050 L34/TMS4050 L33/TMS4050 L32/TMS4050 L31/TMS4050 L28/TMS4050 L27/TMS4050 L26/TMS4050 L25/TMS4050 L24/TMS4050 L23/TMS4050 L22/TMS4050 L20/TMS4050

L19/TMS4050 L18/TMS4050 L17/TMS4050 L16/TMS4050 L15/TMS4050 L14/TMS4050 L13/TMS4050 L12/TMS4050 L9/TMS4050 L8/TMS4050 L7/TMS4050 L6/TMS4050 L5/TMS4050 L4/TMS4050 L3/TMS4050 L2/TMS4050 L1/TMS4050

L87/TMS4050 L86/TMS4050 L85/TMS4050 L84/TMS4050 L83/TMS4050 L82/TMS4050 L52/TMS4050 L51/TMS4050 L48/TMS4050 L47/TMS4050 L46/TMS4050 L45/TMS4050 L44/TMS4050 L43/TMS4050 L42/TMS4050 L41/TMS4050 L40/TMS4050

L77/TMS4050 L76/TMS4050 L75/TMS4050 L74/TMS4050 L73/TMS4050 L72/TMS4050 L71/TMS4050 L70/TMS4050 L67/TMS4050 L66/TMS4050 L65/TMS4050 L64/TMS4050 L63/TMS4050 L62/TMS4050 L61/TMS4050 L60/TMS4050 L59/TMS4050

TYP. CAP. ON PINS 10 & 18 L1-9, L11-19 QTY. 18

TYP. CAP. ON PINS 10 & 18 L20-38, L39-59 QTY. 18

TYP. CAP. ON PINS 10 & 18 L40-48, L50-58 QTY. 18

TYP. CAP. ON PINS 1 & 18 L59-61, L70-79 QTY. 18

+12V ⑤1

.1uf 50V C1-C18

C81 270pf R11 10Ω 5%

.1uf 50V C19-C36

C82 270pf R12 10Ω 5%

.1uf 50V C37-C54

C83 270pf R13 10Ω 5%

C84 270pf R14 10Ω 5%

C85 15uf 15V TA

.1uf 50V C55-C72

C86 .1uf 15V TA

R15 2.2K 5% R16 2.2K 5% R17 2.2K 5% R18 2.2K 5% R19 2.2K 5% R20 2.2K 5% R21 2.2K 5% R22 2.2K 5% R23 2.2K 5% R24 2.2K 5% R25 2.2K 5% R26 2.2K 5% R27 2.2K 5% R28 2.2K 5% R29 2.2K 5% R30 2.2K 5% R31 2.2K 5% R32 2.2K 5% +5VR

L84 74175 L85 74175 L86 74175 L87 74175 L88 74175 L89 74175 L90 74175 L91 74175 L92 74175

74LS368 L79 74LS368 L80 74LS368 L81 74LS368 L82 74LS368 L83 74LS368 L84 74LS368 L85 74LS368 L86 74LS368 L87 74LS368 L88 74LS368 L89 74LS368 L90 74LS368 L91 74LS368 L92 74LS368

DIO DI1 DI2 DI3 DI4 DI5 DI6 DI7 DI8 DI9 DI10 DI11 DI12 DI13 DI14 DI15 DI16 DI17

DM00 DM01 DM02 DM03 DM04 DM05 DM06 DM07 DM08 DM09 DM010 DM011 DM012 DM013 DM014 DM015 DM016 DM017

±0V -5VR

E-KEY

REVISION	BY	DATE	APPROVED BY	DATE
ORIGINATED PER ECN #5362				
REVISED PER ECN #5362-11				
REVISED PER ECN #5362-12				
REVISED PER ECN #5362-13				
REVISED PER ECN #5362-14				
REVISED PER ECN #5362-15				
REVISED PER ECN #5362-16				
REVISED PER ECN #5362-17				
REVISED PER ECN #5362-18				
REVISED PER ECN #5362-19				
REVISED PER ECN #5362-20				
REVISED PER ECN #5362-21				

QTY	NAME	MATERIAL	DESCRIPTION

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL	MODEL NO 2400	DWN	
	SEE ENGRG SPECIFICATIONS	CHK	
FINISH	TOL EX AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG ± 1/30 FINISH	E. C. CONTROL	MFG ENGR
		TITLE 32K x 18 BIT DATA MEMORY	
		SCALE	SHT 1 OF 7
		SEE CHART 210-6757	SIZE E
		WANG PART NUMBER	DRAWING NUMBER 6757

F-5

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DO NOT SCALE

HOLE LEGEND		
	HOLE DIA	TOL
DRILLED OR PUNCHED HOLE TOLERANCES	0.125 to 125	± .002 ± .003 ± .004 ± .005
	.126 to .250	
	.251 to .500	

IDENT	DESCRIPTION	QTY.
A		

CONN.1

±0V	A 1	±0V
+5VR	B 2	+5VR
-5VR	C 3	-5VR
DI17	D 4	DI16
DI14	E 5	DI13
DI15	F 6	DI12
DM012	H 7	DM016
DM014	J 8	DM013
DM015	K 9	DM017
DM010	L 10	DM011
DM09	M 11	$\overline{CE}$
$\overline{RIW_2}$	N 12	DI11
DI10	P 13	DI9
RA3	R 14	PL4
+12.7V	S 15	+12.7V

SIGNAL - TERMINAL DESIGNATIONS; VIEW FROM BOTTOM WIRING SIDE OF CONNECTOR

CONN.3

PL5	A 1	RA4
PL6	B 2	PL3
PH5	C 3	RA2
PL2	D 4	RA5
RA0	E 5	PH6
PH4	F 6	PL1
PL7	H 7	RA1
PH3	J 8	PH1
PH2	K 9	PH0
$\overline{REF}$	L 10	DMS(1,2)
DM07	M 11	DM06
$\overline{RIW_1}$	N 12	DM08
DI7	P 13	DI8
$\overline{MARCLR}$	R 14	DI6
DI2	S 15	DI5
DI3	T 16	DI0
DI4	U 17	DI1
DM02	V 18	DM04
DM03	W 19	DM00
DM05	X 20	DM01
+5VR	Y 21	+5VR
±0V	Z 22	±0V

COMP. SIDE — WIRING SIDE

COMPONENT LAYOUT

6787 R5

LOCATION FOR 32K	W.L. NO.	TERM. FOR ±0V	TERM. FOR VCC +5VR
* L1-5, (11-19), (20-28), L31-39, L40-48, 50-67, L70-78	377-0314	18	
* (L10) 49	376-0178	7	14
L29, 30, 68, 69, L79-82, L89-92	376-0179	8	16
* L83, 84, (87) 88	376-0092	7	14
L85	376-0096	8	16
L86	376-0002	7	14
L93, 95, 96	376-0138	8	16
* (L1-5), (11-19), (L20-28), L31-39, L40-48, 50-67, L70-78	SOCKET 376-9014		
L94	376-0006	7	14

COMPONENT	W.L. NO.
R1	330-3010
R6	330-3011
* (R2, 3, 4, 5) T-14, 33-36	330-1011
R15-32	330-3023
* (C1-18) C37-54	300-1931
* (C19-36) C55-72 (C74) C75	300-1930
* (C75, 76) C78, 82 (C83), 84	300-1270
* (C73) 77, 85, 86, 98-100	300-4018
* (Q1, 2), 3, 4	375-1050

I.C. TYPE	LOCATION	SPARES
9321	L85	1

NOTE:
* DELETE ALL CIRCLED ITEMS FOR 16K VERSION

REVISION		
A	SEE ECN # FOR REV.	

WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
P/N	FIRST USED ON	ASSY USED ON	WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.		

	BY	DATE	APPROVED BY	DATE
DWN F.S.S.	2/27	E ENGR		
CHK		M ENGR		
E.C. CONTROL		MFG ENGR		

MATERIAL — MODEL NO 2600 — SEE ENGRG SPECIFICATIONS No. —

FINISH — TOL. XX AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG ± 1°30' FINISH

TITLE: SCHEMATIC LOGIBLOC 32K x 18 BIT MEMORY

SCALE — SHT 1 OF 7 — SEE CHART 210-6787 — E — 6787 — A

WANG PART NUMBER — SIZE — DRAWING NUMBER — REV.

E 2697

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DO NOT SCALE

PRELIMINARY

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY
MATERIAL	DWN FSS	12-8-78	E ENGR
	CHK		M ENGR
			MFG ENGR
MODEL NO. 2200 MVP (SEE ENGRG. SPECIFICATIONS)	TITLE 128K EXTENDER MEMORY		
FINISH	TOL. EX. AS NOTED .XX ± FRAC. ± .XXX ± ANG. ± FINISH √	210-7587	D 7587 4
	SCALE	SHT 1 OF 4	WANG PART NUMBER / SIZE / DRAWING NUMBER / REV.

REVISION	BY	DATE
SEE SH.4 FOR REV.		

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DO NOT SCALE

DMI17 (1F3) DMI16 (1F3) DMI15 (1F3) DMI14 (1F3) DMI13 (1F3) DMI12 (1F4) DMI11 (1F4) DMI10 (1F4) DMI9 (1F4)

AB00 (1F3)
AB01 (1F3)
AB02 (1E3)
AB03 (1E3)
AB04 (1E3)
AB05 (1E3)
AB06 (1E3)
DRAS0 (1A5)
DCAS0 (1B5)
R/W02 (1C3)

AB10 (1D3)
AB11 (1D3)
AB12 (1D3)
AB13 (1D3)
AB14 (1D3)
AB15 (1D3)
AB16 (1D3)
DRAS2 (1A5)
DCAS2 (1B5)
R/W02 (1C3)

AB20 (1C3)
AB21 (1C3)
AB22 (1C3)
AB23 (1C3)
AB24 (1B3)
AB25 (1B3)
AB26 (1B3)
DRAS4 (1A5)
DCAS4 (1B5)
R/W12 (1B1)

AB30 (1C1)
AB31 (1C1)
AB32 (1C1)
AB33 (1C1)
AB34 (1B1)
AB35 (1B1)
AB36 (1B1)
DRAS6 (1A5)
DCAS6 (1C5)
R/W12 (1B1)

DO17 (1D2) DO16 (1D2) DO15 (1D2) DO14 (1D2) DO13 (1E2) DO12 (1E2) DO11 (1E2) DO10 (1E2) DO9 (1E2)

PRELIMINARY

NO.	REVISION	BY	DATE
	SEE SH. 4 FOR REV.		

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	FSS	12-8-78	E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO. 2200MVP

SEE ENGR. SPECIFICATIONS

No.

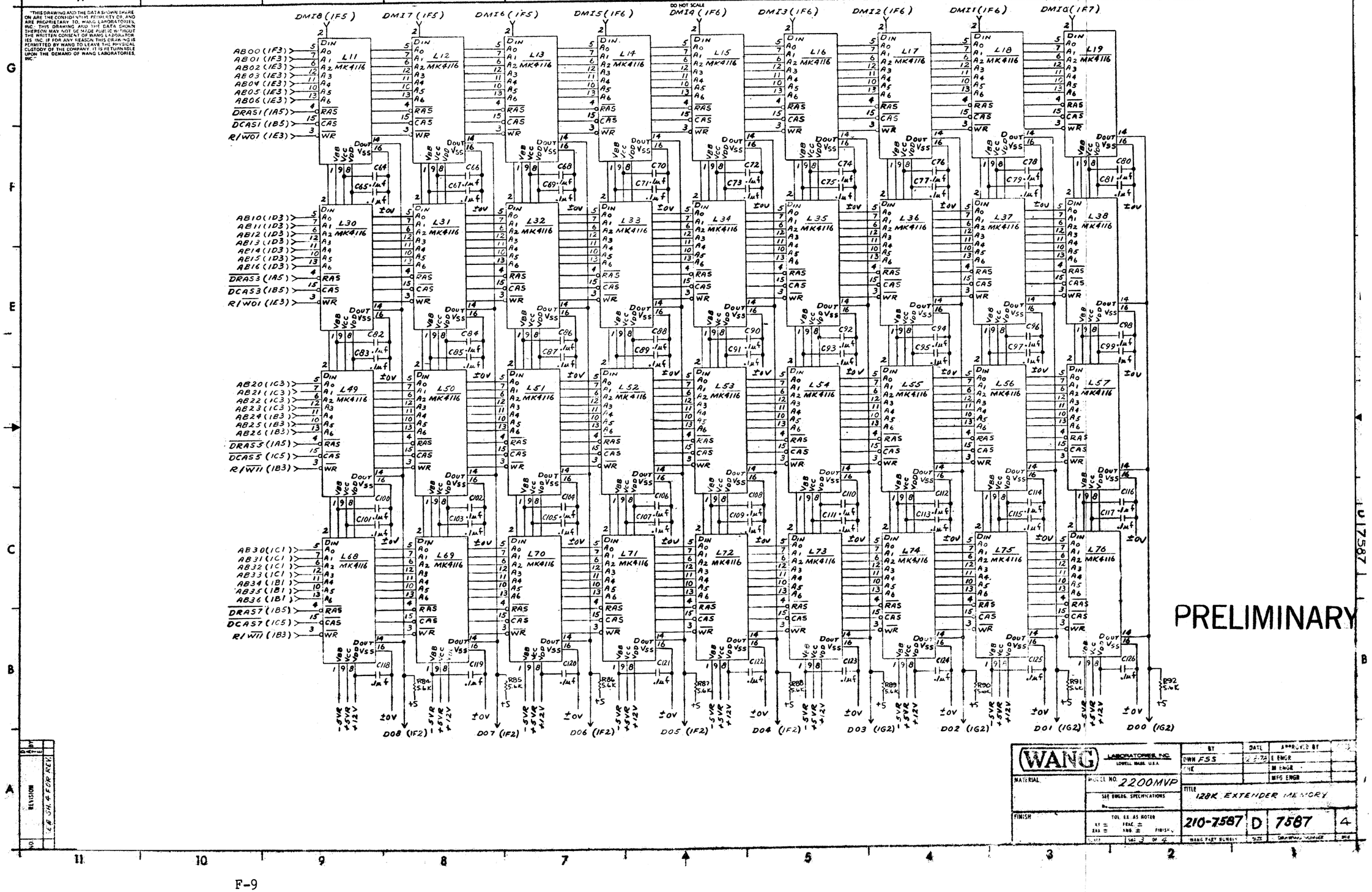
TITLE 128K EXTENDER MEMORY

FINISH

TOL EX. AS NOTED
XX ± FRAC. ±
XXX ± ANG. ± FINISH √

SCALE	SHT 2 OF 4	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
		210-7587	D	7587	4

D 7587


DMI8 (IF5)
DMI7 (IF5)
DMI6 (IF5)
DMI5 (IF6)
DMI4 (IF6)
DMI3 (IF6)
DMI2 (IF6)
DMI1 (IF6)
DMI0 (IF7)
AB00 (IF3)
AB01 (IF3)
AB02 (IE3)
AB03 (IE3)
AB04 (IE3)
AB05 (IE3)
AB06 (IE3)
DRAS1 (IA5)
DCAS1 (IB5)
R/W01 (IE3)
AB10 (ID3)
AB11 (ID3)
AB12 (ID3)
AB13 (ID3)
AB14 (ID3)
AB15 (ID3)
AB16 (ID3)
DRAS3 (IA5)
DCAS3 (IB5)
R/W01 (IE3)
AB20 (IC3)
AB21 (IC3)
AB22 (IC3)
AB23 (IC3)
AB24 (IB3)
AB25 (IB3)
AB26 (IB3)
DRAS5 (IA5)
DCAS5 (IC5)
R/W11 (IB3)
AB30 (IC1)
AB31 (IC1)
AB32 (IC1)
AB33 (IC1)
AB34 (IB1)
AB35 (IB1)
AB36 (IB1)
DRAS7 (IB5)
DCAS7 (IC5)
R/W11 (IB3)
L11 MK4116
L12 MK4116
L13 MK4116
L14 MK4116
L15 MK4116
L16 MK4116
L17 MK4116
L18 MK4116
L19 MK4116
L30 MK4116
L31 MK4116
L32 MK4116
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L73 MK4116
L74 MK4116
L75 MK4116
L76 MK4116
DO8 (IF2)
DO7 (IF2)
DO6 (IF2)
DO5 (IF2)
DO4 (IF2)
DO3 (IG2)
DO2 (IG2)
DO1 (IG2)
DO0 (IG2)
DO NOT SCALE
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PRELIMINARY
WANG LABORATORIES, INC. LOWELL MASS. U.S.A.
MODEL NO. 2200MVP
TITLE 128K EXTENDER MEMORY
210-7587 D 7587 4

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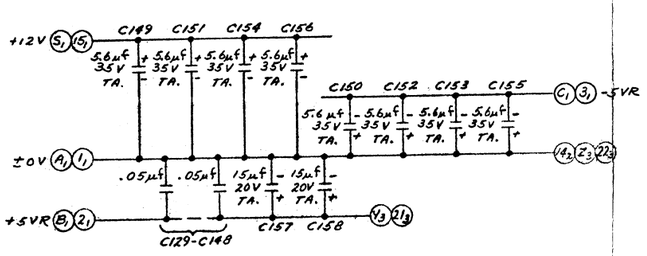
DO NOT SCALE

I.C. LOCATION	TYPE	W.L. NO.
L1-11-28, 30-47, 49-66, 68-76	MK4116-N3	SEE CHART
L10, 29, 48, 67	74LS240	SEE CHART
L77, 79, 86	74367	376-0176
L78, 80, 87	8T97	376-0189
L81	9321	376-0096
L82	74LS244	376-0288
L83, 90	7408	376-0081
L84, 96	74298	376-0138
L85, 97	74174	376-0098
L88, 98	7404	376-0010
L89	7403	376-0028
L91	74S32	376-0205
L92	74S37	376-0296
L93	1519-100B	376-8002
L94, 95	74157	376-0082
L1-9, 11-28, 30-47, 49-66, 68-76	16 PIN SKT. LOAD PER CHART	376-9002

LOCATION	TYPE	SPARES
L88	7404	1
		1
L90	7408	2

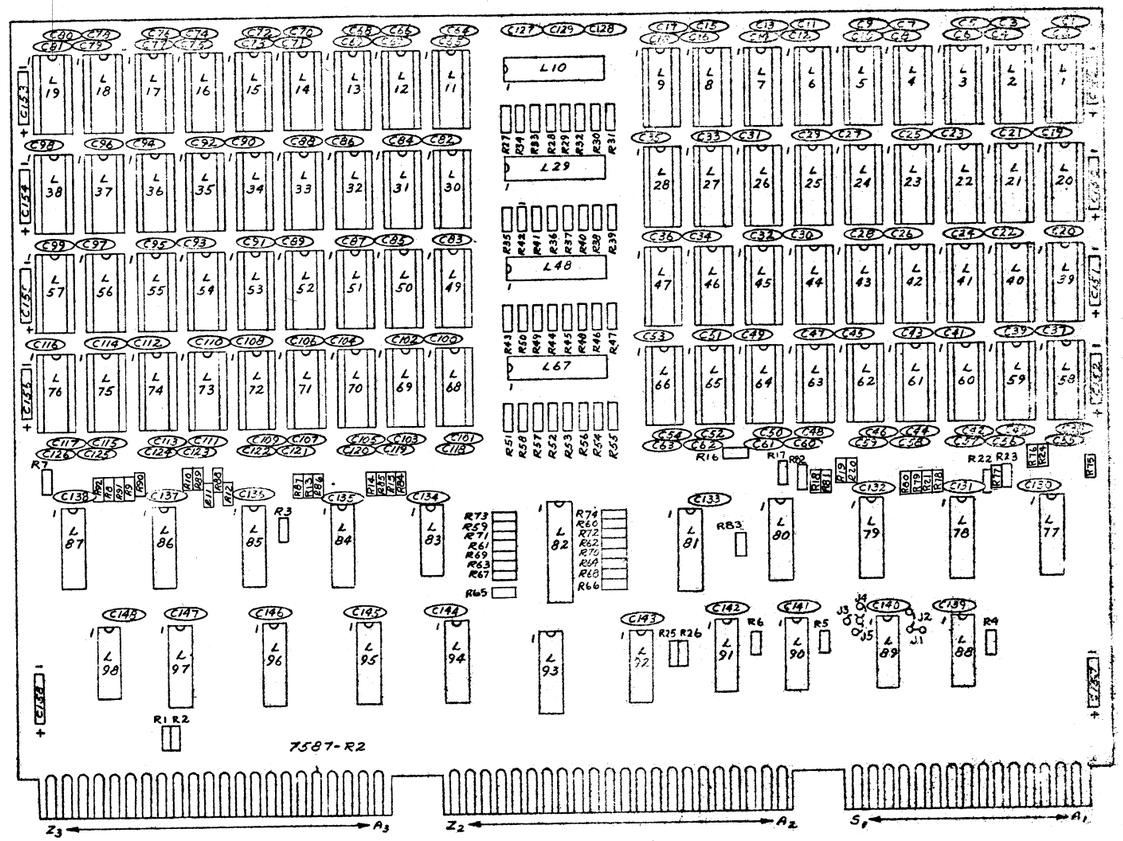
COMPONENT	TYPE	W.L. NO.
R1-5	2.2K 10% 1/4W	330-3022
R6	330Ω 10% 1/4W	330-2039
R7-24	180Ω 10% 1/4W	330-2018
R25	150Ω 10% 1/4W	330-2015
R26	330Ω 10% 1/4W	330-2033
R27-74	56Ω 10% 1/4W	SEE CHART
R75-92	5.6K 10% 1/4W	330-3056
C1-126	.1μf 50V	300-1930
C127,128	330pf 500V (C)	300-1330
C129-148	.05μf 12V	300-1900
C149-156	5.6μf 35V TA.	300-4017
C157,158	15μf 20V TA.	300-4022

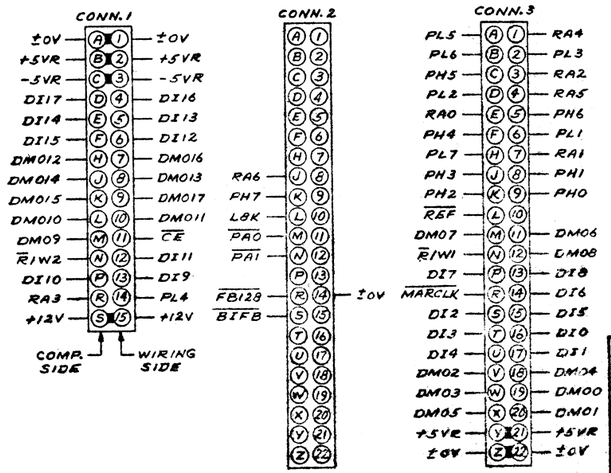
MNEMONIC	COORDINATE
$\overline{BIFB}$	1G9
$\overline{CE}$	1G8
DI0-DI17	1G6
DM00-DM17	1G1
$\overline{FB128}$	1G9
LBK	1G11
$\overline{MARCLK}$	1G10
$\overline{PA0}$-$\overline{PA1}$	1F11
PH0-PH7	1D11
PL1-PL7	1C11
RA0-RA6	1C11
$\overline{REF}$	1E11
$\overline{RIW1}$-$\overline{RIW2}$	1G7



MODEL	209	210	L1-9 L11-19	L20-28 L30-38	L39-47 L49-57	L58-66 L68-76	L10	L29	L48	L67	R27-33 R65,66, R73,74	R34-42 R63,64, R71,72	R43-49 R61,62, R69,70	R50-60 R67,68
2200MVP 32K	7587	7587-A				377-0345			376-0297	376-0297				330-1056
2200MVP 64K	7587-1	7587-1A			377-0345	377-0345			376-0297	376-0297			330-1056	330-1056
2200MVP 96K	7587-2	7587-2A		377-0345	377-0345	377-0345	376-0297	376-0297	376-0297	376-0297		330-1056	330-1056	330-1056
2200 MVP 128K	7587-3	7587-3A	377-0345	377-0345	377-0345	377-0345	376-0297	376-0297	376-0297	376-0297	330-1056	330-1056	330-1056	330-1056

NO	REVISION	BY	DATE	APPROVED
1/0	ORIGINATED PER ECN#9305 APPD. [illegible]	FSS	12-8-78	
1/1	REVISED PER ECN#9305 ADDED [illegible]	FSS	12-8-78	
1/2	REVISED PER ECN#9305 ADDED [illegible]	FSS	12-9-78	
1/3	REVISED PER ECN#9305 ADDED [illegible]	FSS	12-20-78	
1/4	REV. PER ECN 10485, JOB 22,1035 APPD:	JB	5-10-79	





PRELIMINARY

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY	DATE
	L.W. FSS	12-8-78	E ENGR.	
	CHK		M ENGR	
MATERIAL	MODEL NO. 2200MVP SEE ENGRG. SPECIFICATIONS		MFG ENGR	
FINISH	TOL. EX. AS NOTED .XX ± .XXX ± FRAC ± ANG ± FINISH √	TITLE 128K EXTENDER MEMORY		
	SCALE 1/4 SHT 4 OF 4	WANG PART NUMBER 210-7587	SIZE D	DRAWING NUMBER 7587 REV 4

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DO NOT SCALE

COMPONENT LAYOUT

*NOT LOADED FOR 8K VERSION

COMPONENT	W.L. PART NO.
* R1-8, 11, 12, 38-41, 43, 44	330-1011
R9, 14-37	330-3023
* C1-12, 25-36, 49-60	300-1931
* C13-24, 37-48, 61, 62, 82, 86, 93, 94-101	300-1930
* C73-75, 77, 78, 81, 84, 85, 88, 89, 90, 91, 92, 95	300-1270
* C76, 80, 83, 87, 103, 102, 103	300-4018
* Q1, 2, 3, 4, 5, 6	375-1050

* DELETE ALL CIRCLE ITEMS FOR 8K VERSION

LOCATION	W.L. PART NO.	±0V	Vcc 5VR
* L1-6, 10-33, 37-54, 55-60, 64-80	377-0314	18	
* L7, 34, 61, 62, 63, 89, 90, 91, 92, 93	376-0177	8	16
* L8, 35, 62	376-0178	7	14
L86	376-0002	7	14
L87	376-0003	7	14
L89	376-0016	7	14
* L1-6, 10-33, 37-54, 55-60, 64-80	376-9014		

2. ALL OTHER CHIPS ARE 7400 SERIES UNLESS OTHERWISE SPECIFIED.
1. ALL MEMORY CHIPS ARE TMS 4050.

NOTES

REVISION	BY	DATE	APPROVED BY	DATE
1 REVISED PER RFA-1914 APP'D BY USA		3-8-76		
2 REVISED PER RFA-1976 APP'D BY MCB		4-27-76		
3 REVISED PER ECO 1344 APP'D BY MCB		6-22-76		
4 REVISED PER ECO 1385 APP'D BY MCB		8-16-76		
5 REVISED PER ECO 1407 APP'D BY MCB		9-28-76		
6 REVISED PER ECO 1417 APP'D BY MCB		10-14-76		
7 REVISED PER ECO 1437 APP'D BY MCB		10-27-76		

	BY	DATE	APPROVED BY	DATE
DWN				
CHK				
E C CONTROL				

QTY	NAME
	WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.
MATERIAL	MODEL NO 2600
	SEE ENGRG SPECIFICATIONS
FINISH	TOL EX AS NOTED .XX ± .010 FRAC ± 1/64 .XXX ± .005 ANG ± 1°30' FINISH
SCALE	SHT OF

TITLE SCHEMATIC LOGIBLOC 8K/16K X 24 BIT MEMORY BOARD

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
210-6788	E	6788	7

E-REV 2

E 6788

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DO NOT SCALE

HOLE LEGEND

	HOLE DIA.	TOL
DRILLED OR PUNCHED HOLE	.0135 to .125	± .003
	.126 to .250	± .004
TOLERANCES	.251 to .500	± .005
		etc.

IDENT	DESCRIPTION	QTY.
A		

NOTE: ALL I.C. CHIPS ARE 7400 SERIES UNLESS OTHERWISE SPECIFIED.

COMPONENT	W.L. PART NO.
R1-11	330-3010
C1-22	300-1900
C23,24	300-4022
J1	376-9002
L27-29	376-9003

LOCATION	TYPE	SPARES
L1	74S08	1
L4	74S02	1
L6	T432	2
L7	T474	1
L12	74S51	1
L14	74S00	3
L18	7404	2
L19	7410	2
L30	74S04	2
L41	T432	5

LOCATION	W.L. PART NO.	±0V	+5VR
L1	376-0200	7	14
L2,7,9,11	0006	7	14
L3,42	0201	7	14
L4	0199	7	14
L5,10	0012	7	14
L6,41	0093	7	14
L8,12	0184	7	14
L13,18	0010	7	14
L14	0228	7	14
L16	0081	7	14
L17,19	0003	7	14
L15,20,25,26,31	0246	7	14
L21-24	376 0138	8	16
L27-29	377-0317	12	24
L30	376 0197	7	14
L32-35	0224	8	16
L36,37	0098	8	16
L38-40	376-0094	8	16

210:209 + 377 OR 378

MODEL	209	210	L27	L28	L29
2200 VP	6789	6789-B	378-2174	378-2175	378-2176
2200 VP	6789	6789-C	378-2156	378-2157	378-2158
2200 VP	6789	6789-D	378-2187	378-2188	378-2189
2200 VP	6789	6789-E	378-2204	378-2205	378-2206
2200 VP	6789	6789-F	378-2207	378-2208	378-2209
2200 VP	6789	6789-G	378-2225	378-2226	378-2227
2200 VP	6789	6789-A	378-2045 R2	378-2046 R2	378-2047 R2

SIGNAL TERMINAL DESIGNATIONS, VIEW FROM BOTTOM (WIRING) SIDE OF THE CONNECTOR

REVISION	BY	DATE	APPROVED BY	DATE
ORIG. PER DWR # 6062				
REVISED PER ECN # 2214				
REVISED PER ECN # 5765				
REVISED PER ECN # 6789				
REVISED PER ECO # 7111				
REVISED PER ECO # 7111				
REVISED PER ECO # 7111				
REVISED PER ECO # 7111				
REVISED PER ECO # 7111				
REVISED PER ECO # 7111				

WANG PART NO.	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
P/C ASY FIRST USED ON	ASSY USED ON				

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	R.A.	10/7/75	E ENGR J.C.D.	1/12/76
CHK	G.D.	1-21-76	M ENGR	
E.C. CONTROL			MFG ENGR	

MATERIAL — MODEL NO. 2200VP — SEE ENGNG SPECIFICATIONS No.

FINISH — TOL. EX. AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG ± 1°30' FINISH

TITLE: MEMORY CONTROL

210-6789 | E | 6789 | 8

SCALE — SHT — OF — WANG PART NUMBER — SIZE — DRAWING NUMBER — REV.

E-REV 0

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DO NOT SCALE

HOLE LEGEND

DRILLED OR PUNCHED HOLE TOLERANCES	HOLE DIA	TOL
	.0135 to .125	± .001
	.126 to .250	± .002
	.251 to .500	± .003

IDENT	DESCRIPTION	QTY
A		

CONN. 1

10V	A 1	10V
+5VR	B 2	+5VR
R_{22}	C 3	R_{18}
R_{21}	D 4	R_{20}
$\overline{R/W}$	E 5	$\overline{LPA}$
$\overline{TAP}$	F 6	$\overline{TSP}$
$\overline{WPB}$	H 7	$\overline{PCCC}$
PINC	J 8	$\overline{LPI}$
XOP	K 9	CNTD
$\overline{LLPC}$	L 10	$\overline{LHPC}$
T_3	M 11	T_7
T_4	N 12	T_{12}
T_{16}	P 13	T_1
	R 14	
	S 15	

CONN. 2

$\overline{T_5}$	A 1	$\overline{T_9}$
$\overline{REC}$	B 2	DMPI
MS_3	C 3	PEDM
MS_2	D 4	CA_5
MS_1	E 5	CA_2
CA_0	F 6	CA_4
CA_1	H 7	CA_3
RA_2	J 8	RA_4
RA_1	K 9	BRANCH
T_{15}	L 10	RA_3
CA_7	M 11	CA_6
CA_{11}	N 12	CA_8
CA_9	P 13	CA_{10}
RA_7	R 14	RA_5
RESET	S 15	REC CLK
$\overline{MS_4}$	T 16	$\overline{MS_5}$
LOP	U 17	$\overline{MS_6}$
$\overline{B}$	V 18	PECM
POR	W 19	$\overline{SB}$
ROMS	X 20	R_9
R_{11}	Y 21	$\overline{SR}$
R_8	Z 22	SWITCH

CONN. 3

S_6	A 1	R_6
ICC_3	B 2	ICC_{15}
S_7	C 3	ICC_{14}
R_7	D 4	ICC_{13}
R_5	E 5	ICC_{12}
R_6	F 6	R_{16}
MARCLK	H 7	S_8
ICC_{10}	J 8	ICC_{11}
ICC_9	K 9	ICC_9
R_{14}	L 10	R_{17}
S_2	M 11	S_1
ICC_6	N 12	ICC_7
ICC_5	P 13	ICC_2
ICC_4	R 14	ICC_8
S_3	S 15	ICC_1
R_3	T 16	R_2
R_{15}	U 17	S_4
S_5	V 18	R_{12}
R_{13}	W 19	R_{19}
$\overline{MS5}$	X 20	$\overline{MS8}$
+5VR	Y 21	+5VR
10V	Z 22	10V

COMP SIDE — WIRING SIDE

SIGNAL TERMINAL DESIGNATIONS, VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

I.C. TYPE	LOCATION	SPARE
7902	L2	1
74502	L35	2
79502	L42	1
7408	L9	1
79511	L41	2
7932	L5	2
	L31	1
79532	L43	2
74508	L12A	1
	L47	1
7402	L20	1
7404	L13	2
	L16	2
7474	L46	1
74508	L49	1
7404	L40	1

I.C. LOCATION	W.L. PART No.	PIN NO 10V	PIN NO +5VR
L1, 46, 29A	376-0006	7	14
L2	376-0125	7	14
L3, 20	376-0002	7	14
L4, 8, 51	376-0008	8	16
L5, 14, 31	376-0093	7	14
L6	376-0016	7	14
L7, 24	376-0003	7	14
L9, 15	376-0081	7	14
L10, 11, 12, 23, 27, 33, 36	376-0098	8	16
L13, 16, 40	376-0010	7	14
L17, 18, 27, 28, 29	376-0203	8	16
L19, 45	376-0004	7	14
L25, 26	376-0057	7	14
L30	376-0126	1	8
L32	376-0238	7	14
L34, 37, 52	376-0201	7	14
L38, 48	376-0082	8	16
L39, 50	376-0011	10	5
L41	376-0237	7	14
L42, 35	376-0199	7	14
L43	376-0205	7	14
L44, 53, 55, 56	376-0034	8	16
L47, 54, 12A	376-0200	7	14
L48	376-0197	7	14
L18A	376-0176	8	16

COMPONENT	W.L. PART No.
R1, 4-13	330-3070
R2	330-2039
R3	330-3022
E-S BAR	654-0517
C1, 3,	300-1903
C2	340-5006
C5, 28	300-4022
C6 THRU 27	300-1900
J1	376-9005
C4	300-1909

J1

IC_{14}	A 7	IC_0
IC_{16}	B 11	IC_1
IC_{13}	C 10	IC_2
IC_{12}	D 9	IC_3
IC_{11}	E 8	IC_4
IC_{10}	F 6	IC_5
IC_9	H 5	IC_6
IC_8	J 4	IC_7

COMPONENT LAYOUT

6790 R11

E-REV 7

REVISION	DRWN	CHK	E.C. NO.	E.C.K.	I.I.	I.S.
A	DENVER ECO DWR 6790	11-2-76	11-26	11-27-76	10-9-76	10-9-76
B	REVISED ECO ECN M 8950 AMD W.C.Q.	11-26-76	11-26	11-27-76	11-10-76	11-10-76
C	REVISED PER ECO M 8950 AMD W.C.Q.	11-26-76	11-26	11-27-76	11-10-76	11-10-76
D	REVISED PER ECO M 8950 AMD W.C.Q.	11-26-76	11-26	11-27-76	11-10-76	11-10-76
E	REVISED PER ECN M 8950 AMD W.C.Q.	11-26-76	11-26	11-27-76	11-10-76	11-10-76
F	REVISED PER ECN M 8950 AMD W.C.Q.	11-26-76	11-26	11-27-76	11-10-76	11-10-76
G	REVISED PER ECN M 8950 AMD W.C.Q.	11-26-76	11-26	11-27-76	11-10-76	11-10-76
H	REVISED PER ECN M 8950 AMD W.C.Q.	11-26-76	11-26	11-27-76	11-10-76	11-10-76
I	REVISED PER ECN M 8950 AMD W.C.Q.	11-26-76	11-26	11-27-76	11-10-76	11-10-76
J	REVISED PER ECN M 8950 AMD W.C.Q.	11-26-76	11-26	11-27-76	11-10-76	11-10-76

WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
DASH NO. / FIRST USED ON	ASSY USED ON				

WANG LABORATORIES, INC. BILLERICA, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN			E ENGR	
CHK			M ENGR	
E C CONTROL			MFG ENGR	

MATERIAL

FINISH

MODEL NO 2200VP

SI ENGRG SPECIFICATIONS

TOL EX. AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG ± 1/2° FINISH

SCALE — SHT 1 OF 1

TITLE SCHEMATIC, INSTRUCTION COUNTER, BOARD

210-6790 | E | 6790 | 12

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.

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DO NOT SCALE

HOLE LEGEND

	HOLE DIA.	TOL
DRILLED OR PUNCHED HOLE TOLERANCES	.0135 to .125	± .001
	.126 to .250	± .002
	.251 to .500	± .005

IDENT	DESCRIPTION	QTY.
A		

LOCATION	WL PART No.	-10V	Vcc +5VR
L21 A	376-0125	7	14
L1,2	376-0053	8	16
L3,4	0082	8	16
L5-12	0254	8	16
L13,54,55	0093	7	14
L14,35	0002	7	14
L15, 24,53,58	0006	7	14
L17-20,49-52,60-63	0048	8	16
L21,22,31	0010	7	14
L23,34	0197	7	14
L25,45	0228	7	14
L26,36,12	0003	7	14
L27-30,38-41	0203	8	16
L32	0016	7	14
L33	0194	7	14
L37	0004	7	14
L43	0081	7	14
L44	0260	7	14
L46,47	0031	7	14
L48,59	0098	8	16
L56	0008	8	16
L57	376-0247	8	16
L16	376-0202	7	14
L5-12	376-9002		

COMPONENT	W.L. PART NO.
R1-8	330-3010
C1-26	300-1900
C27,28	300-4022
R9,10	330-3022
BUS BAR	654-0516

LOCATION	TYPE	SPARES
L13	7432	1
L15	7474	1
L22	7404	1
L23	74S04	2
L25	74S00	3
L31	7404	3
L21A	7427	1
L34	74S04	1
L36	7410	1
L44	74S08	1
L53	7474	1

1. ALL I.C. CHIPS ARE 7400 SERIES UNLESS OTHERWISE NOTED.

NOTES

SIGNAL-TERMINAL DESIGNATIONS, VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

COMPONENT LAYOUT

E-REV

REVISION	BY	DATE	APPROVED BY	DATE
ENG # 6124 DWG # 6791				
ECN # 5791 REVISED PER ECN # 5963				
REVISED PER ECN # 6043				
REVISED PER ECN # 6124				
REVISED PER ECN # 6791				

WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
FIRST USED ON	ASSY USED ON				

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

			DWN	E ENGR W. C.	7/1/76
			CHK G.D.	9-7-76 M ENGR	
MATERIAL	MODEL NO 2200VP		E C CONTROL	MFG ENGR	
	SEE ENGRG SPECIFICATIONS for		TITLE SCHEMATIC LOGIC-DC STACK & PROGRAM COUNTER		
FINISH	TOL. EX. AS NOTED .XX ± .010 FRAC. ± 1/64 .XXX ± .005 ANG. ± 1/2° FINISH		JD-6791	E	6791 .B
	SCALE	SHT 1 OF 1	WANG PART NUMBER	SIZE	DRAWING NUMBER REV.

E 6791

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DO NOT SCALE

HOLE LEGEND

SYMBOL	HOLE DIA.	TOL.
DRILLED OR PUNCHED HOLE	.0135 to .125	±.002
TOLERANCE:	.126 to .250	±.003
	.251 to .260	±.005

QUANT.	DESCRIPTION	QTY.
A		

SIGNAL-TERMINAL DESIGNATIONS, VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

CONN.1

±0V	A 1	1	±0V
+5VR	B 2	2	+5VR
.	C 3	3	.
R22	D 4	4	R16
R21	E 5	5	R20
T4	F 6	6	TP7
TP3	H 7	7	TP2
TCMDR	J 8	8	.
TP10	K 9	9	LPI
TP5	L 10	10	TP1
T1	M 11	11	ROM3
T3	N 12	12	T12
T4	P 13	13	T16
T14	R 14	14	T1
	S 15	15	

CONN.2

T6	A 1	1	T5
REF	B 2	2	T9
T10	C 3	3	T11
T14	D 4	4	T13
T15	E 5	5	BRANCH
PL4	F 6	6	ABUS7
C7	H 7	7	SH0
PL5	J 8	8	CA
C6	K 9	9	CEN
PH7	L 10	10	BLK-CA
C5	M 11	11	C4
PL3	N 12	12	C3
PL6	P 13	13	REFCLK
C2	R 14	14	PH5
C1	S 15	15	PL2
CE	T 16	16	C0
ABUS6	U 17	17	ABUS5
PL1	V 18	18	ABUS4
ALUCLK	W 19	19	SR
ABUS2	X 20	20	ABUS1
ABUS3	Y 21	21	R6
PH6	Z 22	22	R1

CONN.3

PL7	A 1	1	R8
ABUS8	B 2	2	PH4
R7	C 3	3	PH1
STOP	D 4	4	B7
PH3	E 5	5	B6
MARCLK	F 6	6	R16
TP6	H 7	7	B5
B3	J 8	8	B4
B1	K 9	9	B2
B0	L 10	10	TP4
R4	M 11	11	ZDCLK
R5	N 12	12	R19
DI7	P 13	13	DIP
DI2	R 14	14	DI6
DI3	S 15	15	DI5
PL8	T 16	16	DI4
R15	U 17	17	DI1
R3	V 18	18	R2
R14	W 19	19	DI0
PH2	X 20	20	PH0
+5VR	Y 21	21	+5VR
±0V	Z 22	22	±0V

COMP SIDE — WIRING SIDE

COMPONENT	W.L. PART NO.
R1,2	330-2047
BUS BAR	654-0674
B3-37	330-3010
C1	300-1105
C2-31	300-1900
C32,33	300-4022
XTAL	321-0020
L9	376-9002
R38	330-5032

LOCATION	TYPE	SPARES
L1	7404	1
L6	74367	2
L10	7408	2
L11	7408	4
L8	74S10	1
L16	7402	2
L25	74502	1
L30	74S04	2
L31	7408	2
L32	74300	3
L38	74 32	3
L66	74S11	1

BUS BAR

6792 R0

COMPONENT LAYOUT

NOTE: ALL CHIPS ARE 7400 SERIES UNLESS OTHERWISE SPECIFIED.

LOCATION	W.L. PART NO.	±0V	+5VR
L1,4,5,9,10,17,18,19,20,21,22,23,70,71	376-0006	7	14
L2,61,69	376-0010	7	14
L3,67	376-0008	8	16
L4,5,6	376-0176	8	16
L7,45,46	376-0052	8	16
L8,36,37,63	376-0228	7	14
L9	376-9346	8	16
L10,26,28	0200	7	14
L11,30,38	0197	7	14
L12,13,39,148	0202	7	14
L14,62	0094	8	16
L15,55	0237	7	14
L16	0206	7	14
L17,24	0205	7	14
L18	0016	7	14
L19,20	0258	18	24
L81,82	0201	7	14
L25	01399	7	14
L26,42,43,44	0252	8	16
L29	0217	8	16
L31	0081	7	14
L32,60A,63-66	0218	7	14
L33	0036	7	14
L34,35	0018	12	5
L38	0093	7	14
L47,48,60,61	0204	8	16
L50,51	0102	7	14
L58	0253	8	16
L59	0252	8	16
L68	0198	7	14
L72,73	0119	8	16
L74	376-0246	7	14

C2-31 .01µf

(2) 15µf, 10V (T)

REV.	REVISION	BY	CHK	APPD	DATE
0	ORIGINAL RELEASE				
A	ECN 6792-123				
B	ECN 6792-174				
C	ECN 6792-208				
D	ECN 6792-244				
E	ECN 6792-274				
F	ECN 6792-304				
G	ECN 6792-344				
H	ECN 6792-374				
J	ECN 6792-404				
K	ECN 6792-434				
L	ECN 6792-464				
M	ECN 6792-494				
N	ECN 6792-524				
P	ECN 6792-554				
R	ECN 6792-584				

WANG PART NO.	ITEM	QTY.	NAME

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL

FINISH

MODEL NO 2600

SEE ENGRG SPECIFICATIONS No.

TOL. EX AS NOTED .XX ± .010 FRAC ± 1/64 .XXX ± .005 ANG. ± 1°30' FINISH √

SCALE 1/1 SHT 1 OF 1

MATERIAL	DESCRIPTION
BY	DATE
DWN CK	9-3-76
CHK G.D.	9-7-76
E C CONTROL	
MFG ENGR	

APPROVED BY: E ENGR M.SG. 9/7/76; M ENGR

TITLE SCHEMATIC LOGIBLOC ALU

210-6792 | E | 6792 | $11

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.

E-REV. S

F 6792

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DO NOT SCALE

HOLE LEGEND		
DRILLED OR PUNCHED HOLE TOLERANCES	HOLE DIA.	TOL.
	.0135 to .125	±.003
	.126 to .250	±.004
	.251 to .500	±.005

IDENT	DESCRIPTION	QTY.
A		

L2 THRU L9 TO BE FAIRCHILD ONLY.

6793 R6

LOAD FOR 6793-1 ONLY. SEE 6793-1 CHART BELOW

COMPONENT LAYOUT

COMPONENT	W.L. PART NO.
R1-18,22-28,30	330-3010
R19,20,21,29	330-4034
C1,2,3,5	300-5005
C4, C41	300-1330
C6-38	300-1900
C39,40	300-4022

6793-1 CHART

COMPONENT	W.L. NO.
L10A	376-0080
R31	330-3010
R32	333-0081
R33	333-0080
C42	300-4016
D1	380-1001

LOCATION	W.L. PART NO.	TERM. NO. 10V	TERM. NO. VCC+5VR
L13,14,50,54,61	376-0119	8	16
L2-9	-0100	8	16
L16,39	-0010	7	14
L11,32,41,52	-0125	7	14
L12,29,38	-0194	7	14
L15,31	-0093	7	14
L14	-0238	7	14
L17-19,21,23,47	-0006	7	14
L20,28,40,42	-0002	7	14
L22,24	-0080	8	16
L25	-0012	7	14
L26,35-37,58,60	-0192	8	16
L27	-0096	8	16
L30	-0031	7	14
L33,43,45,55	-0041	8	16
L46,48	-0097	8	16
L49,51,57,59	-0204	8	16
L53	-0200	7	14
L56	-0098	8	16
L62	376-0016	7	14
J1,J2	376-3012		
L10	376-0197	7	14
L2-9	376-9002	16PIN SOCKET	
BUS BAR	654-0516	QTY. 1	

LOCATION	TYPE	SPARES
L16	7404	1
L19	7474	1
L39	7404	1
L52	7427	2
L60	74LS367	2
L62	7402	1
L14	74S10	1

SIGNAL-TERMINAL DESIGNATIONS, VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

WANG PART NO.	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
ON ITEM	FIRST USED ON	ASSY USED ON			

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL

FINISH

MODEL NO. 2200 MVP

SEE ENGRG SPECIFICATIONS

TOL. EX. AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG. ± 1° 30' FINISH √

SCALE - WG. SHT 1 OF 1

	BY	DATE	APPROVED BY	DATE
DWN	G.K.	1-27-76	ENGR	
CHK	G.D.	9-30-76	M. ENGR	
E.C. CONTROL			MFG ENGR	

TITLE SCHEMATIC LOGIBLOC REGISTERS & I/O

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
210-6793	E	6793	9

E 6793

TEST CONN. REF	6793 A-REV	6793-1 C-REV
	3	3

REVISION	BY	DATE	APPROVED
CHNG PER DWR # E122	PER	10-21-76	
ADDED P/S & PC		11-5-76	
ADDED P/S & PC		11-15-76	
ADDED P/S & PC		11-17-76	
ECN # 5985		12-28-76	
ADDED P/S & PC		1-3-77	
ECN # 6044		1-27-77	
ADDED P/S & PC		2-4-77	
ECN # 6111		2-25-77	
ADDED P/S & PC		3-4-77	
ECN # 6111		3-10-77	
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ECN # 6178		4-7-77	
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ECN # 6178		4-20-77	
ADDED P/S & PC		4-27-77	
ECN # 6178		5-4-77	
ADDED P/S & PC		5-11-77	
ECN # 6178		5-18-77	
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ECN # 6178		6-1-77	
ADDED P/S & PC		6-8-77	
ECN # 6178		6-15-77	
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ECN # 6178		6-29-77	
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ECN # 6178		7-13-77	
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ECN # 6178		7-27-77	
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ECN # 6178		10-19-77	
ADDED P/S & PC		10-26-77	
ECN # 6178		11-2-77	
ADDED P/S & PC		11-9-77	
ECN # 6178		11-16-77	
ADDED P/S & PC		11-23-77	
ECN # 6178		11-30-77	
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ECN # 6178		12-14-77	
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ECN # 6178		12-28-77	
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ECN # 6178		1-11-78	
ADDED P/S & PC		1-18-78	
ECN # 6178		1-25-78	
ADDED P/S & PC		2-1-78	
ECN # 6178		2-8-78	
ADDED P/S & PC		2-15-78	
ECN # 6178		2-22-78	
ADDED P/S & PC		3-1-78	
ECN # 6178		3-8-78	
ADDED P/S & PC		3-15-78	
ECN # 6178		3-22-78	
ADDED P/S & PC		3-29-78	
ECN # 6178		4-5-78	
ADDED P/S & PC		4-12-78	
ECN # 6178		4-19-78	
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ECN # 6178		5-17-78	
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ECN # 6178		5-31-78	
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ECN # 6178		6-14-78	
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ECN # 6178		6-28-78	
ADDED P/S & PC		7-5-78	
ECN # 6178		7-12-78	
ADDED P/S & PC		7-19-78	
ECN # 6178		7-26-78	
ADDED P/S & PC		8-2-78	
ECN # 6178		8-9-78	
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ECN # 6178		8-23-78	
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ECN # 6178		9-6-78	
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ECN # 6178		9-20-78	
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ECN # 6178		2-17-82	
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ECN # 6178		4-28-82	
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ECN # 6178		5-12-82	
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ECN # 6178		7-7-82	
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ECN # 6178		8-18-82	
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ECN # 6178		12-19-85	
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ECN # 6178		1-16-86	
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ECN # 6178		2-13-86	
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ADDED P/S & PC		5-15-86	
ECN # 6178		5-22-86	
ADDED P/S & PC		5-29-86	
ECN # 6178		6-5-86	
ADDED P/S & PC		6-12-86	
ECN # 6178		6-19-86	
ADDED P/S & PC		6-26-86	
ECN # 6178		7-3-86	
ADDED P/S & PC		7-10-86	
ECN # 6178		7-17-86	
ADDED P/S & PC		7-24-86	
ECN # 6178		7-31-86	
ADDED P/S & PC		8-7-86	
ECN # 6178		8-14-86	
ADDED P/S & PC		8-21-86	
ECN # 6178		8-28-86	
ADDED P/S & PC		9-4-86	
ECN # 6178		9-11-86	
ADDED P/S & PC		9-18-86	
ECN # 6178		9-25-86	
ADDED P/S & PC		10-2-86	
ECN # 6178		10-9-86	
ADDED P/S & PC		10-16-86	
ECN # 6178		10-23-86	
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ECN # 6178		11-6-86	
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ECN # 6178		11-20-86	
ADDED P/S & PC		11-27-86	
ECN # 6178		12-4-86	
ADDED P/S & PC		12-11-86	
ECN # 6178		12-18-86	
ADDED P/S & PC		12-25-86	
ECN # 6178		1-1-87	
ADDED P/S & PC		1-8-87	
ECN # 6178		1-15-87	
ADDED P/S & PC		1-22-87	
ECN # 6178		1-29-87	
ADDED P/S & PC		2-5-87	
ECN # 6178		2-12-87	
ADDED P/S & PC		2-19-87	
ECN # 6178		2-26-87	
ADDED P/S & PC		3-5-87	
ECN # 6178		3-12-87	
ADDED P/S & PC		3-19-87	
ECN # 6178		3-26-87	
ADDED P/S & PC		4-2-87	
ECN # 6178		4-9-87	
ADDED P/S & PC		4-16-87	
ECN # 6178		4-23-87	
ADDED P/S & PC		4-30-87	
ECN # 6178		5-7-87	
ADDED P/S & PC		5-14-87	
ECN # 6178		5-21-87	
ADDED P/S & PC		5-28-87	
ECN # 6178		6-4-87	
ADDED P/S & PC		6-11-87	
ECN # 6178		6-18-87	
ADDED P/S & PC		6-25-87	
ECN # 6178		7-2-87	
ADDED P/S & PC		7-9-87	
ECN # 6178		7-16-87	
ADDED P/S & PC		7-23-87	
ECN # 6178		7-30-87	
ADDED P/S & PC		8-6-87	
ECN # 6178		8-13-87	
ADDED P/S & PC		8-20-87	
ECN # 6178		8-27-87	
ADDED P/S & PC		9-3-87	
ECN # 6178		9-10-87	
ADDED P/S & PC		9-17-87	
ECN # 6178		9-24-87	
ADDED P/S & PC		10-1-87	
ECN # 6178		10-8-87	
ADDED P/S & PC		10-15-87	
ECN # 6178		10-22-87	
ADDED P/S & PC		10-29-87	
ECN # 6178		11-5-87	
ADDED P/S & PC		11-12-87	
ECN # 6178		11-19-87	
ADDED P/S & PC		11-26-87	
ECN # 6178		12-3-87	
ADDED P/S & PC		12-10-87	
ECN # 6178		12-17-87	
ADDED P/S & PC		12-24-87	
ECN # 6178		12-31-87	
ADDED P/S & PC		1-7-88	
ECN # 6178		1-14-88	
ADDED P/S & PC		1-21-88	
ECN # 6178		1-28-88	
ADDED P/S & PC		2-4-88	
ECN # 6178		2-11-88	
ADDED P/S & PC		2-18-88	
ECN # 6178		2-25-88	
ADDED P/S & PC		3-3-88	
ECN # 6178		3-10-88	
ADDED P/S & PC		3-17-88	
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ADDED P/S & PC		5-12-88	
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ADDED P/S & PC		5-26-88	
ECN # 6178		6-2-88	
ADDED P/S & PC		6-9-88	
ECN # 6178		6-16-88	
ADDED P/S & PC		6-23-88	
ECN # 6178		6-30-88	
ADDED P/S & PC		7-7-88	
ECN # 6178		7-14-88	
ADDED P/S & PC		7-21-88	
ECN # 6178		7-28-88	
ADDED P/S & PC		8-4-88	
ECN # 6178		8-11-88	
ADDED P/S & PC		8-18-88	
ECN # 6178		8-25-88	
ADDED P/S & PC		9-1-88	
ECN # 6178		9-8-88	
ADDED P/S & PC		9-15-88	
ECN # 6178		9-22-88	
ADDED P/S & PC		9-29-88	
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ECN # 6178		10-20-88	
ADDED P/S & PC		10-27-88	
ECN # 6178		11-3-88	
ADDED P/S & PC		11-10-88	
ECN # 6178		11-17-88	
ADDED P/S & PC		11-24-88	
ECN # 6178		12-1-88	
ADDED P/S & PC		12-8-88	
ECN # 6178		12-15-88	
ADDED P/S & PC		12-22-88	
ECN # 6178		12-29-88	
ADDED P/S & PC		1-5-89	
ECN # 6178		1-12-89	
ADDED P/S & PC		1-19-89	
ECN # 6178		1-26-89	
ADDED P/S & PC		2-2-89	
ECN # 6178		2-9-89	
ADDED P/S & PC		2-16-89	
ECN # 6178		2-23-89	
ADDED P/S & PC		3-2-89	
ECN # 6178		3-9-89	
ADDED P/S & PC		3-16-89	
ECN # 6178		3-23-89	
ADDED P/S & PC		3-30-89	
ECN # 6178	

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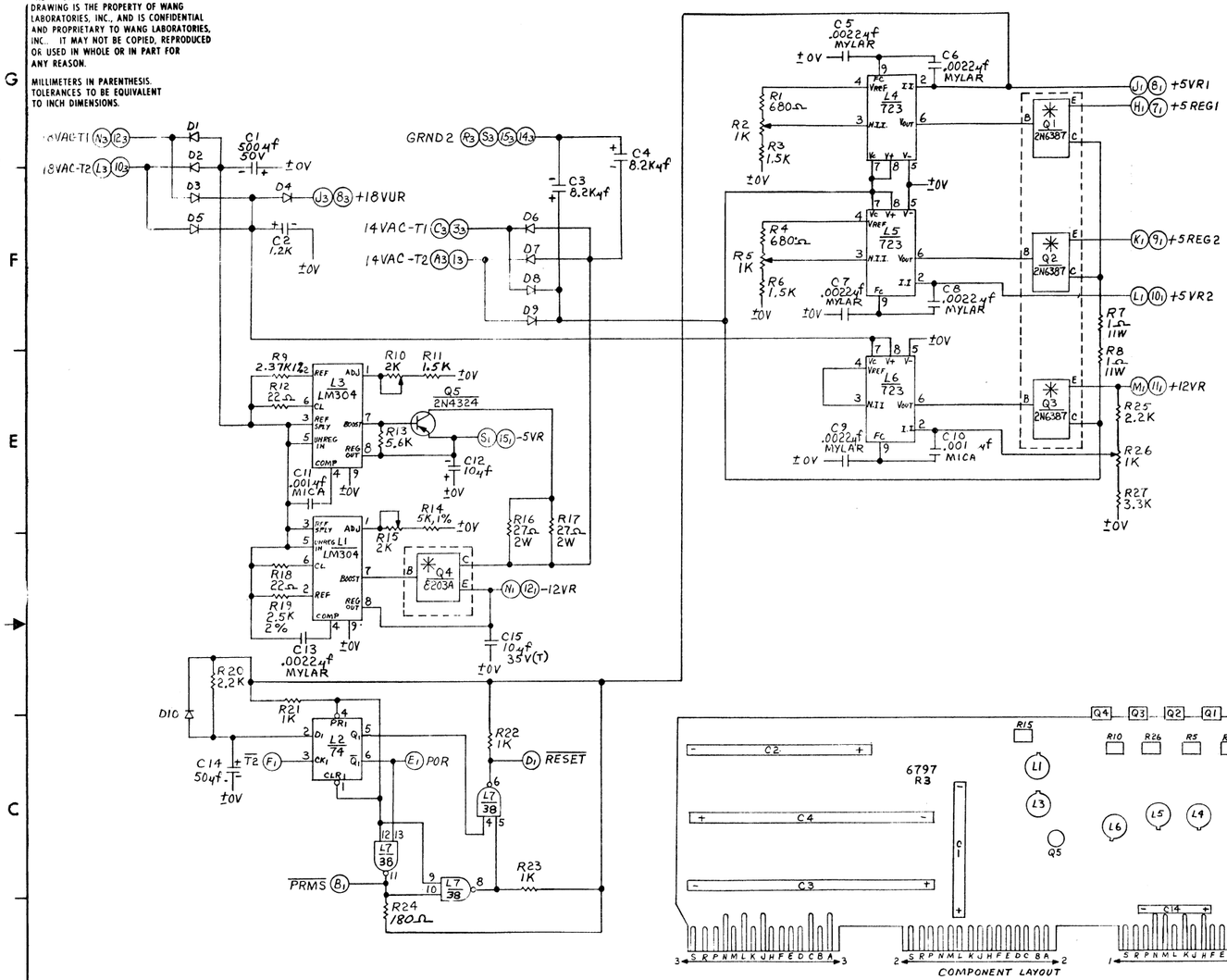
MILLIMETERS IN PARENTHESIS.
TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

DO NOT SCALE



COMPONENT LAYOUT

LOCATION	W.L. PART NO.	TERM. NO. ±0V	TERM. NO. Vcc +5VR
L1, 3	376-0134	9	—
L2	376-0006	7	14
L4, 5, 6	376-0066	5	—
L7	376-0128	7	14

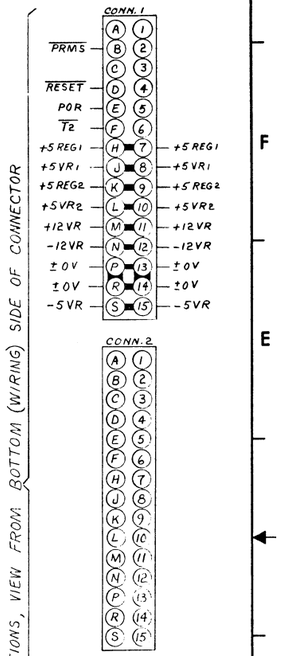
COMPONENT	W.L. PART NO.
R1, 4	330-2068
R2, 5, 26	336-1014
R3, 6, 11	330-3015
R7, 8	334-0000
R20, 25	330-3022
R12, 18	330-1022
R14	333-0015
R10, R15	336-1022
R16, 17	337-1027
R19	333-0014
R21, 22, 23	330-3010
R27	330-3033
C1	300-3053
C2	300-3055
C3, 4	300-3078
C5-9, 13	300-2022
C10, 11	300-5006
C12, 15	300-4032
C14	300-3010
Q1, 2, 3	375-1052
Q4	375-1053
Q5	375-1024
D1, 2, 10	380-4000
D3-9	380-3008
R24	330-2018
R9	333-0093
R13	330-3056

LOCATION	TYPE	SPARES
L2	7474	1
L7	7438	1

HOLE LEGEND & TOLERANCES

HOLE DIA	TOLERANCE
.0135 - .125	+.003 -.001
.126 - .250	+.004 -.001
.251 - .500	+.005 -.001

SYM.	DESCRIPTION	QTY.
A		



1. ALL I.C. CHIPS ARE 7400 SERIES UNLESS OTHERWISE SPECIFIED.
✳ - THESE COMPONENTS MOUNT ON REGULATOR BOARD HEAT SINK.

NOTES

NO.	REVISION	DR BY	CHK BY	APP'D
0	ORIG. PER DWG. REL.			
1	APP'D: W.C.D.			
2	REVISED PER ECN# 2272			
3	REVISED PER ECN# 4533			
4	REVISED PER ECN# 7251			
5	REVISED PER ECN# 8914			

E-REV 2

QTY.	ITEM	WANG PART NO.	DRAWING NO.	DESCRIPTION
NEXT ASSY.				

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN		3-2-76	E ENGR W.C.D	9/9/76
CHK	G.D.	9-9-76	M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO. 2200VP
SEE ENGRG. SPECIFICATIONS No.

TITLE: REGULATOR

FINISH

TOL. EX. AS NOTED
XX ± FRAC ±
XXX ± ANG ± FINISH √

SCALE 1/1 SHT 1 OF 1

210-6797	D	6797	5
WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

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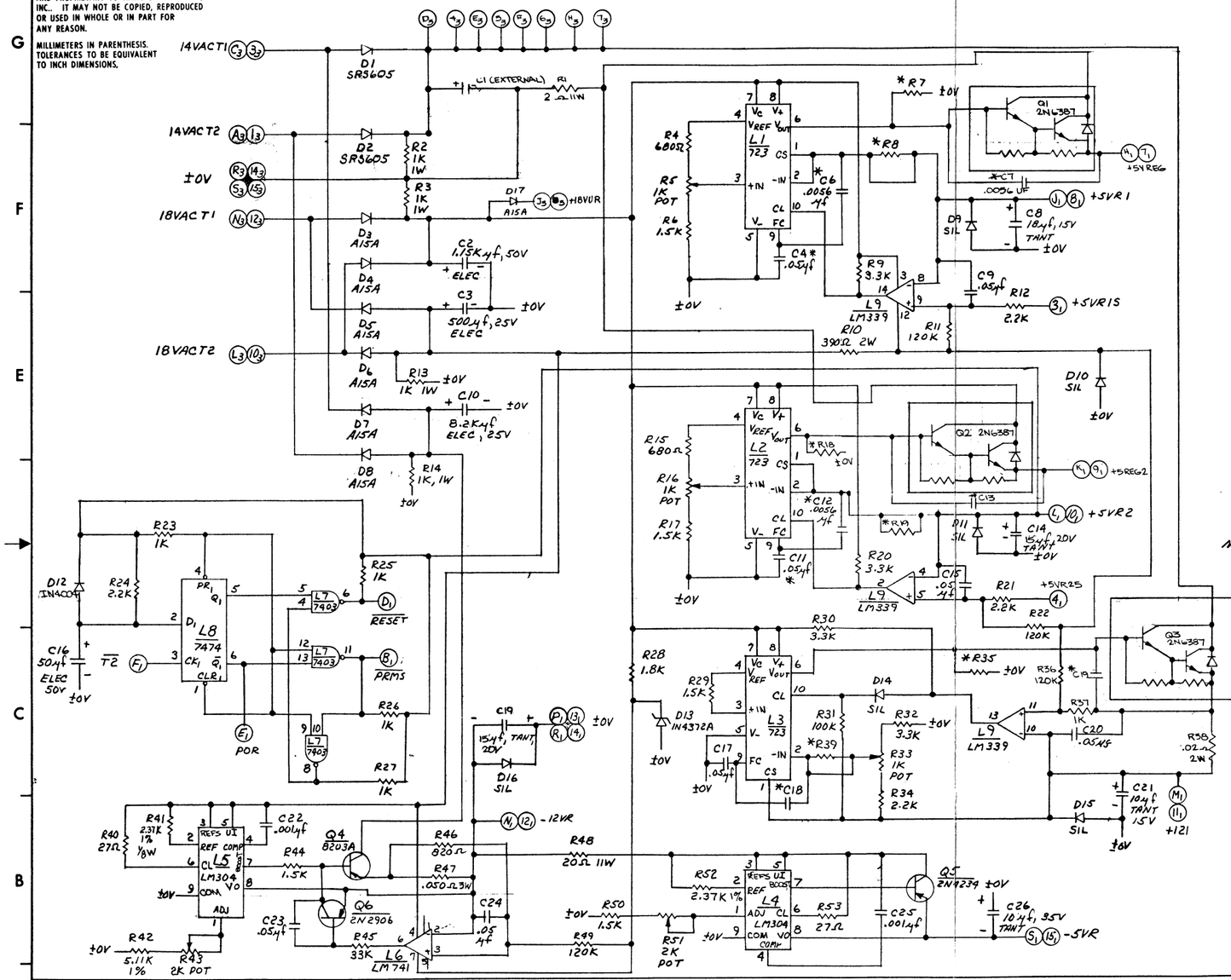
MILLIMETERS IN PARENTHESIS. TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

DO NOT SCALE



LOCATION	W.L. PT. NO.	VCC	GND
L1,2,3	376-0066	—	—
L4,5	376-0134	—	9
L6	376-0074	—	—
L7	376-0028	14	7
L8	376-0006	14	7
L9	376-0240	3	12

SPARES		
LOCAT.	TYPE	SPARES
L7	7403	1
L8	7474	1
L9	LM339	1

COMPONENT	W.L. PT. NO.
Q1,2,3	375-1052
Q4	375-1053
Q5	375-1024
Q6	375-1017

NOTE:
ALL COMPONENTS DESIGNATED (*) ARE NOT LOADED

COMPONENT	W.L. PT. NO.
R1	339-0001
R2,3,13,14	332-3010
R4,15	330-2068
R5,16,33	336-1014
R6,17,29,44,50	330-3015
R9,20,30,32	330-3033
R10	337-2039
R11,22,36,49	330-5012
R12,21,24,34,	330-3022
R23,25,26,27,37	330-3010
R28	330-3018
R31	330-5010
R38	334-0032
R40,53	330-1027
R42	333-0088
R43,51	336-1022
R45	330-4033
R46	330-2082
R47	334-0039
R48	339-0003
R52,41	333-0093
D3 THRU 8,17	380-3008
D9,10,11,14,15,16	380-1001
D12	380-4000
D13	380-2129
C19,21,14	300-4022
C10	300-3078
C2	300-3055
C3	300-3021
C5,9,15,17,20,23,24,27	300-1900
C8,	300-4018
C16	300-3010
C1	EXTERNAL
C22,25	300-1906
C26,	300-4032
D1,2	380-3015

HOLE LEGEND & TOLERANCES

HOLE DIA	TOLERANCE
.0135 - .125	+ .003 - .001
.126 - .250	+ .004 - .001
.251 - .500	+ .005 - .001

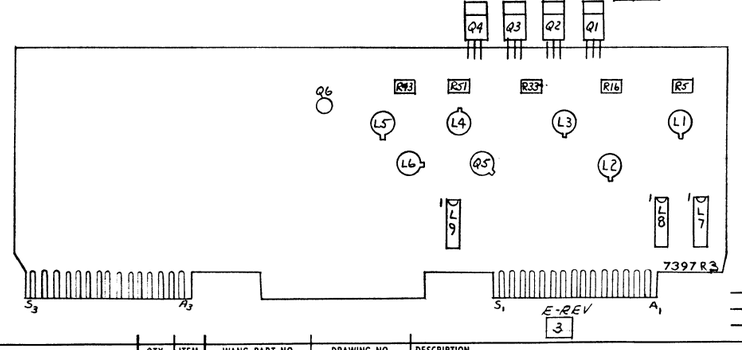
SYM.	DESCRIPTION	QTY.
A		

CONN #1

A 1	PRMS	+5VR1S
B 2		+5VR2S
C 3	RESET	
D 4	POR	
E 5	T2	
F 6		
H 7	+5 REG1	+5 REG1
J 8	+5VR1	+5 VR1
K 9	+5REG2	+5REG2
L 10	+5VR2	+5VR2
M 11	+12VR	+12VR
N 12	-12VR	-12VR
P 13	±0V	±0V
R 14	±0V	±0V
S 16	-5VR	-5VR

CONN #3

A 1	14VAC T2	14VAC T2
B 2		
C 3	14VAC T1	14 VAC T1
D 4	+14VUR	+14VUR
E 5	+14VUR	+14VUR
F 6	+14VUR	+14VUR
H 7	+14VUR	+14VUR
J 8	+18VUR	+18VUR
K 9		
L 10	18VAC T2	18 VAC T2
M 11		
N 12	18VAC T1	18 VAC T1
P 13		
R 14	±0V	±0V
S 15	±0V	±0V



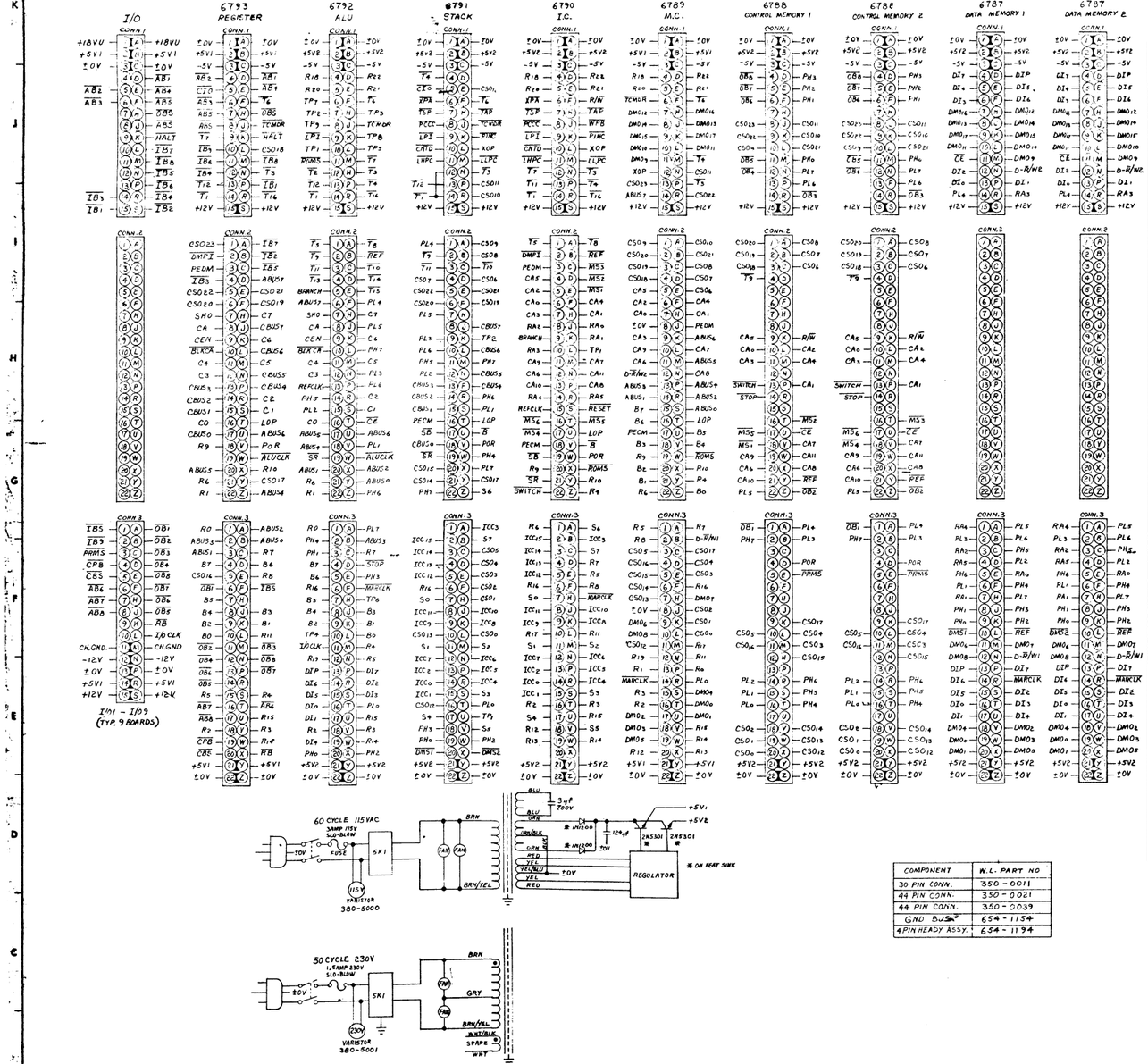
REVISION	BY	DATE	NO.
ORIGINATED PER DWG #E-388	EBA	8-25-77	0
APP'D: S.L.L.			0
REVISED PER ECN #2539	BP	10-11-77	1
APP'D: S.L.L.			1
REVISED PER ECN #3103	AN	6-9-78	2
APP'D: [illegible]			2
REVISED PER ECN #3157	SD	11-7-78	3
APP'D: S.L.L. 12/11/78	CL	2-9-79	4
REVISED PER ECN #3479	JT	2-8-79	5
APP'D: S.L.L. 5-24-79			5
REVISED PER ECN #3479	FSS	5-24-79	6
APP'D: S.L.L. 5-24-79			6

QTY.	ITEM	WANG PART NO.	DRAWING NO.	DESCRIPTION
NEXT ASSY.				

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL	MODEL NO. 2200 VP	BY	DATE / APPROVED BY / DATE
	SEE ENGRG. SPECIFICATIONS No.	DWN EBA	8-25-77 E ENGR
FINISH	TOL. EX. AS NOTED XX ± FRAC. ± XXX ± ANG. ± FINISH √	CHK S.L.L.	10-28-77 M ENGR
	SCALE NONE SHT 1 OF 1		MFG ENGR
		TITLE	POWER SUPPLY REGULATOR
		210-7397	D 7397 6
		WANG PART NUMBER	SIZE DRAWING NUMBER REV.

7397



COMPONENT	W.L. PART NO
30 PIN CONN.	350-0011
44 PIN CONN.	350-0021
44 PIN CONN.	350-0039
GND BUS	654-1154
4 PIN HEADY ASSY.	654-1194

REVISION	BY	DATE
A ORIGINATED PER DWG. #210-6798	AR	11-2-76
B REVISED PER ECN #6284	AR	11-30-77

WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
PC PWR	FIRST USED ON	ASSY USED ON	WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.		

	BY	DATE	APPROVED BY	DATE
DWN	AR	10-29-76	E. ENGR	
CHK	G.D.	11-2-76	M. ENGR	
E.C. CONTROL			MFG ENGR	

MODEL NO 2600
SEE ENGRG SPECIFICATIONS
TOL. EX. AS NOTED .XX ± .010 .XXX ± .005 ANG. ± 1/2° FINISH
MATERIAL
FINISH
TITLE MOTHERBOARD
210-6798 | E | 6798 | A
WANG PART NUMBER | SIZE | DRAWING NUMBER | REV
SHT 4 OF 5

E-REV 2

E 6798

F-19

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DO NOT SCALE

HOLE LEGEND

DRILLED OR PUNCHED HOLE TOLERANCES	HOLE DIA	TOL
	.0135 to .125	± .003
	.126 to .250	± .004
	.251 to .500	± .005

IDENT	DESCRIPTION	QTY
A		

I/O — CONN.1

+18VU	A	+18VU
+5V1	B	+5V1
±0V	C	±0V
	D	ABT
ABZ	E	ABZ
ABS	F	ABS
	H	SBS
	J	ABS
	K	HALT
IBT	L	IBT
IB6	M	IB6
IB5	N	IB5
IB4	P	IB4
IB3	R	IB4
IB1	S	IB2
	T	+12V

I/O1 - I/O9 (TYP. 9 BOARDS)

6793 REGISTER — CONN.1

±0V	A	±0V
+5V2	B	+5V2
-5V	C	-5V
ABT	D	ABT
ABZ	E	ABZ
ABS	F	ABS
T7	H	T6
IB5	J	IB5
IB4	K	IB4
T12	L	IB1
T1	M	T4
T11	N	T3
T10	P	T2
T9	R	T1
T8	S	+12V

6792 ALU — CONN.1

±0V	A	±0V
+5V2	B	+5V2
-5V	C	-5V
R10	D	R22
R20	E	R21
TP1	F	T6
TP2	H	TP3
TP3	J	TP4
TP1	K	TP8
TP1	L	TP5
XOMS	M	T7
T8	N	T3
T10	P	T4
T11	R	T4
+12V	S	+12V

6791 STACK — CONN.1

±0V	A	±0V
+5V2	B	+5V2
-5V	C	-5V
CTS	D	CS018
XPA	E	T6
TSP	F	TAP
PCC	H	TCNOR
LPI	J	PINC
CNTD	K	XOP
LMPC	L	LLPC
T12	M	T5
T11	N	CS011
T1	P	CS010
+12V	R	+12V

6790 I.C. — CONN.1

±0V	A	±0V
+5V2	B	+5V2
-5V	C	-5V
R18	D	R24
R28	E	R23
XPA	F	R/W
TSP	H	TAP
PCC	J	WPB
LPI	K	PINC
CNTD	L	XOP
LMPC	M	LLPC
T7	N	T5
T11	P	T4
T1	R	T14
+12V	S	+12V

6789 M.C. — CONN.1

±0V	A	±0V
+5V2	B	+5V2
-5V	C	-5V
R20	D	R22
R10	E	R21
TCNOR	F	T6
DMO12	H	DMO14
DMO18	J	DMO13
DMO15	K	DMO17
DMO18	L	DMO11
DMO3	M	T4
XOP	N	CS011
CS023	P	T5
ABUS7	R	CS022
+12V	S	+12V

6788 CONTROL MEMORY 1 — CONN.1

±0V	A	±0V
+5V2	B	+5V2
-5V	C	-5V
OBA	D	PH3
OBT	E	PH2
OB4	F	PH1
CS023	J	CS011
CS022	K	CS010
CS019	L	CS021
OB3	M	PH0
OB4	N	PL7
+12V	R	OB3
	S	+12V

6788 CONTROL MEMORY 2 — CONN.1

±0V	A	±0V
+5V2	B	+5V2
-5V	C	-5V
C5025	J	CS011
C5026	K	CS010
C5023	L	CS021
C85	M	PH0
OB4	N	PL7
+12V	R	OB3
	S	+12V

6787 DATA MEMORY 1 — CONN.1

±0V	A	±0V
+5V2	B	+5V2
DI7	C	DIP
DI4	E	DI5
DI3	F	DI6
DMO14	H	DMO12
DMO13	J	DMO16
DMO11	K	DMO15
DMO10	L	DMO10
CE	M	DMO9
DI2	N	D-R/W2
DI0	P	DI1
PL4	R	RA3
+12V	S	+12V

6787 DATA MEMORY 2 — CONN.1

±0V	A	±0V
+5V2	B	+5V2
-5V	C	-5V
DI7	D	DIP
DI4	E	DI5
DI3	F	DI6
DMO14	H	DMO12
DMO13	J	DMO16
DMO11	K	DMO15
DMO10	L	DMO10
CE	M	DMO9
DI2	N	D-R/W2
DI0	P	DI1
PL4	R	RA3
+12V	S	+12V

CONN.2

	A	
	B	
	C	
	D	
	E	
	F	
	H	
	J	
	K	
	L	
	M	
	N	
	P	
	R	
	S	
	T	
	U	
	V	
	W	
	X	
	Y	
	Z	

CONN.2

CSO23	A	IB7
DMPI	B	IB2
PEDM	C	IB5
IB3	D	ABUS7
CSO22	E	CSO21
CSO20	F	CSO19
SHO	H	C7
CA	J	CBUS7
CEN	K	C6
BLKCA	L	CBUS6
C4	M	C5
C3	N	CBUS5
CBUS3	P	CBUS4
CBUS2	R	C2
CBUS1	S	C1
CO	T	LOP
CBUS0	U	ABUS6
R9	V	P.O.R
	W	ALUCLK
ABUS5	X	R10
R6	Y	CSO17
R1	Z	ABUS4

CONN.2

T5	A	T8
T9	B	REF
T11	C	T10
T13	D	T14
BRANCH	E	T15
ABU37	F	PL4
SHO	H	C7
CA	J	PL5
CEN	K	C4
BLKCA	L	PH7
C4	M	C5
C3	N	PL3
REFCLK	P	PL6
PH5	R	C2
PL2	S	C1
CBUS3	T	PL2
CBUS2	U	PH6
CBUS1	V	PL1
PECM	W	LOP
SB	X	B
CBUS0	Y	POR
SR	Z	PH4
CSO15	a	PL7
CSO14	b	PH1
PH1	c	S6

CONN.2

PL4	A	CSO9
T5	B	CSO8
T4	C	T10
CSO7	D	CSO6
CSO22	E	CSO21
CSO20	F	CSO19
PL5	H	LBK
PAN	J	CBUS7
PL3	K	TP2
PL6	L	CBUS6
PH5	M	PH7
PL2	N	CBUS5
CBUS3	P	CBUS4
CBUS2	R	PH6
CBUS1	S	PL1
PECM	T	LOP
SB	U	B
CBUS0	V	POR
SR	W	PH4
CSO15	X	PL7
CSO14	Y	CSO17
PH1	Z	S6

CONN.2

T5	A	T8
DMPI	B	REF
PEDM	C	MS3
CAS	D	MS2
CA2	E	MS1
CA0	F	CA4
CA1	H	CA1
RA2	J	RA4
CA3	K	RA1
BRANCH	L	TP1
RA3	M	CA7
CA9	N	CA5
CA6	P	CA8
D-R/W2	R	CA11
CA10	S	CA6
RA4	T	RA5
REFCLK	U	RESET
MS4	V	MS5
PECM	W	LOP
SB	X	POR
R9	Y	ROMS
SR	Z	R10
SWITCH	a	R4

CONN.2

CSO9	A	CSO10
CSO20	B	CSO21
CSO19	C	CSO8
CSO18	D	CSO7
CA5	E	CSO4
CA2	F	CA4
CA0	H	CA1
T0V	J	PEDM
CA3	K	ABUS4
CA9	L	CA7
CA6	M	ABUS2
D-R/W2	N	CA8
ABUS3	P	ABUS3
ABUS1	R	ABUS2
B7	S	ABUS0
B6	T	LOP
PECM	U	B5
B3	V	B4
B2	W	ROMS
R9	X	R10
B1	Y	R4
R6	Z	B0

CONN.2

CSO20	A	CSO8
CSO19	B	CSO7
CSO18	C	CSO6
T5	D	MM
	E	
	F	
	H	
	J	
	K	
	L	
CA5	M	R/W
CA4	N	CA2
CA3	P	CA0
SWITCH	R	CA1
STOP	S	MS1
MS0	T	MS2
MS1	U	CE
CA7	V	CA11
CA9	W	CA10
CA8	X	REF
CA10	Y	OB2
PL5	Z	T0V

CONN.2

CSO20	A	CSO8
CSO19	B	CSO7
CSO18	C	CSO6
T5	D	MM
	E	
	F	
	H	
	J	
	K	
	L	
CA5	M	R/W
CA4	N	CA2
CA3	P	CA0
SWITCH	R	CA1
STOP	S	MS1
MS0	T	MS2
MS1	U	CE
CA7	V	CA11
CA9	W	CA10
CA8	X	REF
CA10	Y	OB2
PL5	Z	T0V

CONN.2

	A	
	B	
	C	
	D	
	E	
	F	
	H	
	J	
	K	
	L	
	M	
	N	
	P	
	R	
	S	
	T	
	U	
	V	
	W	
	X	
	Y	
	Z	

CONN.2

	A	
	B	
	C	
	D	
	E	
	F	
	H	
	J	
	K	
	L	
	M	
	N	
	P	
	R	
	S	
	T	
	U	
	V	
	W	
	X	
	Y	
	Z	

CONN.3

IBS	A	OB1
IB3	B	OB2
PRMS	C	OB3
CPB	D	OB4
CBS	E	OB5
AB4	F	OB7
AB7	H	OB6
ABB	J	OB8
	K	RB
	L	T/B CLK
CH.GND	M	CH.GND
-12V	N	-12V
±0V	P	±0V
+5V1	R	+5V1
+12V	S	+12V

CONN.3

RO	A	ABUS2
ABUS3	B	ABUS0
ABUS1	C	R7
B7	D	STOP
CSO14	E	PH3
OB1	F	MARCLK
B5	H	PA3
B4	J	B3
B3	K	R11
B2	L	B1
B0	M	R10
OB2	N	OB3
OB5	P	PA1
R5	R	P4
AB7	S	AB6
AB5	T	R15
R2	U	R3
CPB	V	R14
OB5	W	RB
+5V2	X	+5V2
±0V	Y	±0V
	Z	

CONN.3

RO	A	PL7
PH4	B	ABUS3
PH1	C	R7
B7	D	STOP
B6	E	PH3
R14	F	MARCLK
S0	H	TP6
ICC11	J	ICC10
ICC9	K	ICC8
CSO13	L	CSO6
S1	M	S2
ICC7	N	ICC4
ICC2	P	ICC5
ICC0	R	ICC4
ICC1	S	S3
CSO12	T	PL0
S4	U	TP1
PH3	V	S5
PH0	X	PH2
OMST	Y	DMS2
+5V2	Z	+5V2
±0V	a	±0V

CONN.3

PA1	A	ICC3
ICC15	B	S7
ICC14	C	S6
ICC13	D	CSO4
ICC12	E	CSO3
R14	F	CSO2
S0	H	CSO1
ICC11	J	ICC10
ICC9	K	ICC8
R17	L	R11
S1	M	S2
ICC7	N	ICC6
ICC2	P	ICC5
ICC0	R	ICC4
ICC1	S	S3
R2	T	R3
S4	U	R15
R12	V	S5
R13	W	R14
MS3	X	MS4
+5V2	Y	+5V2
±0V	Z	±0V

CONN.3

R4	A	S4
R6	B	ICC3
CSO5	C	S7
CSO4	D	S6
CSO3	E	R5
CSO2	F	R6
CSO1	H	MAROLX
T0V	J	ICC10
DMO6	K	ICC8
DMO8	L	R11
CSO12	M	S2
R13	N	ICC6
R1	P	ICC5
MARCLK	R	PL0
R3	S	S3
R2	T	R3
DMO2	U	R15
DMO3	V	S5
DMO5	W	R14
R12	X	MS4
+5V2	Y	+5V2
±0V	Z	±0V

CONN.3

R5	A	R7
R8	B	D-R/W1
CSO5	C	CSO17
CSO4	D	CSO9
CSO3	E	CSO3
CSO2	F	R16
CSO3	H	DMO7
T0V	J	CSO2
DMO4	K	CSO1
CSO17	L	CSO0
DMO8	M	R7
DMO7	N	R11
MARCLK	P	R0
R1	R	R11
S3	S	DMO4
R2	T	DMO0
DMO1	U	R17
DMO5	V	R14
R12	W	R13
+5V2	X	+5V2
±0V	Z	±0V

CONN.3

OB1	A	PL4
PH7	B	PL3
	C	
	D	POR
	E	PRMS
	F	
	H	
	J	
	K	
	L	
CSO5	M	CSO17
CSO4	N	CSO4
CSO3	P	CSO3
DMO4	R	DMO7
DMO8	S	DMO4
DMO7	T	DMO0
D-R/W1	U	R17
DMO6	V	DMO2
DMO3	W	DMO3
DMO1	X	DMO5
+5V2	Y	+5V2
±0V	Z	±0V

CONN.3

PA4	A	PL5
PL3	B	PL6
RA5	C	PH5
RA1	E	PL3
RA4	F	RA0
PH4	H	PL4
PL7	J	RA1
PH1	K	PH3
PH0	L	PH2
DI7	M	D-R/W1
DI4	N	MARCLK
DI5	P	DI2
DI0	R	DI3
DI1	S	DI4
PH4	T	PL0
PH5	U	PL1
PL5	V	PL2
PL6	X	PH6
PH7	Y	PL7
+5V2	Z	+5V2
±0V	a	±0V

CONN.3

RA4	A	PL5
PL5	B	PL6
RA5	C	PH5
RA2	E	PL3
RA3	F	RA0
PH4	H	PL4
PL7	J	RA1
PH1	K	PH3
PH0	L	PH2
DMO5	M	DMO7
DMO4	N	DMO6
DMO2	P	DMO0
DMO3	R	DMO1
DMO5	S	DMO4
DI7	T	DIP
DI4	U	DI5
DI3	V	DI6
DMO12	W	DMO14
DMO13	X	DMO16
DMO15	Y	DMO17
DMO10	Z	DMO11
DMO9	a	CE
D-R/W2	b	DI2
DI1	c	DI0
RA3	d	PL4
+12V	e	+12V

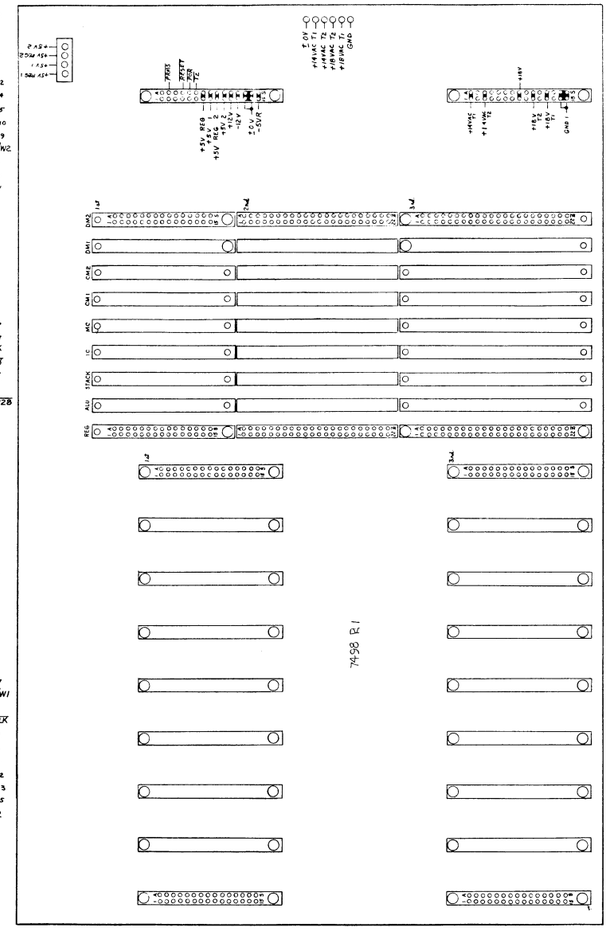
CUT ETCH FOR 2200 VP6

60 CYCLE 115 VAC
3AMP 115V SLO-BLOW
FUSE
SK1
VARISTOR 380-5000
BRN
FAN
GRN/YEL

50 CYCLE 230V
1.5AMP 230V SLO-BLOW
SK1
230V VARISTOR 380-5001
BRN
GRY
BRN/YEL
BLU/BLK
SPARE
WHT

BLU
BLU/BLK
3 μF 700V
D1
* IN1200
D2
* IN1200
ORN
RED
YEL
YEL/BLU
GRN
YEL
RED
124 μF 10V
Q1
Q2
+5V1
+5V2
2N5685
2N5685
REGULATOR
* ON HEAT SINK

COMPONENT	W.L. PART NO
30 PIN CONN.	350-0011
44 PIN CONN.	350-0021
44 PIN CONN.	350-0039
GND BUS	654-1154
4 PIN READY ASSY.	654-1194



E-REV 0

WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
Qty/Bd	FIRST USED ON	ASSY USED ON	WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.		

	BY	DATE	APPROVED BY	DATE
DWN J.L.B.		2-21-79	S. ENGR D. Kelly	4-16-79
CHK G.D.		4-2-79	M. ENGR	
E.C. CONTROL			MFG ENGR	

MATERIAL

FINISH

MODEL NO 2200 VP/MVP

SEE ENGRG SPECIFICATIONS

TOL EX AS NOTED
XX ± .010 FRAC ± 1/64
XXX ± .005 ANG ± 1° 30' FINISH

SCALE — SHT 1 OF 1

TITLE MOTHERBOARD

210-7498 | E | 7498 | 0
WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.

NO	REVISION	BY	DATE
1	ECN M 82-179		
0	PER DWG RESS APPROVED 12-15-77		

7498

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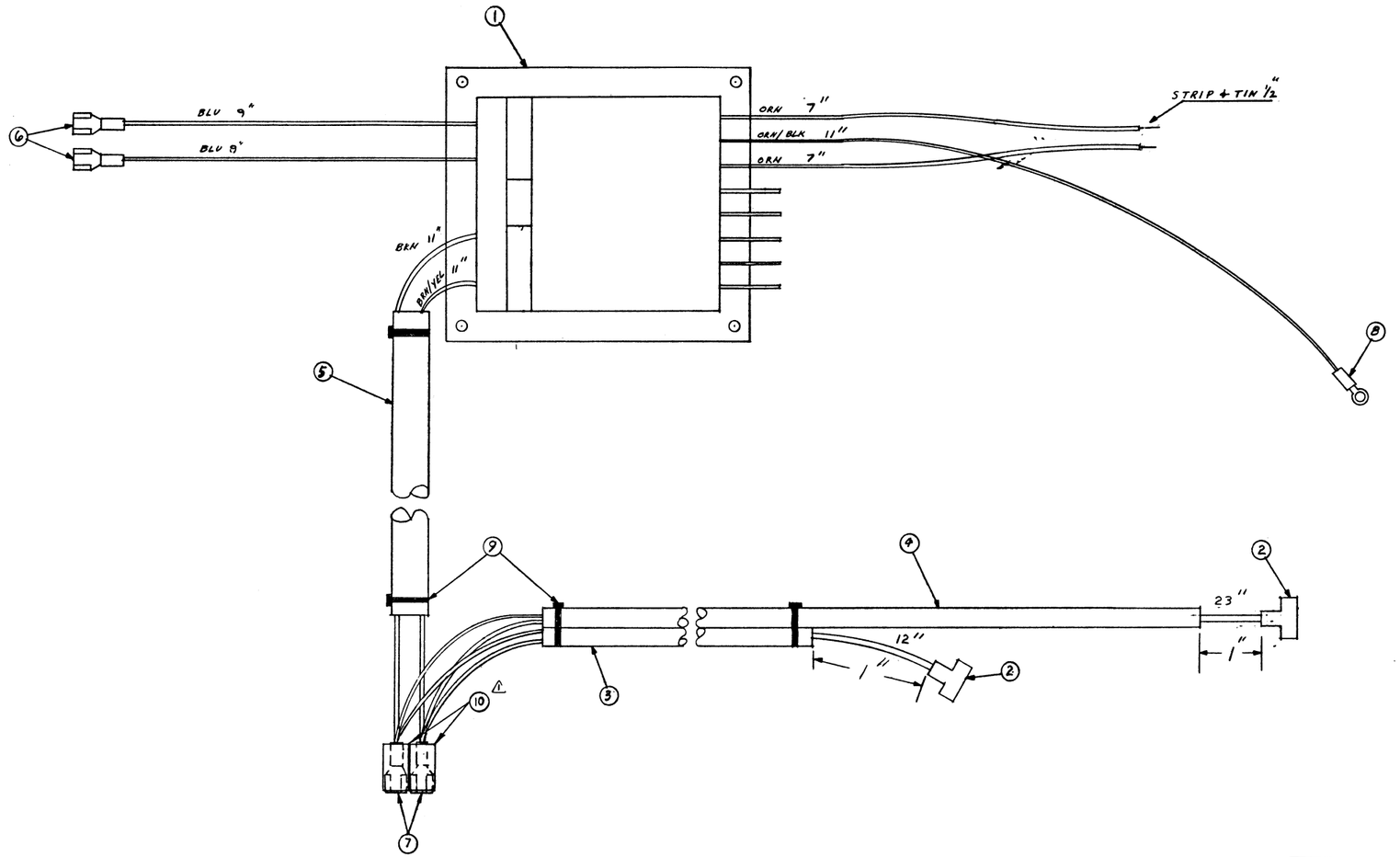
MILLIMETERS IN PARENTHESIS.
TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

DO NOT SCALE

HOLE LEGEND & TOLERANCES	
HOLE DIA	TOLERANCE
.0135 - .125	+ .003 - .001
.126 - .250	+ .004 - .001
.251 - .500	+ .005 - .001

SYM.	DESCRIPTION	QTY.
A		



ECN NO. PENDING 12091

QTY.	ITEM	WANG PART NO.	DRAWING NO.	DESCRIPTION
A/R	10	605-0132		TUBING, HEATSHRINK
4	9	654-1004		CABLE TYE
1	8	654-0075R		RING LUG YELLOW
2	7	654-0017R		FASTON TERM YELLOW
2	6	654-0048R		FASTON TERM RED
1	5	605-0012		SLEEVE #4 TUBING 9" LONG
1	4	605-0015		SLEEVE #3 TUBING 20" LONG
1	3	605-0015		SLEEVE #3 TUBING 9" LONG
2	2	420-1005		POWER CORD ROTRON FAN
1	1	410-0114		TRANSFORMER

NEXT ASSY.

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

BY	DATE	APPROVED BY	DATE
DWN LB	10/27/76	E ENGR	
CHK		M ENGR	
		MFG ENGR D.L.	11/5/76

MATERIAL

MODEL NO.

SEE ENGRG. SPECIFICATIONS No.

FINISH

TOL. EX. AS NOTED
XX ± FRAC ±
XXX ± ANG ± FINISH √

SCALE 1/2 SHT 1 OF 1

TITLE
TRANSFORMER HARNESS (2200 VA 60 Hz)

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
270-3065	D	6482-125	3

NO.	REVISION	BY	DATE
1	ORG PER PWR 8232	VPS	6.D. 10/15/76
2	REVISED PER ECN 6203 REVISED PER ECN 6183	JP	8-11-76
3	REVISED PER ECN 11036 APP'D:		12-16-76

D 6482-125

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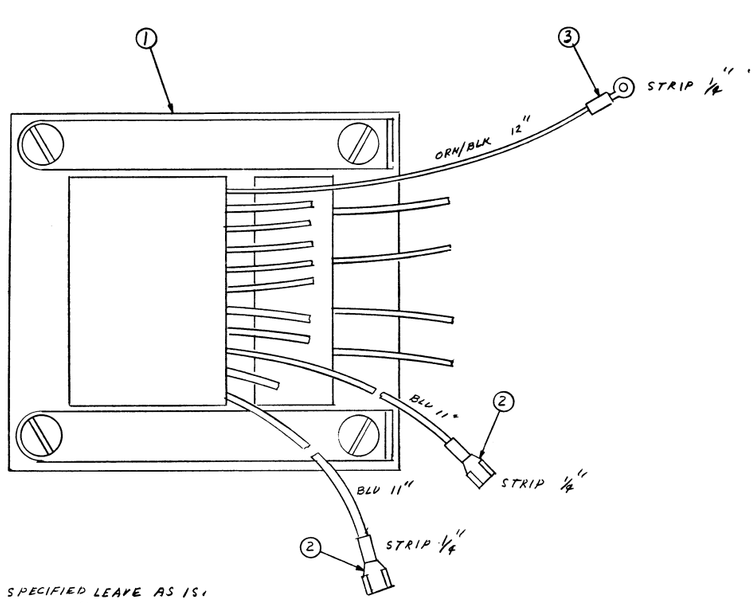


NOTE:
1. WIRES NOT SPECIFIED LEAVE AS IS.
2. OVERALL TOL. ± 1/4"

WANG PART NO.	ITEM	QTY	NAME	DESCRIPTION
659-0075R	3	1	RING LUG	#10 YELLOW
659-0048R	2	2	FASTON	RED
410-0131	1	1	TRANSFORMER	C5068-131

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	YS	5/1/79	E ENGR	
CHK	G.D.	5/16/79	M ENGR	5/22/79
E C CONTROL			MFG ENGR	

MATERIAL

MODEL NO 2200 MVPA

SEE ENGRG SPECIFICATIONS NO.

FINISH

TOL. EX. AS NOTED
XX ± .010 FRAC ± 1/64
XXX ± .005 ANG ± 1°30' FINISH 125

SCALE 7/1 SHT 1 OF 1

TITLE: TRANSFORMER HARNESS 60 Hz

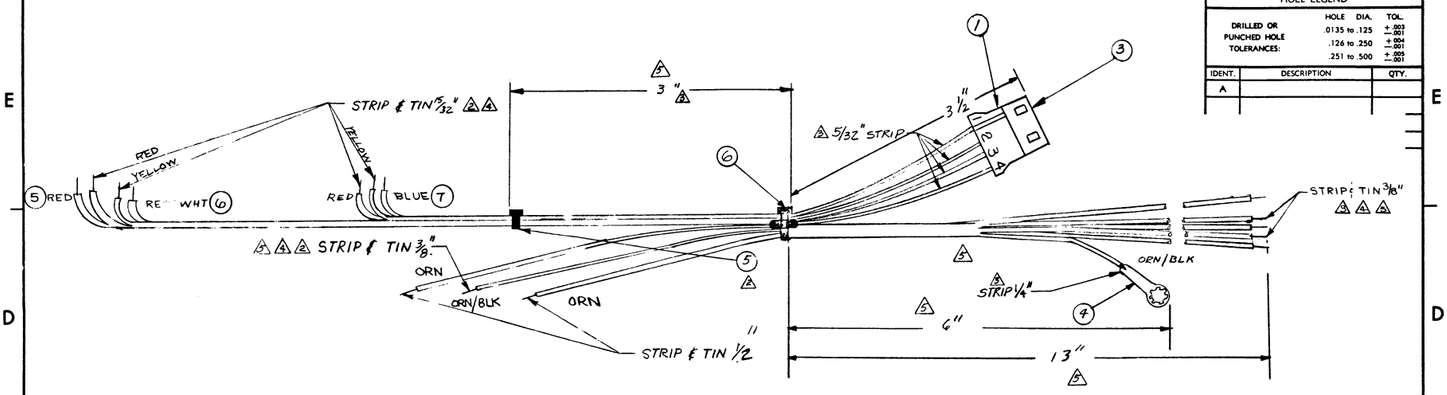
270-3120 | C | 6482-371 | 0

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

16E-2869 D

NO.	REVISION	DATE	BY
0	ORG. REL. DWG.	5/1/79	YS

F-22



SOCKET NO	WIRE COLOR	GAUGE	LENGTH ± 1/2"
1	YELLOW	#14	9 1/2"
2	RED	#14	9 1/4"
3	YELLOW	#14	13 1/2"
4	RED	#14	13 1/4"

PIN NO.	WIRE COLOR	GAUGE	LENGTH ± 1/2"
1	ORANGE	#12	15 5/8"
2	ORANGE	#12	16 3/4"
5	RED	#24	2.3330
6	RED/WHT	#24	2.3330
7	BLUE	#24	2.0000

605-1011	6	1	TY-WRAP I.D. MARKER		270-3066	
600-2092		A/R	WIRE		#24 RED/WHT	
600-2002		A/R	WIRE		#24 RED	
600-2006		A/R	WIRE		#24 BLUE	
600-6130		A/R	WIRE		#12 GA ORN/BLACK	
600-6103		A/R	WIRE		#12 GA ORANGE	
600-6004		A/R	WIRE		#14 GA YELLOW	
600-6002		A/R	WIRE		#14 GA RED	
605-1004	5	1	TY-RAP			
654-0075R	4	1	LUG, RING BURNDY		YELLOW	
654-1163R	3	4	MATE-LOCK SOCKET		14-20 GA	
654-1195	1	1	SOCKET HOUSING 4 POS		AMP.	
WANG PART NO.	ITEM	QTY.	NAME	MATERIAL	DESCRIPTION	

REV	NO	REVISION	BY	DATE	APPROVED BY	DATE
	C	ORG. PER DWG #210				
	1	REV PER ECN 6203 12-13-76 JEFFOWERS				
	2	REV PER ECN 7248 T.R.A. 7/27/77				
	3	REV PER ECN #7639 MJB 10-20-77				
	4	REV PER ECN #7824 TRP 11-30-77				
	5	REV PER ECN #8157 2-15-78 JMB				
	6	REV PER ECN #9183 JAB 8-10-78				
	7	REV PER ECN #10568 APP'D 7-2-79				
	8	REVISED PER ECN # 11874 APP'D: 9.27.7979				

DRN	1/1	EPS	12/4/76
CHK	1/1		
T.M.			10/21/77
E.C.N.			
C.D.			2-26-78
C.D.		LB	8/21/78
			7.2.79

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL	MODEL NO. 2200 VP	DWN	10/16/76
	SEE ENGRG SPECIFICATIONS No.	CHK	
FINISH	TOL EX AS NOTED .XX ± .010 FRAC. ± 1/64 .XXX ± .005 ANG ± 1° 32 FINISH	E. C. CONTROL	
	SCALE SHT OF	E ENGR	
		M ENGR	
		MFG ENGR	10/16/76

TITLE: HEAT SINK HARNESS (2200 VP)

270-3066	C	6482-126	8
WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

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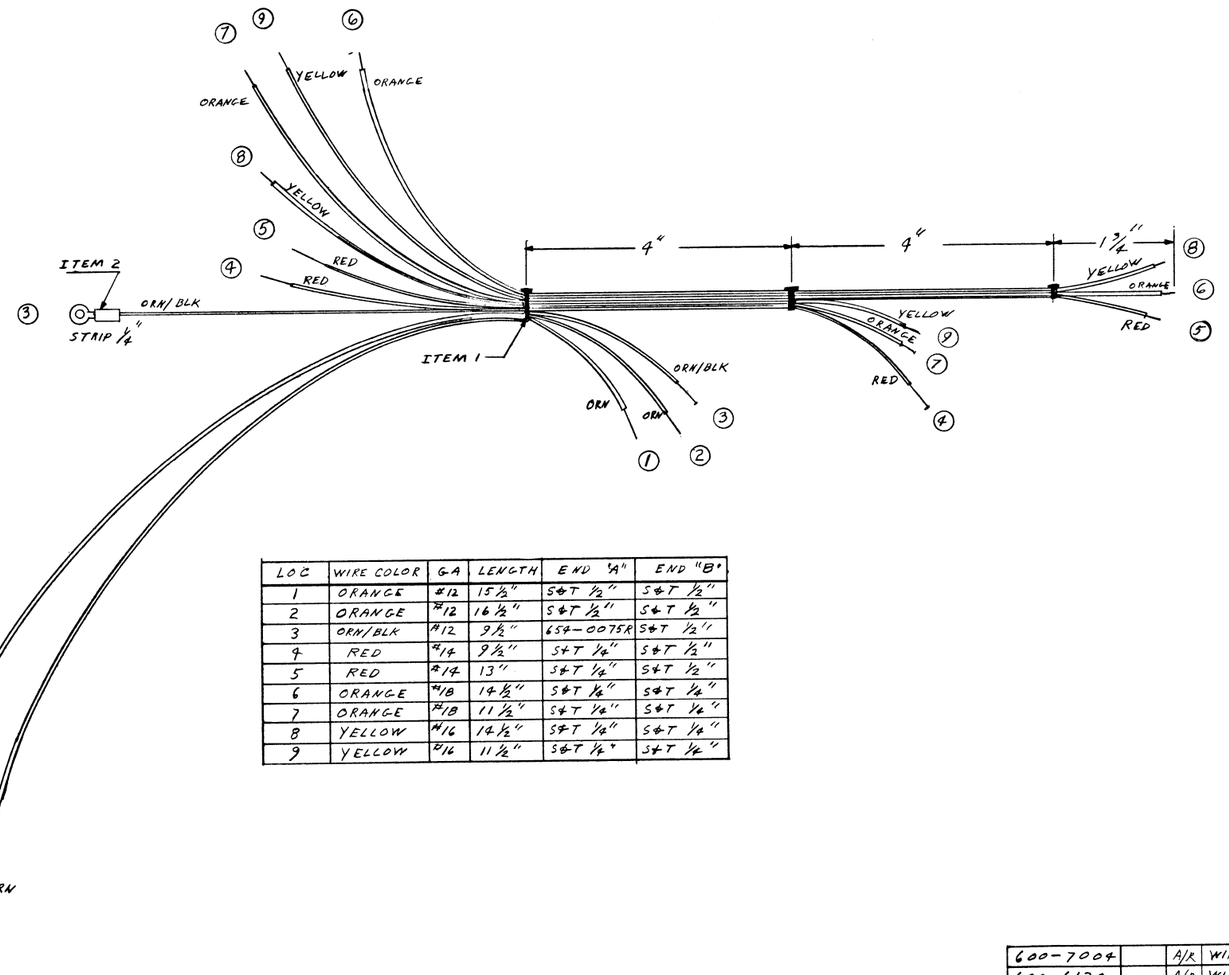
DO NOT SCALE



LOC	WIRE COLOR	GA	LENGTH	END "A"	END "B"
1	ORANGE	#12	15½"	S&T ½"	S&T ½"
2	ORANGE	#12	16½"	S&T ½"	S&T ½"
3	ORN/BLK	#12	9½"	654-0075R	S&T ½"
4	RED	#14	9½"	S&T ¼"	S&T ½"
5	RED	#14	13"	S&T ¼"	S&T ½"
6	ORANGE	#18	14½"	S&T ¼"	S&T ¼"
7	ORANGE	#18	11½"	S&T ¼"	S&T ¼"
8	YELLOW	#16	14½"	S&T ¼"	S&T ¼"
9	YELLOW	#16	11½"	S&T ¼"	S&T ¼"

WANG PART NO.	ITEM	QTY	NAME	DESCRIPTION
600-7004		A/R	WIRE	#16GA YELLOW
600-6130		A/R	WIRE	#12GA ORN/BLK
600-6103		A/R	WIRE	#12GA ORANGE
600-6002		A/R	WIRE	#14GA RED
600-0003		A/R	WIRE	#18GA ORANGE
654-0075R	2	1	RING LUG	#10 YELLOW
605-1004	1	3	TYE WRAP	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	[illegible]	12-7-78	E ENGR	
CHK	G.D.	12/12/78	M ENGR	
			MFG ENGR	12/12/78

MATERIAL

MODEL NO. 2200 MVPA
SEE ENGRG. SPECIFICATIONS No.

FINISH

TOL. EX. AS NOTED
XX ± FRAC. ±
XXX ± ANG. ± FINISH √

TITLE MVPA POWER SUPPLY HEATSINK HARNESS

SCALE Full SHT 1 OF 1

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
270-3121	D	6482-378	5

NO.	REVISION	BY	DATE
5	ORG. PER DWR'S 610		12/7

D 6482-378

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DO NOT SCALE

HOLE LEGEND & TOLERANCES			
HOLE DIA		TOLERANCE	
.0135 - .125		+.003 -.001	
.126 - .250		+.004 -.001	
.251 - .500		+.005 -.001	
SYM	DESCRIPTION	QTY	
A	.128 DIA. THRU	12	
B	.137/.140 DIA. THRU	5	
C	.213/.216 DIA. THRU	30	
D	.1875/.1928 DIA. THRU	7	
E	.128 DIA THRU (1 82° CSK TO .250 DIA.	6	
F	.156 DIA. THRU	4	
H	.201 DIA. THRU	6	
J	1.00 WIDE x 2.00 LONG OVAL SLOT	1	
K	.50 DIA DOUBLE 'D'	2	
M	.250 +.005 -.000 DIA THRU	16	
P	.111/.114 DIA THRU	3	
R	.75 DIA THRU	1	
S	.56 DIA THRU	1	
T	.09 W x .56 L. RECT SLOT	3	

SEE NOTE 15

SEE DETAIL Y-Y

SEE NOTE 13

SEE NOTE 14

SEE NOTE 15

(6) (FILL & SAND SMOOTH BEFORE PAINTING IF REQ'D)

.75 5 PLACES

.50(HEM) 2 PLACES

SEE DETAIL X-X

SEE DETAIL W-W

.50 7 PLACES

.38 SQ., 48 PLACES

REVISION	BY	DATE	APPROVED BY	DATE
0 GEN. RELEASE DWG. #451-1105	CRC	2/5/77		
1 REV PER ECN 0044	CRC	2/10/77		
2 REV PER ECN 0068	CRC	3/10/77		
3 REV PER ECN 0682	CRC	5/10/77		
4 REV PER ECN 1015	CRC	8/10/78		
5 REV PER ECN 1082	CRC	3/9/79		
6 REV PER ECN 1115	CRC	4/4/79		
7 REV PER ECN 1178	CRC	6/13/79		

QTY	ITEM	WANG PART NO.	DRAWING NO.	DESCRIPTION
NEXT ASSY.				

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	SEB	4/11/75	E ENGR	
CHK	CRC	4/11/75	M ENGR	
QTY / 1			MFG ENGR	

MATERIAL: .09 THK ALUM., 5052-H32 | MODEL NO. 2200 VP | TITLE: CHASSIS, CPU (9 I.O.)

FINISH - SEE NOTE 8 | TOL EX. AS NOTED .XX ±.01 .XXX ±.005 ANG. ±1° | SCALE 1:1 | SHT 1 OF 2

WANG PART NUMBER 451-1105 (REF.) | SIZE E | DRAWING NUMBER 6819-100 | REV 8

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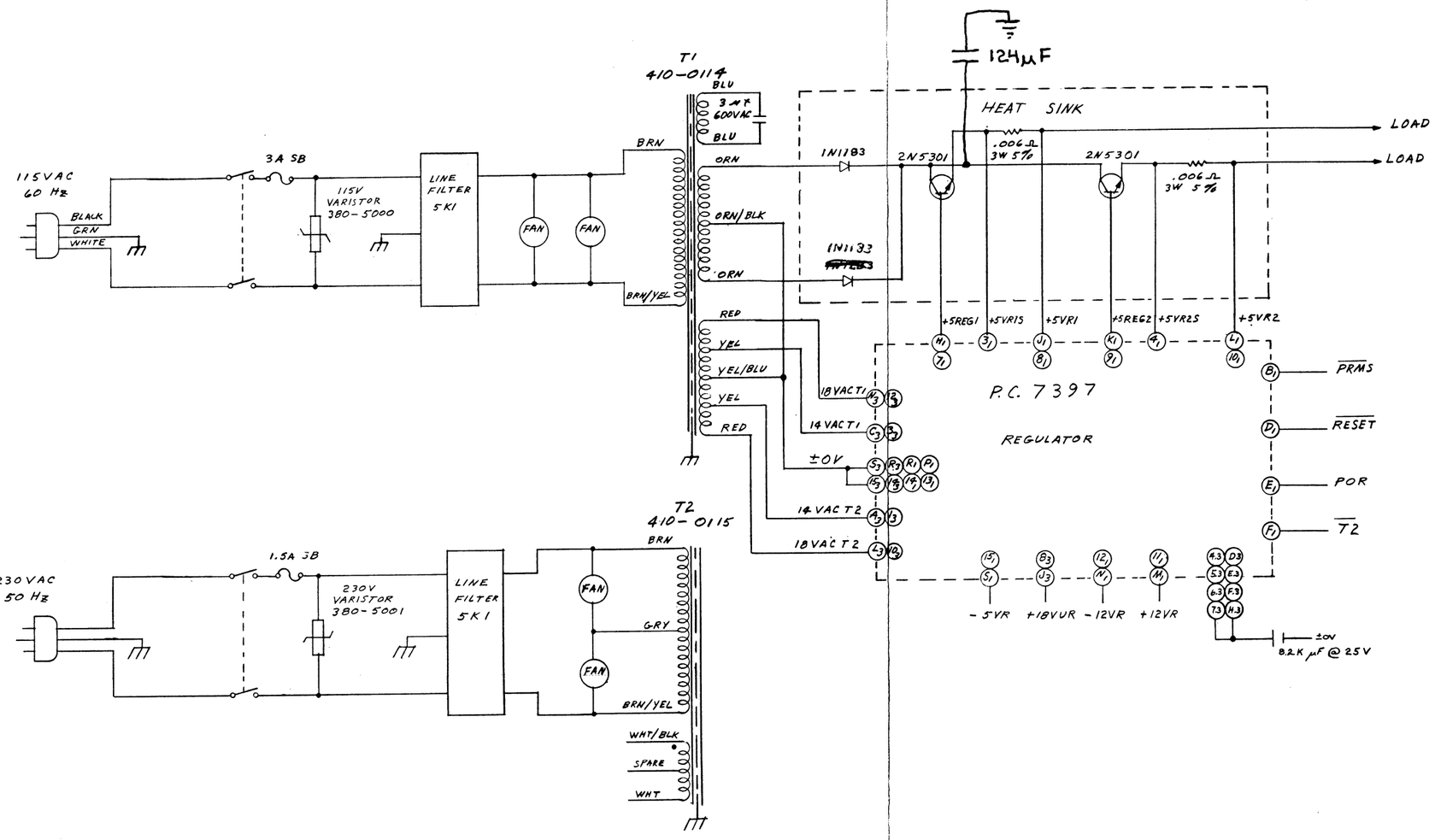
DO NOT SCALE



NO.	REVISION	DR'N BY	DATE
0	ORG. PER DWR E563 APP: DJ 4-1-78	BB	3-15-78
1	REVISED PER ECN #999 APPD: 12-1-78	LL	11-30-78

	BY	DATE	APPROVED BY	DATE
DWN	BB	3-15-78	E ENGR DRESSEL	9-1-78
CHK	G.D.	9-1-78	M ENGR	
			MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL —

MODEL NO. 2200VP
SEE ENGRG. SPECIFICATIONS
No.

FINISH —

TOL. EX. AS NOTED
XX ± FRAC. ±
XXX ± ANG. ± FINISH √

TITLE INTERCONNECTION SCHEMATIC

SCALE — SHT OF

WANG PART NUMBER | SIZE D | DRAWING NUMBER 6819-999 | REV. 1

666-6181

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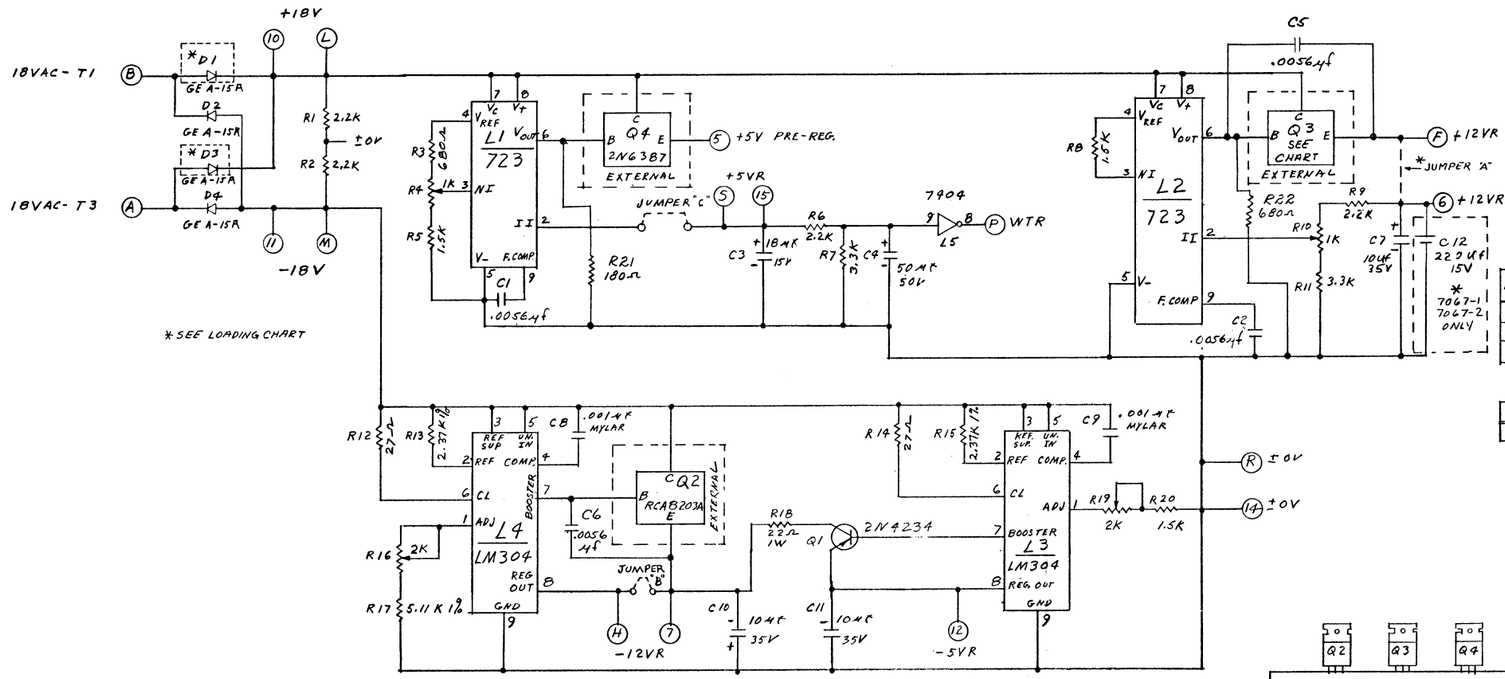
MILLIMETERS IN PARENTHESIS.
TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

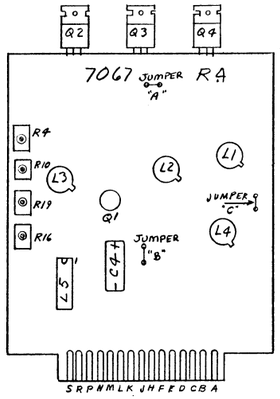
DO NOT SCALE



LOCATION	W.L. PART NO.	PIN NO ±0V	PIN NO +5 VR
L1, 2	376-0066	5	
L3, 4	376-0134	9	
L5	376-0010	7	14

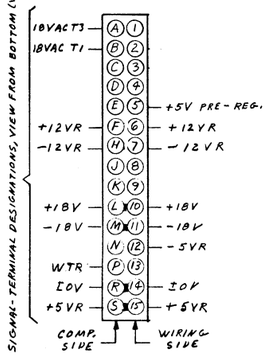
I.C. TYPE	LOCATION	SPARE
7404	L5	5

LOADING CHART	
210-7067	DO NOT LOAD C12, LOAD 375-1052 ON Q3
210-7067-1	DO NOT LOAD D1, D3 & JUMPER "A", CHG. C3 TO A 300-4020-474F, CHG. C7 TO A 300-4045-220μF LOAD 375-1035 ON Q3
210-7067-2	LOADING SAME AS 7067, BUT REMOVE JUMPER "B". LOAD 375-1035 ON Q3



HOLE LEGEND & TOLERANCES	
HOLE DIA	TOLERANCE
.0135 - .125	+.003 - .001
.126 - .250	+.004 - .001
.251 - .500	+.005 - .001

SYM.	DESCRIPTION	QTY.
A		



COMPONENT	W.L. PART NO.
R1, 2, 6, 9	330-3022
R3, 22	330-2068
R4, 10,	336-1014
R5, 8, 20	330-3015
R7, 11	330-3033
R16, 19	336-1022
R13, R15	333-0093
R12, 14	330-1027
R17	333-0088
R18	332-1022
R21	330-2018
C1, 2, 5, 6	300-1915
* C3	300-4018
C4	300-3010
C8, 9	300-2010
* C7, 10, 11	300-4032
* C12	300-4045
* D1, 2, 3, 4	380-3008
Q1	375-1024
Q2	375-1053
* Q3, 4	375-1052
Q1 FAD	375-9001

7067 E-REV	7067-1 E-REV	7067-2 E-REV
6	6	5

NO.	REVISION	DRWN BY	DATE
0/0	ORIG. PER DWR # E151 APP'D W.C.D.	RB	7-30-76
1/1	REVISED PER ECN # 5153 APP'D W.C.D. 11/5	RB	9-13-76
2/0	REVISED PER ECN # 5537 APP'D: W.C.D. 1977	JR	6-13-76
3/1	REVISED PER ECN # 5876 APP'D: W.C.D. 9/23	WRJ	8-23-76
4/2	REVISED PER ECN # C381 APP'D: W.C.D.	EBA	2-17-77
5/2	REVISED PER ECN # 6625 APP'D: W.C.D.	WRJ	5-3-77
6/6	REVISED PER ECN # 6929 APP'D: W.C.D. 6/16-77	EBA	5-18-77
7/3	REVISED PER ECN # 7112 APP'D: J.L.L.	EBA	7-28-77
8/4	REVISED PER ECN # 7279/7313 APP'D: J.L.L.	EBA	10-25-77
9/5	REVISED PER ECN # 7280/7280A APP'D 7596 J.L.L.	EBA	5-4-77
10/6	REVISED PER ECN # 7584 APP'D 7504	WRJ	10-11-77
11/3	ECN # 8989 APP'D: W.C.D. 4/18	EC	4-24-78

QTY.	ITEM	WANG PART NO.	DRAWING NO.	DESCRIPTION
NEXT ASSY.				

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	JAB	3/30/76	E ENGR W.C.D.	4/5/78
CHK	G.D.	4-30-76	M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO. 2200F
SEE ENGRG. SPECIFICATIONS
No.

FINISH

TOL. EX. AS NOTED
XX ± FRAC ±
XXX ± ANG. ± FINISH √

TITLE SCHEMATIC POWER SUPPLY REGULATOR

SCALE | SHT 1 OF 1

SEE CHART	D	7067	11
WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

7067

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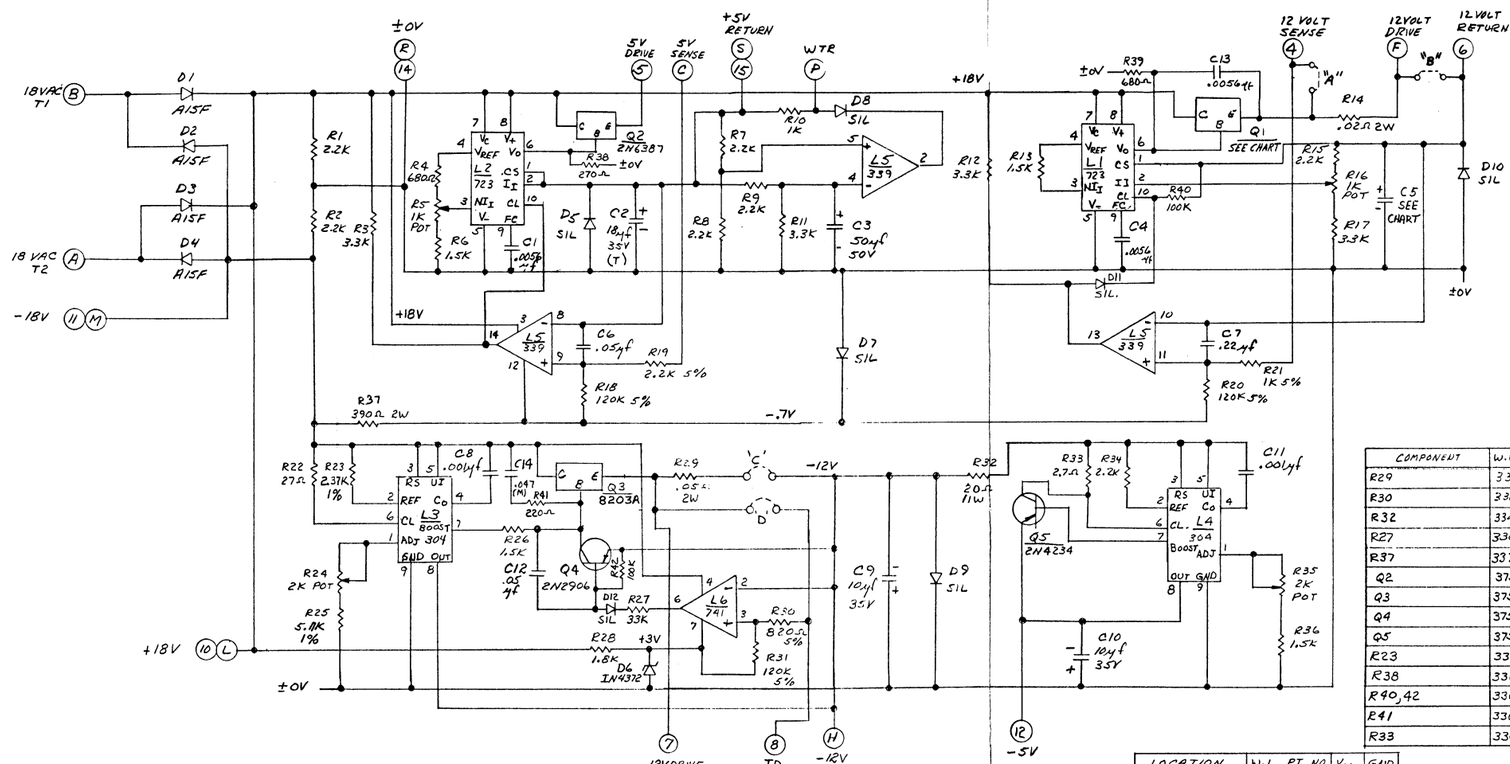
MILLIMETERS IN PARENTHESIS.
TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

DO NOT SCALE

HOLE LEGEND & TOLERANCES

HOLE DIA	TOLERANCE
.0135 - .125	+.003 -.001
.126 - .250	+.004 -.001
.251 - .500	+.005 -.001

SYM.	DESCRIPTION	QTY.
A		



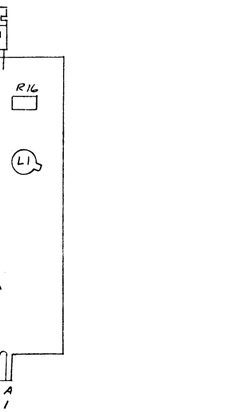
COMPONENTS	W.L. PART NO.
C7	300-1926
C6,12	300-1900
C2,	300-4018
C3,	300-3010
C9,10	300-4032
C8,11	300-1906
C1, 4, 13	300-1915
C14	300-2147
D1,2,3,4	380-3008
D5,7,8,9,10,11,12	380-1001
D6	380-2129
R1,2,7,8,9,15,34	330-3022
R3,11,12,17,	330-3033
R4,39	330-2068
R5,16	336-1014
R6,13,24,36	330-3015
R10,	330-3010
R14,	334-0032
R18,20,31	330-5013
R22	330-1027
R24.35	336-1022
R25	330-3052
R28	330-3018

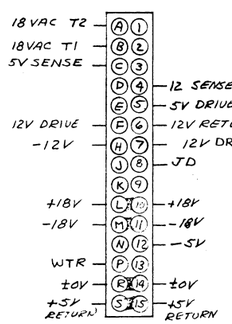
COMPONENT	W.L. PT.NO
R29	334-0032
R30	330-2083
R32	334-0003
R27	330-4033
R37	337-2039
Q2	375-1052
Q3	375-1053
Q4	375-1017
Q5	375-1024
R23	333-0093
R38	330-2027
R40,42	330-5010
R41	330-2022
R33	330-0027

LOCATION	W.L. PT. NO.	V_{CC}	GND
L1,2	376-0066	—	5
L3,4	376-0134	-	9
L5	376-0240	—	—
L6	376-0074	—	—

VARIATION CHART					
	Q1	D1, D3	'C', D'	C5	'A, B'
7156	375-1052	IN	IN	10µf	IN
7156-1	375-1035	OUT	IN	220µf -300-4045	OUT
7156-2	375-1035	OUT	OUT	220µf -300-4045	OUT

COMPONENT	W.L. PT.NO
R19	330-3023
R21	330-3011





NOTE: FOR USE WITH WANG MONITOR, REMOVE JUMPERS "A", "B" AND DIODES 1 & 3.

E-REV
2

NO.	REVISION	BY	DATE
0	ORIGINATED PER DWG# E3342 APP'D: 11-8-77	EBA	5-9-77
1	REVISED PER ECN# 726 APP'D: 11-8-77	EBA	6-28-77
2	REVISED PER ECN# 7177 APP'D: 11-8-77	EBA	7-14-77
3	REVISED PER ECN# 7405 APP'D: 11-8-77	EBA	10-10-77
4	ECN# 8199 APP'D: 1-24-78	P.R.	1-24-78
5	REVISED PER ECN# 8975 APP'D: DF 7-6-78	D.T.	7-6-78
6	REVISED PER ECN# APP'D	MP.M.	10-13-78

QTY.	ITEM
NEXT ASSY.	

WANG PART NO. | DRAWING NO. | DESCRIPTION

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL

FINISH

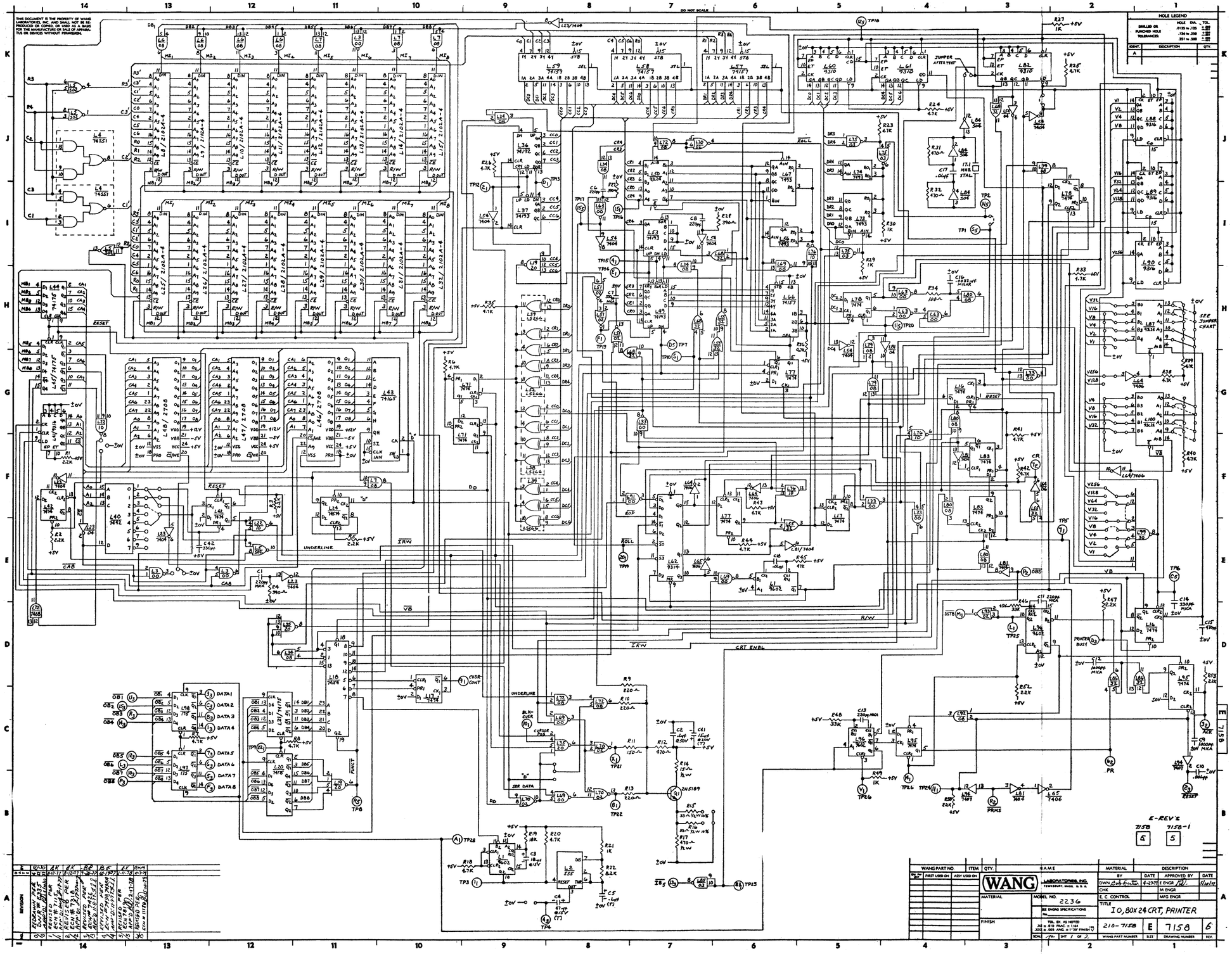
MODEL NO. 928,2200F, 2210, 2236
SEE ENGRG. SPECIFICATIONS
No.

TOL. EX. AS NOTED
XX ± FRAC. ±
XXX ± ANG. ± FINISH √
SCALE | SHT | OF

	BY	DATE	APPROVED BY	DATE
DWN	EBA	5-9-77	E ENGR	5-9-77
CHK			M ENGR	
			MFG ENGR	

TITLE: P.S. REGULATOR WITH FOLD BACK

210-7156 | D | 7156 | 6
WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.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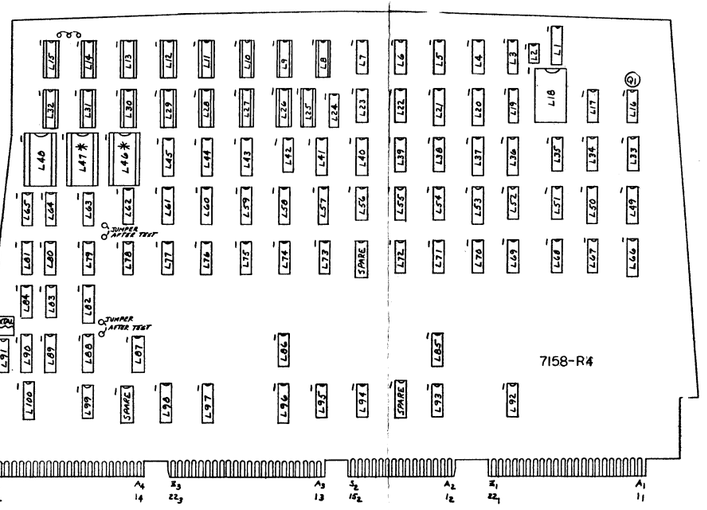
DO NOT SCALE
HOLE LEGEND
DRILLED OR PUNCHED HOLE TOLERANCES
HOLE DIA. TOL.
.0135 to .125 ± .005
.136 to .390 ± .006
.201 to .500 ± .008
IDENT. DESCRIPTION QTY.
A
JUMPER AFTER TEST
+5V
+0V
-5V
-15V
+12V
-12V
RESET
CAB
IRW
R/W
VB
ROLL
UNDERLINE
CURSOR CONT
CRT ENBL
SER DATA
DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
DATA 6
DATA 7
DATA 8
SEE JUMPER CHART
E-REV'S
7158 5
7158-1 5
WANG LABORATORIES, INC.
TEWKSBURY, MASS. U.S.A.
MODEL NO. 2236
SEE ENGRG SPECIFICATIONS
TOL. EX. AS NOTED
.XX ± .010 FRAC ± 1/64
.XXX ± .005 ANG. ± 1° 30' FINISH
SCALE NONE SHT 1 OF 2
210-7158 E 7158 6
WANG PART NO. SIZE DRAWING NUMBER REV.
TITLE 10,80X24 CRT, PRINTER
MATERIAL FINISH
BY DATE APPROVED BY DATE
DWN Bob Brown 4-23-79 E ENGR 5/16/79
CHK M ENGR
E.C. CONTROL MFG ENGR
REVISION
REVISED PER ECN #1 (7-12-79)
REVISED PER ECN #2 (8-27-79)
REVISED PER ECN #3 (10-19-79)
REVISED PER ECN #4 (11-7-79)
REVISED PER ECN #5 (11-28-79)
REVISED PER ECN #6 (3-11-80)

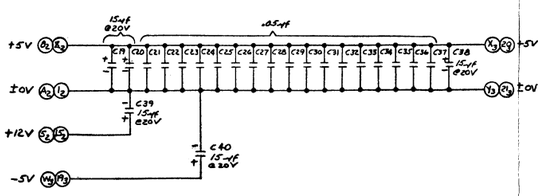
LOCATION	WL. PT. NO.	VCC	GND
L1, 96	376-0109	16	8
L2	376-0126	8	1
L3,33,63,63,93	376-0002	14	7
L4	376-0184	14	7
L5	376-0199	14	7
L6,7,34,72,73 80,92	376-0081	14	7
L8-15,25-32	376-9002	10	9
L16,17,42,71,77, 78,83,95	376-0006	14	7
L18	376-0090	24	12
L19,35	376-0004	14	7
L20,21,44,45, 87,98	376-0119	16	8
L22,76	376-0003	14	7
L23,54,85	376-0010	14	7
L24	376-0202	14	7
L36	376-0190	16	8
L38,39,52	376-0198	14	7
L40	376-0008	16	8
L41,88,89,90	376-0094	16	8
L43	376-0105	16	8
L46,47,48	377-0217	24	12
L37,49,53	376-0053	16	8
L50,87,100	376-0120	16	8
L51,70,93	376-0016	14	7
L55,68,86	376-0093	14	7
L56,67,73,74	376-0011	5	10
L57,58,59,66	376-0082	14	8
L60,61,82	376-0191	16	8
L62	376-0108	16	8
L64,65	376-0055	14	7
L75,85	376-0028	14	7
L84	376-0197	14	7
L94	376-0056	14	7
L99	376-0031	14	7
L8-15,25-32	376-9002		
L18,48	376-9003		
* NOT LOADED L46,47			

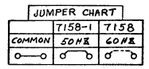
SPARES		
LOCATION	TYPE	QTY
L3	7400	1
L22	7410	1
L23	7408	1
L26	74S74	1
L51	7402	1
L64	7406	1
L65	7406	4
L72	7408	1
L79	7408	1
L81	7409	1
L85	7403	3
L86	7432	2
L91	7400	3
L92	7408	3
L93	7402	3
L94	7407	4
L75	7403	1
L84	74S04	3

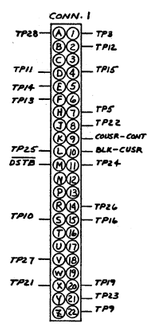
VARIATION CHART			
210 = 209 + 377 OR 378			
MODEL	209	210	L48
CYRILLIC/LATIN 2236	7158-1	7158-18	378-2413
SWISS/FRENCH 2236	7158-1	7158-1C	378-2414
AZERTY 2236	7158-1	7158-1D	378-2415
SWEDISH 2236	7158-1	7158-1F	378-2416
NORWAY 2236	7158-1	7158-1F	378-2417
U.K. 2236	7158-1	7158-1G	378-2418
NETHERLANDS 2236	7158-1	7158-1H	378-2419
GERMAN 2236	7158-1	7158-1J	378-2420
GREEK/LATIN 2236	7158-1	7158-1K	378-2421

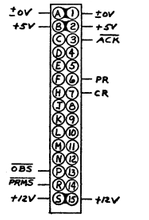
PARTS LIST	
COMPONENT	WL. PT. NO.
R1,2,3,5,41,50-53	330-3022
R4,27,28	330-2039
R6,7,8,16,29,23,35,45, 46,33,35,36,38,39, 40-44	330-3047
R9,10,13	330-2022
R11	330-2015
R12,31,32	330-2047
R14	331-1015
R15,16	331-1033
R19	330-4018
R21,30,37,49,29	330-3010
R22	330-3082
R24	330-2010
R25	330-4047
R26,48	330-4033
R17	331-2047
Q1	375-1021
Q1 TRASI-PAD	375-9001
XTAL	331-0018
C1,11,13	300-5004
C9,12	300-5006
C3	300-4018
C4	300-4020
C5	300-4002
C6,8	300-1220
C7,14	300-5007
C10	300-1906
C15	300-1470
C16	300-2033
C17,18	300-1903
C19,20,38-41	300-4022
C21-37	300-1900
C2	300-1930
C42	300-1330
L8-15,25-32 SKT	377-0065
L48 SKT	376-9003

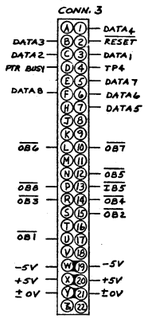


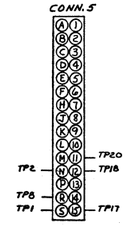


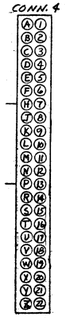












WANG PART NO.	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
FIRST USED ON	ASSY USED ON		WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.		BY / DATE / APPROVED BY / DATE
					DWN JSG 4-27-78 / ENGR
			MODEL NO. 2236	MATERIAL	CHK / M ENGR
			SEE ENGRG SPECIFICATIONS No.		E. C. CONTROL / MFG ENGR
				FINISH	TITLE: 10,80X24 CRT, PRINTER
			TOL EX. AS NOTED .XX ± .010 FRAC. ± 1/64 .XXX ± .005 ANG. ± 1°30' FINISH		210-7158 / E / 7158 / 6
			SCALE NONE SHT 2 OF 2		WANG PART NUMBER / SIZE / DRAWING NUMBER / REV.

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DO NOT SCALE

REVISION	BY	DATE	APPROVED BY	DATE
A	LARSON PMF ADDED 6429	5-29-77		
B	REVISED PER ECN # 7131 APPD [illegible]	6-11-77	[illegible]	6-29-77
C	REVISED PER ECO 7158	6-17-77	[illegible]	7-11-77
D	REVISED PER ECO 7172	6-28-77	[illegible]	8-1-77
E	REVISED PER ECO 7171	7-12-77	[illegible]	8-1-77
F	REVISED PER ECO 7193	9-22-77	[illegible]	9-23-77
G	REVISED PER ECO 7245	10-31-77	[illegible]	11-1-77
H	REVISED PER ECO 7245	11-1-77	[illegible]	11-3-77
J	REVISED PER ECO 7245	11-3-77	[illegible]	11-3-77
K	REVISED PER ECO 7245	11-3-77	[illegible]	11-3-77
L	REVISED PER ECO 7245	11-3-77	[illegible]	11-3-77
M	REVISED PER ECO 7245	11-3-77	[illegible]	11-3-77
N	REVISED PER ECO 7245	11-3-77	[illegible]	11-3-77

SEE SHEET 2

7292-1 E-REV 5 | 7292 E-REV 4

ALL BOARDS BUILT PRIOR TO REV. 3 SEE ECN 7292 REV 5

WANG PART NO.	ITEM	QTY.	NAME	MATERIAL	DESCRIPTION
FIRST USED ON	ASSY USED ON		WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.	BY	DATE / APPROVED BY / DATE
			MODEL NO. 2236 SEE ENGNG SPECIFICATIONS	DWN EBA 5-9-77 / E ENGR [illegible] 5/11/77	
				CHK	M ENGR
				E. C. CONTROL	MFG ENGR
			FINISH	TITLE INTERACTIVE TERMINAL	
			TOL. EX. AS NOTED .XX ± .010 FRAC. ± 1/64 .XXX ± .005 ANG. ± 1°30' PARTS	210-7292	E / 7292 / 14
			SCALE 1/1 SHT 1 OF 2	WANG PART NUMBER	SIZE / DRAWING NUMBER / REV

E 7292

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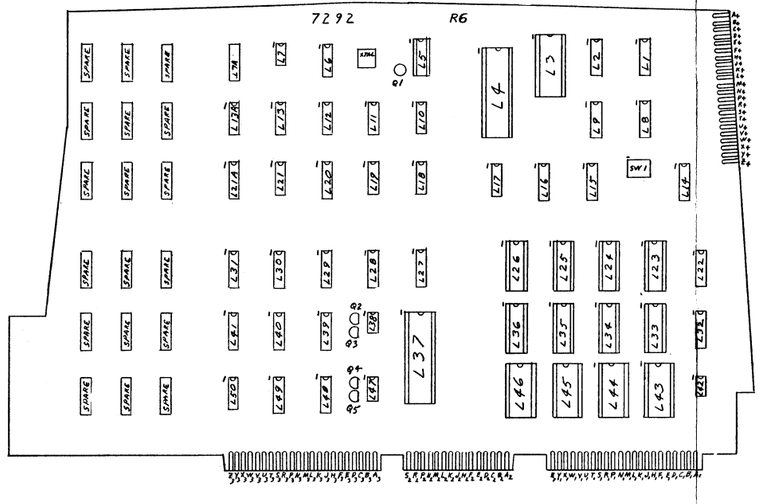
DO NOT SCALE

HOLE LEGEND

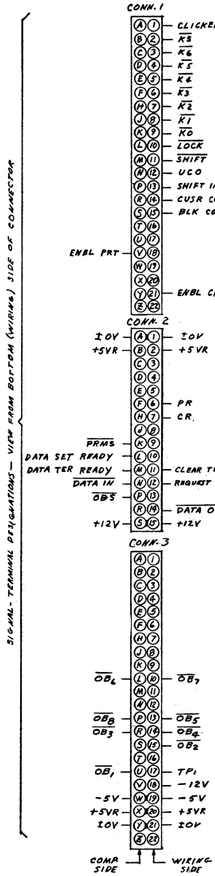
	HOLE DIA.	TOL.
DRILLED OR PUNCHED HOLE TOLERANCES:	.031 to .125	±.002
	.126 to .250	±.003
	.251 to .500	±.005

SYMBOL	DESCRIPTION	QTY.
A		



LOCATION	W.L. PART NO.	TYPE
L1, 2, 8, 9	376-0189	8T97
L3	SEE CHART	8228
L4	SEE CHART	8080
L5	SEE CHART	8224
L6, 10	376-0010	7404
L7, 42	376-0126	555
L11, 12, 21, 50	376-0006	7474
L13	376-0003	7410
L13A, 17	376-0081	7408
L18, 15	376-0185	8T98
L16, 27	376-0096	9321
L18	376-0093	7432
L19	376-0002	7400
L20, 49	376-0080	74123
L21A, 29, 36, 38, 41, 48	376-0119	74175
L22, 32	376-0183	74173
L23-26, 33-36	SEE CHART	2101
L28	376-0077	75154
L30, 40	376-0094	74161
L37	SEE CHART	1402
L38, 47	376-0076	75150
L43-46	SEE CHART	2708
L7A	376-0012	7451

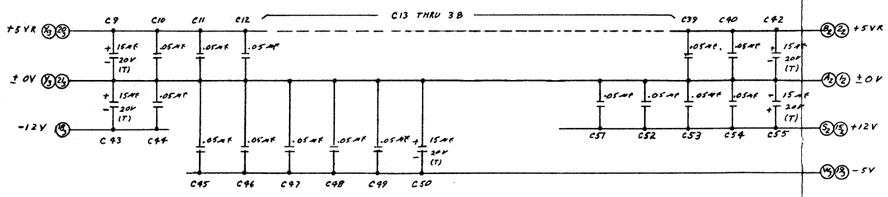
I.C. TYPE	LOCATION	SPARE
7410	L13	1
7400	L19	2
74123	L20	1
7404	L6	1
7408	L13A	1
7432	L18	1
7451	L7A	1



SIGNAL - TERMINAL DESIGNATIONS — VIA PANA BOARD (WIRING) SIDE OF CONNECTOR

COMPONENT	WL. PART NO.	TYPE
R1	330-2033	330Ω ¼W 10%
R2	330-3047	4.7K ¼W 10%
R30, 3, 5, 6, 12-14, 17-21, 23, 32	330-3010	1K ¼W 10%
R4, 7, 22, 31	330-3022	2.2K ¼W 10%
R8	330-5010	100K ¼W 1%
R9	330-4047	47K ¼W 10%
R10, 11	330-5047	470K ¼W 10%
R15, 16	330-1068	68Ω ¼W 10%
R17	330-4022	22K ¼W 10%
R23	330-4033	33K ¼W 10%
R25-28	SEE CHART	120Ω ½W 10%
XTAL	SEE CHART	
D1	380-4000	1N4004
C1	300-1068	68PF CER
C2, 8	300-1903	.01MF 25V CER
C3	300-3009	35MFD 16V ELECT
C9, 10-19, 44-48, 51-54	300-1900	.05MF 12V CER
C5	300-1039	39PF CER
C6	300-1470	470PF CER
C7	300-4011	.68MF 35V (T)
C9, 42, 43, 50, 55	300-4022	15MF 20V (T)
C41	300-1330	330PF CER
Q1	375-0017	2N3014
Q3A	375-1012	MPS 6512
Q2, 5	375-1014	MPSG 518
Q1	375-9007	PAD
SW1	325-1501	ROCKER SWITCH
L3	376-9015	SOCKET 28 PIN
L4, 37	376-9011	SOCKET 40 PIN
L5	376-9002	SOCKET 16 PIN
# L43-46	376-9003	SOCKET 24 PIN
# L23-26, 33-36	376-9010	SOCKET 22 PIN

LOAD PER CHART



PROM CHART

210 = 209 + 377 OR 378

MODEL	209	210	L23	L24	L25	L26	L33	L34	L35	L36	XTAL	L43	L44	L45	L46	L3	L4	L5	L37	R25-28
2236	7292-1	7292A	377-0308				377-0308				321-0012	378-2085				377-0338	377-0269	377-0337	377-0071	331-1012
DIAG. TEST	7292-1	7292B									321-0012	378-2135								
2236 D	7292-1	7292-1A	377-0308	377-0308	377-0308	377-0308	377-0308	377-0308	377-0308	377-0308	321-0028	378-2278	378-2279			377-0338	377-0269	377-0337	377-0071	331-1012
9017-5C	7292-1	7292-1B	377-0308	377-0308	377-0308	377-0308	377-0308	377-0308	377-0308	377-0308	321-0028	378-2181	378-2182			377-0338	377-0269	377-0337	377-0071	331-1012
2236D KATAKANA	7292-1	7292-1C	377-0308	377-0308	377-0308	377-0308	377-0308	377-0308	377-0308	377-0308	321-0028	378-2278	378-2283			377-0338	377-0269	377-0337	377-0071	331-1012
CYRILLIC/Latvian 2236	7292-1	7292-1D											378-2602							
ARABIC 2236	7292-1	7292-1E											378-2933-01							
HEBREW 2236	7292-1	7292-1F											378-2929							
NATIONAL BLANKS 2236	7292-1	7292-1G											378-2925							
SWISS/GERMAN 2236	7292-1	7292-1H											378-2926							
SWISS/FRENCH 2236	7292-1	7292-1J											378-2927							
GERMAN 2236	7292-1	7292-1K											378-2928							
ARABIC/Latin 2236	7292-1	7292-1L											378-2927							
SWEDISH 2236	7292-1	7292-1M											378-2930							
U.K. 2236	7292-1	7292-1N											378-2931							

REV.	REVISION	DATE	APPROVED
A	REVISED P/N'S, ECN # 2000 ADDED REF. DES.	1-26-77	

WANG PART NO.	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
QTY PER ASSY	FIRST USED ON	ASSY USED ON	WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.		
			MATERIAL	MODEL NO. 2236	BY / DATE / APPROVED BY / DATE
				SEE ENGRG SPECIFICATIONS No.	DWN 9-3-76 / E ENGR
			FINISH	TOL. ALL AS NOTED .XX ± .010 .XXX ± .005 ANG. ± 1/2° FINISH	CHK / M ENGR
				SCALE 1/1 SHT 2 OF 2	E.C. CONTROL / MFG ENGR
					TITLE INTERACTIVE TERMINAL
					210-7292 / E / 7292 / 1A
					WANG PART NUMBER / SIZE / DRAWING NUMBER / REV.

7292

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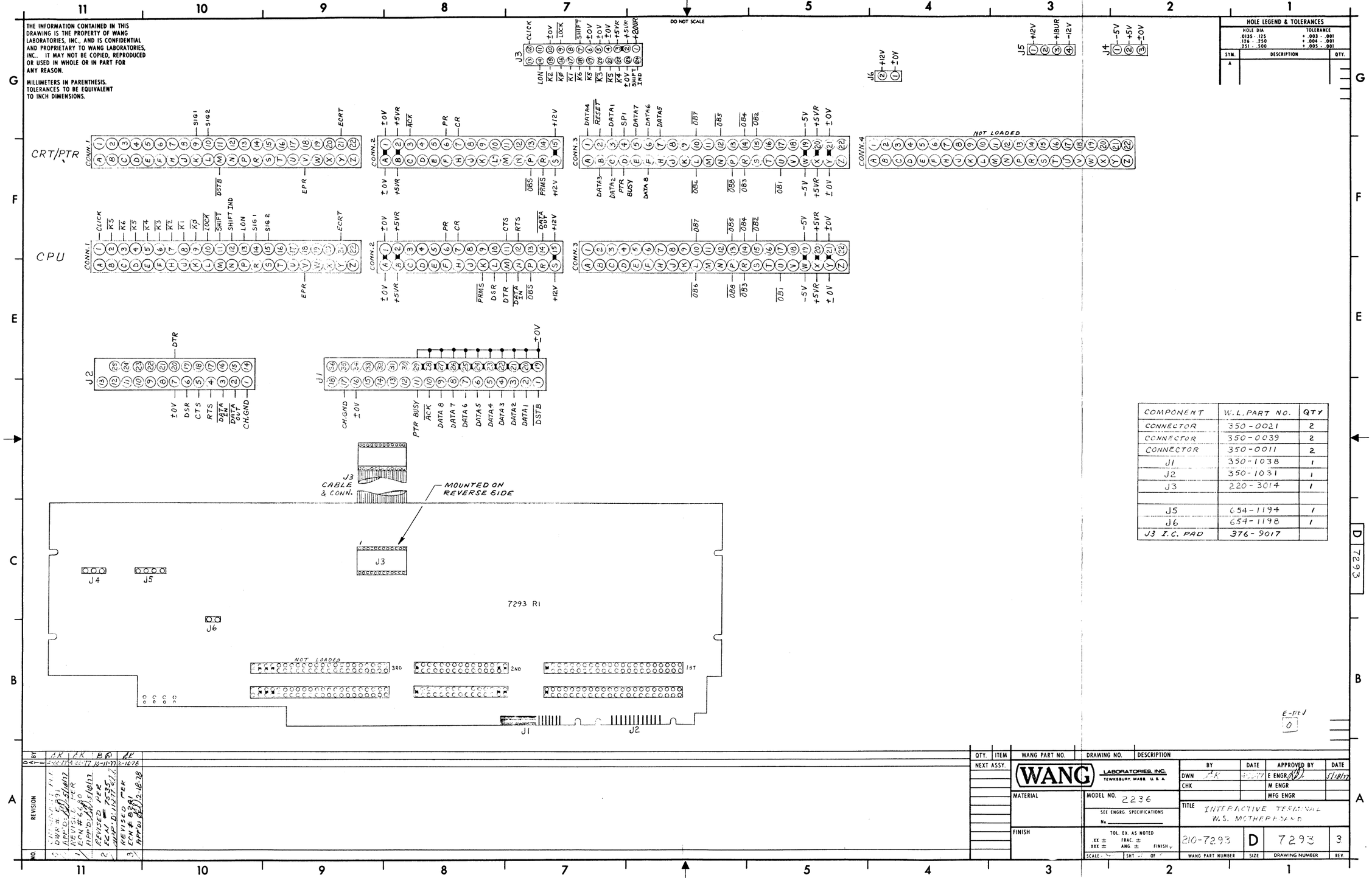
MILLIMETERS IN PARENTHESIS.
TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

DO NOT SCALE

HOLE LEGEND & TOLERANCES	
HOLE DIA	TOLERANCE
.0135 - .125	+ .003 - .001
.126 - .250	+ .004 - .001
.251 - .500	+ .005 - .001

SYM.	DESCRIPTION	QTY.
A		



COMPONENT	W.L. PART NO.	QTY
CONNECTOR	350-0021	2
CONNECTOR	350-0039	2
CONNECTOR	350-0011	2
J1	350-1038	1
J2	350-1031	1
J3	220-3014	1
J5	654-1194	1
J6	654-1198	1
J3 I.C. PAD	376-9017	

NO	REVISION	BY	DATE
1	DWN #: E-691 APP'D: AR/SLEIN REVISED PER ECN # 5676 APP'D: AR/SLEIN	AR	10-11-77
2	REVISED PER ECN # 7535 APP'D: AR/SLEIN	AR	10-11-77
3	REVISED PER ECN # 8241 APP'D: AR/SLEIN	AR	10-16-78

QTY.	ITEM	WANG PART NO.	DRAWING NO.	DESCRIPTION
NEXT ASSY.				

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL

FINISH

MODEL NO. 2236
SEE ENGRG. SPECIFICATIONS
No.

TOL. EX. AS NOTED
XX ± FRAC ±
XXX ± ANG ± FINISH √

SCALE - SHT OF

	BY	DATE	APPROVED BY	DATE
DWN	AR	10-11-77	E ENGR	5/18/77
CHK			M ENGR	
			MFG ENGR	

TITLE: INTERACTIVE TERMINAL W.S. MOTHERBOARD

210-7293 | D | 7293 | 3
WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.

E-PM 0

7293 D

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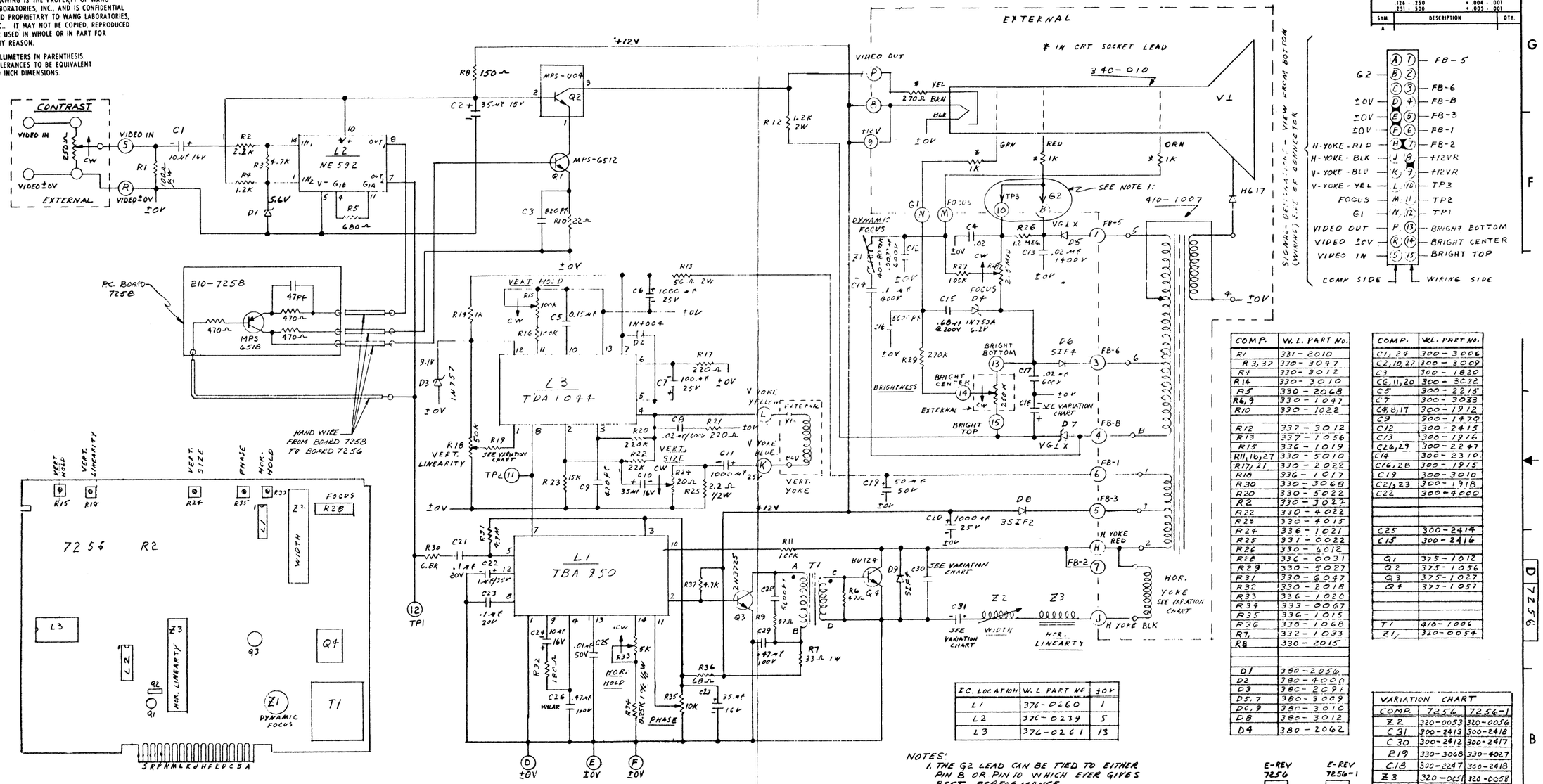
MILLIMETERS IN PARENTHESIS. TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

DO NOT SCALE



HOLE LEGEND & TOLERANCES		
HOLE DIA.	TOLERANCE	
.0125 - .125	+ .003 - .001	
.126 - .250	+ .004 - .001	
.251 - .500	+ .005 - .001	
SYM.	DESCRIPTION	QTY.
A		

COMP.	WL. PART No.
R1	331-2010
R3, 37	330-3047
R4	330-3012
R14	330-3010
R5	330-2068
R6, 9	330-1047
R10	330-1022
R12	337-3012
R13	337-1056
R15	336-1019
R11, 16, 27	330-5010
R17, 21	330-2022
R18	336-1017
R30	330-3068
R20	330-5022
R2	330-3022
R22	330-4022
R23	330-4015
R24	336-1021
R25	331-0022
R26	330-6012
R28	336-0031
R29	330-5027
R31	330-6047
R32	330-2018
R33	336-1020
R34	333-0067
R35	336-1015
R36	336-1068
R7	332-1033
R8	330-2015
D1	380-2056
D2	380-4000
D3	380-2091
D5, 7	380-3009
D6, 9	380-3010
D8	380-3012
D4	380-2062

COMP.	WL. PART No.
C1, 24	300-3006
C2, 10, 27	300-3009
C3	300-1820
C6, 11, 20	300-3032
C5	300-2215
C7	300-3033
C4, 8, 17	300-1912
C9	300-1420
C12	300-2415
C13	300-1916
C26, 29	300-2247
C14	300-2310
C16, 28	300-1915
C19	300-3010
C21, 23	300-1918
C22	300-4000
C25	300-2414
C15	300-2416
Q1	375-1012
Q2	375-1056
Q3	375-1027
Q4	373-1057
T1	410-1006
Z1,	320-0054

IC. LOCATION	W. L. PART NO.	40V
L1	376-0260	1
L2	376-0239	5
L3	376-0261	13

NOTES:
1. THE G2 LEAD CAN BE TIED TO EITHER PIN B OR PIN 10 WHICH EVER GIVES BEST PERFORMANCE.

VARIATION CHART		
COMP.	7256	7256-1
Z2	320-0053	320-0056
C31	300-2413	300-2418
C30	300-2412	300-2417
R19	330-3068	330-4027
C18	300-2247	300-2418
Z3	320-0051	320-0058
EXTERNAL	336-0035	336-0035
HOR. YOKE	320-0052	320-0057
FLY BACK	410-1007	410-1007

E-REV 7256: 2
E-REV 7256-1: 2

NO.	REVISION	BY	DATE
0	ORIGINATED PER ECN # 6047 APPROVED	RK	11-5-76
1	REVISED PER ECN # 6346 APPROVED	RK	1-7-77
2	REVISED PER ECN # 6361 APPROVED	RK	1-7-77
3	REVISED PER ECN # 6402 APPROVED	RK	2-1-77
4	REVISED PER ECN # 6378 APPROVED	RK	2-1-77
5	REVISED PER ECN # 6372 APPROVED	RK	2-1-77
6	REVISED PER ECN # 6999 APPROVED	RK	3-7-77
7	REVISED PER ECN # 6978 APPROVED	RK	3-7-77
8	REVISED PER ECN # 7078 APPROVED	RK	3-21-77
9	REVISED PER ECN # 7131 APPROVED	RK	3-21-77

QTY.	ITEM NEXT ASSY.	WANG PART NO.	DRAWING NO.	DESCRIPTION

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL

FINISH

MODEL NO. 9" & 12" WANG MONITOR
SEE ENGRG. SPECIFICATIONS
No.

TOL EX. AS NOTED
XX ± FRAC. ±
XXX ± ANG. ± FINISH √

SCALE 4/1 SHT 1 OF 1

BY	DATE	APPROVED BY	DATE
DWN RK	11-5-76	E ENGR	4/1/76
CHK	12-2-76	M ENGR	
		MFG ENGR	

TITLE: ELECTRONICS FOR 9" AND 12" MONITOR

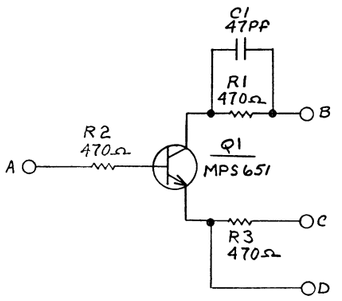
SEE CHART | D | 7256 | 9

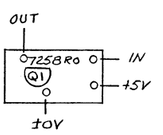
WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.

D 7256 9

DO NOT SCALE

COMP	W.L.PT. NO.
R1,2,3	330-2047
C1	300-1047
Q1	375-1014





HOLE LEGEND

DRILLED OR PUNCHED HOLE TOLERANCES:	HOLE DIA.	TOL.
	.0135 to .125	+.003 −.001
	.126 to .250	+.004 −.001
	.251 to .500	+.005 −.001

IDENT.	DESCRIPTION	QTY.
A		

B 7258

E. REV 1

NO.	REVISION	BY	DATE
0	ORIGINATED PER DWR # E370 APPD:	EBA	7-20-77
1	REVISED PER ECN # T378 APPD:	dK	9-8-77

WANG PART NO.	ITEM	QTY.	NAME	MATERIAL	DESCRIPTION
Qty. Per Unit	FIRST USED ON	ASSY USED ON			

WANG LABORATORIES, INC. TEWKSBURY, MASS. U. S. A.

MATERIAL

MODEL NO. WANG MONITOR

SEE ENGRG SPECIFICATIONS No.

FINISH

TOL. EX. AS NOTED
.XX ± .010 FRAC. ± 1/64
.XXX ± .005 ANG. ± 1°30' FINISH 125

SCALE 2/1 SHT 1 OF 1

BY	DATE	APPROVED BY	DATE
DWN EBA	7-20-77	E ENGR	9-20-77
CHK		M ENGR	
E. C. CONTROL		MFG ENGR	

TITLE: BLANKING CKT

210-7258	B	7258	1
WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.

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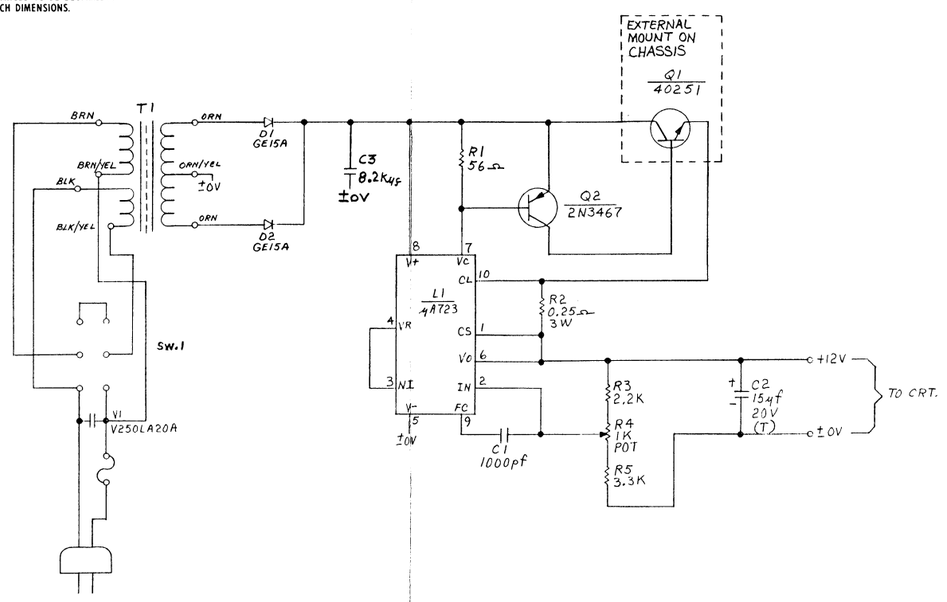
MILLIMETERS IN PARENTHESIS. TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

DO NOT SCALE

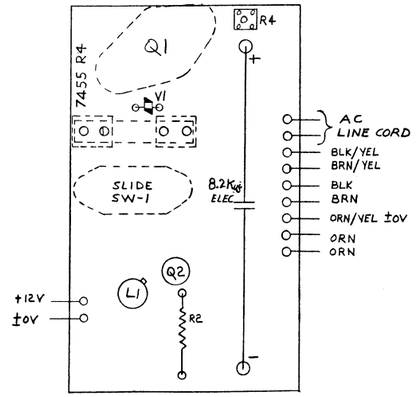
HOLE LEGEND & TOLERANCES	
HOLE DIA	TOLERANCE
.0135 - .125	+ .003 - .001
.126 - .250	+ .004 - .001
.251 - .500	+ .005 - .001

SYM.	DESCRIPTION	QTY.
A		



LOCATION	W.L. PART NO.	GND. PIN
L1	376-0066	5

COMPONENT	W.L. PART NO.
R1	330-1056
R2	334-0017
R3	330-3022
R4	336-1014
R5	330-3033
C1	300-5006
C2	300-4022
D1, D2	380-3008
SW1.	325-2112
FUSE	360-1006
FUSE HOLDER	360-0006
C3	300-3078
V1	380-5001
Q1 SOCKET	375-9022
Q2	375-1026



NO.	REVISION	BY	DATE	APPROVED BY	DATE
0	ORIGINATED PER DWR #E491 APP'D: 12-9-77	ER	9-14-77	G.D. 12-9-77	
1	Revised Per ECN# 7769 APP'D: 12-9-77	ER	12-9-77		
2	REVISED PER ECN #8195 APP'D: 3-22-78	AR	2-22-78		
3	REVISED PER ECN #8944 APP'D: 7-26-78	ZR	7-26-78		
4	REVISED PER ECN 10745 APP'D: 4-14-79	ETR	3-8-79		

QTY.	ITEM	WANG PART NO.	DRAWING NO.	DESCRIPTION
NEXT ASSY.				

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

BY	DATE	APPROVED BY	DATE
DWN	7-14-77	E ENGR B. Solomon	12-9-77
CHK	12-9-77	M ENGR	
		MFG ENGR	

MATERIAL

MODEL NO. 9" & 12" CRT

SEE ENGRG. SPECIFICATIONS No.

FINISH

TOL. EX. AS NOTED .XX ± FRAC. ± .XXX ± ANG. ± FINISH √

SCALE NONE SHT 1 OF 1

TITLE REGULATOR

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
210-7455	D	7455	4

E-REV 1

D 7455

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MILLIMETERS IN PARENTHESIS.
TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

DO NOT SCALE

CONTRAST
VIDEO IN
VIDEO ±0V
EXTERNAL
NOT LOADED FOR 7456-2

VARIATION CHART			
COMP	7456	7456-1	7456-2
R19	330-3068	330-4027	330-3063
C30	300-2412	300-2417	300-2412
C31	300-2413	300-2418	300-2413
Z2	320-0053	320-0056	320-0053
Z3	320-0051	320-0058	320-0051
HOR. YOKE	320-0052	320-0057	320-0052
FLY-BACK	410-1007	410-1008	410-1007
R5	330-2068	330-2068	330-3068

*COMPONENTS NOT LOADED FOR 7456-2	
R9,10,40	330-2047
R11	330-2010
R12	330-1022
R44	337-3012
C3	330-1047
C15	300-1906
Q5	300-4022
Q2	375-1014
D4,10	375-1056
C32	380-1001
Q1	300-1047
	375-1012

EXTERNAL
* IN CRT SOCKET LEAD
340-0101
VIDEO OUT
SEE NOTE 1:
SEE CHART
DYNAMIC FOCUS
SIGNAL DESIGNATIONS - VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

HOLE LEGEND & TOLERANCES	
HOLE DIA	TOLERANCE
.0135 - .125	+.003 - .001
.126 - .250	+.004 - .001
.251 - .500	+.005 - .001

SYM.	DESCRIPTION	QTY.
A		

	A 1		FB-5
G2	B 2		FB-6
±0V	C 3		FB-8
±0V	D 4		FB-3
±0V	E 5		FB-1
H-YOKE-RED	F 6		FB-2
H-YOKE-BLK	H 7		+12VR
V-YOKE-BLU	J 8		+12VR
V-YOKE-YEL	K 9		G2
FOCUS	L 10		TP2
G1	M 11		TP1
VIDEO OUT	N 12		BRIGHT BOTTOM
VIDEO ±0V	P 13		BRIGHT CENTER
VIDEO IN	R 14		BRIGHT TOP
COMP SIDE	S 15		WIRING SIDE

IC. LOCATION	W. L. PART NO.	±0V
L1	376-0260	1
L2	376-0239	5
L3	376-0261	13

NOTES:
1. THE G2 LEAD CAN BE TIED TO EITHER PIN 8 OR PIN 10 WHICH EVER GIVES BEST PERFORMANCE.

E-REV 7456: 3 | E-REV 7456-1: 3 | E-REV 7456-2: 3

COMP.	W. L. PART No.
R2	330-3022
R 3,37	330-3047
R4	330-3012
R14	330-3010
.	-
R6, 39, 44	330-1047
R8	330-2015
R9, 10, 40	330-2047
R12	337-3012
R13	337-1056
R15	336-1019
R16, 27, 38	330-5010
R17, 21	330-2022
R1	331-2010
R30	330-3068
R20	330-5022
R11	330-1022
R22	330-4022
R23	330-4015
R24	336-1021
R25	331-0022
R26	330-6012
R28	336-0031
R29	330-5027
R31	330-6047
R32	330-2018
R18, 33	336-1020
R34	333-0067
R35	336-1015
R36	330-1068
R7	332-1033
R41	330-4027
R42	330-4018
D1	380-2056
D2	380-4000
D3	380-2091
D5, 7	380-3009
D6, 9	380-3010
D8	380-3012
D4, 10	380-1001
Z1	320-0054
R43	330-4068

COMP.	W.L. PART NO.
C1, 24	300-3006
C2, 10, 27	300-3009
C3	300-1906
C9	300-1470
C12	300-2415
C26, 29	300-2247
C14	300-2310
C16, 28	300-1915
C19	300-3010
C21, 23	300-1918
C22	300-4000
C25	300-2414
C18	300-2418
C4, 8, 17	300-1912
C5	300-2215
C6, 11, 20	300-3062
C7	300-3033
C13	300-1916
C32	300-1047
Q1	375-1012
Q2	375-1056
Q3	375-1027
Q4	375-1057
Q5	375-1019
C15	300-4022
T1	410-1006
C33	300-1931

NO.	REVISION	BY	DATE	APPROVED	DATE
9	DWR # 5396 APP'D [illegible] 10-21-77	B.F	8-31-77		
8	REVISED PER ECN # 7776 APP'D: [illegible] 11-28	BD	12-10-77		
7	REVISED PER ECN # 9[illegible] APP'D: [illegible] 2-8-78	AF	2-8-78		
6	REVISED PER ECN # 9[illegible] APP'D: [illegible] 3-8-78	AF	3-8-78		
5	REVISED PER ECN # 10681 APP'D: [illegible] 3-28-79	AF	3-28-79	CB	3-12-79
4	REVISED PER ECN # 10935 APP'D: [illegible] 5-3-79	CB	5-3-79		
3	ECN # 11119 APP'D [illegible] 5-29-79	G.D.	5-29-79		

QTY.	ITEM	WANG PART NO.	DRAWING NO.	DESCRIPTION
NEXT ASSY.				

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL

FINISH

MODEL NO. 9" & 12" WANG MONITOR
SEE ENGRG. SPECIFICATIONS No.

TOL. EX. AS NOTED .XX ± FRAC. ± .XXX ± ANG. ± FINISH √

SCALE — SHT / OF /

BY	DATE	APPROVED BY	DATE
DWN B.F	8-31-77	E ENGR R. Solomon	10-21-77
CHK G.D.	10-21-77	M ENGR	
		MFG ENGR	

TITLE: ELECTRONICS FOR 9" AND 12" MONITOR

SEE CHART	D	7456	5
WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.

D 7456

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DO NOT SCALE

MECH ASSY					
DWG. Nº	W PN	COUNTRY	JUMPERS	Y A x15	MOD. Nº
D-06841-0017	271-1151	SWEDISH	B&E	5&6	928
D-06841-0018	271-1152	GERMAN	D	7	928
D-06841-0019	271-1153	UNITED KINGDOM	—	—	928
D-06841-0020	271-1157	NORWEGIAN	B&D	5&7	928
D-06841-0021	271-1158	AZERTY	A&C	4-8	928
D-06841-0022	271-1159	NETHERLANDS	E	6	928
D-06827-0511	271-1166	GREEK/LATIN	—	—	2236
D-06827-0512	271-1167	CYRILLIC/LATIN	—	—	2236
D-06827-0504	271-1168	SWISS/FRENCH	—	—	2236
D-06827-0506	271-1169	UNITED KINGDOM	—	—	2236
D-06827-0506	271-1170	NETHERLANDS	—	—	2236
D-06827-0509	271-1171	NORWEGIAN	—	—	2236
D-06827-0508	271-1172	SWISS/GERMAN	—	—	2236
D-06827-0507	271-1173	AZERTY	—	—	2236
D-06827-0510	271-1174	GERMAN	—	—	2236
D-06827-0508	271-1175	SWEDISH	—	—	2236

LOADED FOR 2236 ONLY

CLICKER

EM403 D1

2N3725 Q2

R1 560Ω

C1 50µf 50V

R2 82Ω

R3 390Ω

EXTERNAL 100Ω

DS1 SHIFT

2N3014 Q3

R4 1.5K

R5 1K

+5VR

R8 210Ω

2N2906 Q1

R6 8.2K

R7 2.2K

C D E B A

R35 2.2K R36 2.2K R37 2.2K R38 2.2K R39 2.2K

X1 X2 X3 X4 X5 X6 X7

R9 R10 R11 R12 R13 R14 R15 R16 6.8K

L1 74148

A0 A1 A2 GS EI

C2 1000pf

SHIFT

LOCK

R17 R18 6.8K

+5VR

Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

R19 R20 R21 R22 R23 R24 R25 R26 6.8K

L3 74148

Y8 Y9 YA YB YC YD YE YF

R27 R28 R29 R30 R31 R32 R33 R34 6.8K

L4 74148

7408 L2

J1

CLICKER CLG1 AET SHLED LOCK SH KEY DAX +5VR +5VR +17V CLG2 UCO

K2 K0 K1 K4 K5 K3 K6 K7

C3 .05 µf C4 .05 µf C5 .05 µf C6 .05 µf C7 15 µf 20V

+5VR

Q1 Q2 Q3 J1 L1 L2 L3 L4 7229 R10

BOTTOM VIEW

SHIFT LAMP

REVISION	BY	DATE
ECN L215	TW	7/24

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY	DATE
	DWN J. WORLIAK	3/7/79	E ENGR	5/31/79
	CHK		M ENGR	
	QTY		MFG ENGR	
MATERIAL	MODEL NO. SEE CHART	TITLE W. S. KEYBOARD		
	SEE ENGRG. SPECIFICATIONS No. 55-1001			
FINISH	TOL. EX. AS NOTED .XX ± FRAC. ± .XXX ± ANG. ± FINISH √	210-7229	D	7229	0
	SCALE	SHT 1 OF 1	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.

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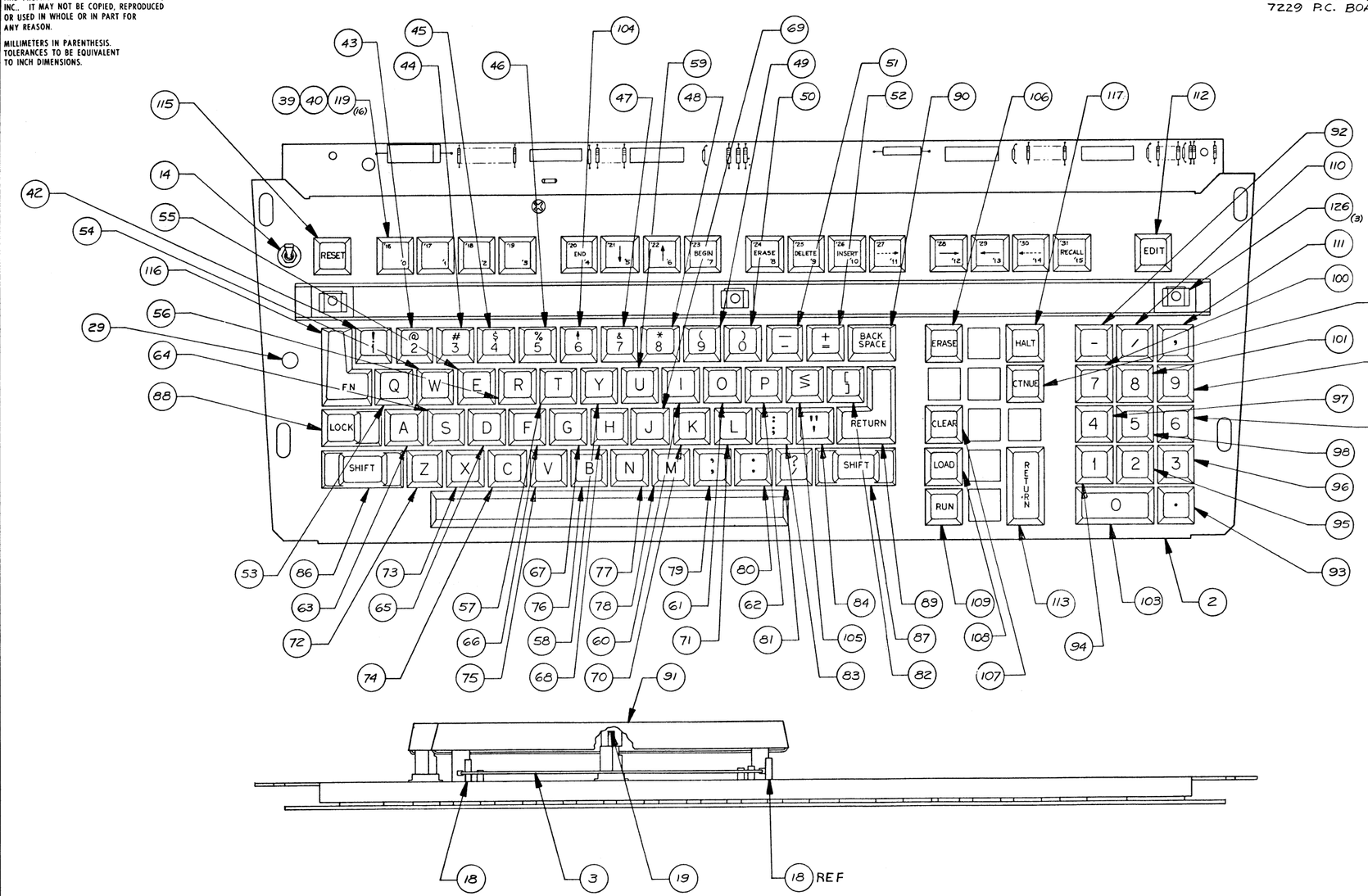
MILLIMETERS IN PARENTHESIS.
TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

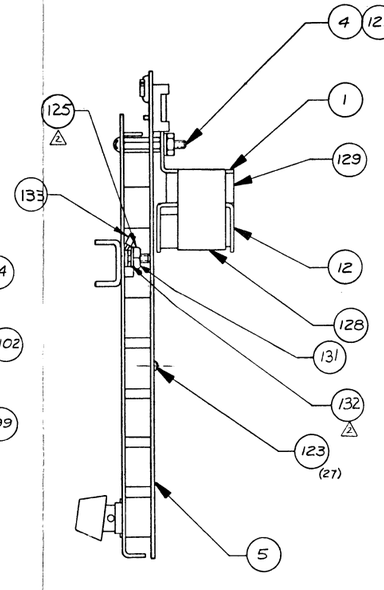
DO NOT SCALE

NOTES:
1. FOR LOCATION OF ITEMS 15,16 & 17 SEE LOADING SKETCH & SCHEMATIC OF 7229 P.C. BOARD.

HOLE LEGEND & TOLERANCES	
HOLE DIA	TOLERANCE
.0135 - .125	+ .003 - .001
.126 - .250	+ .004 - .001
.251 - .500	+ .005 - .001

SYM.	DESCRIPTION	QTY.
A		





SEE PL 6621-090

NO.	REVISION	BY	DATE
1	GEN PER DWR M272	SF	11/8/78
2	REV PER ECN #9615 R3M-1 11-9-78	SF	11/8/78

QTY.	ITEM	WANG PART NO.	DRAWING NO.	DESCRIPTION
NEXT ASSY.				

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

BY	DATE	APPROVED BY	DATE
DWN S.Z.M	10-17-77	E ENGR	
CHK [illegible]	5/11/78	M ENGR	
QTY/1		MFG ENGR DPC	5/19/78

MATERIAL

FINISH

MODEL NO. 2236
SEE ENGRG. SPECIFICATIONS No. ES 1001

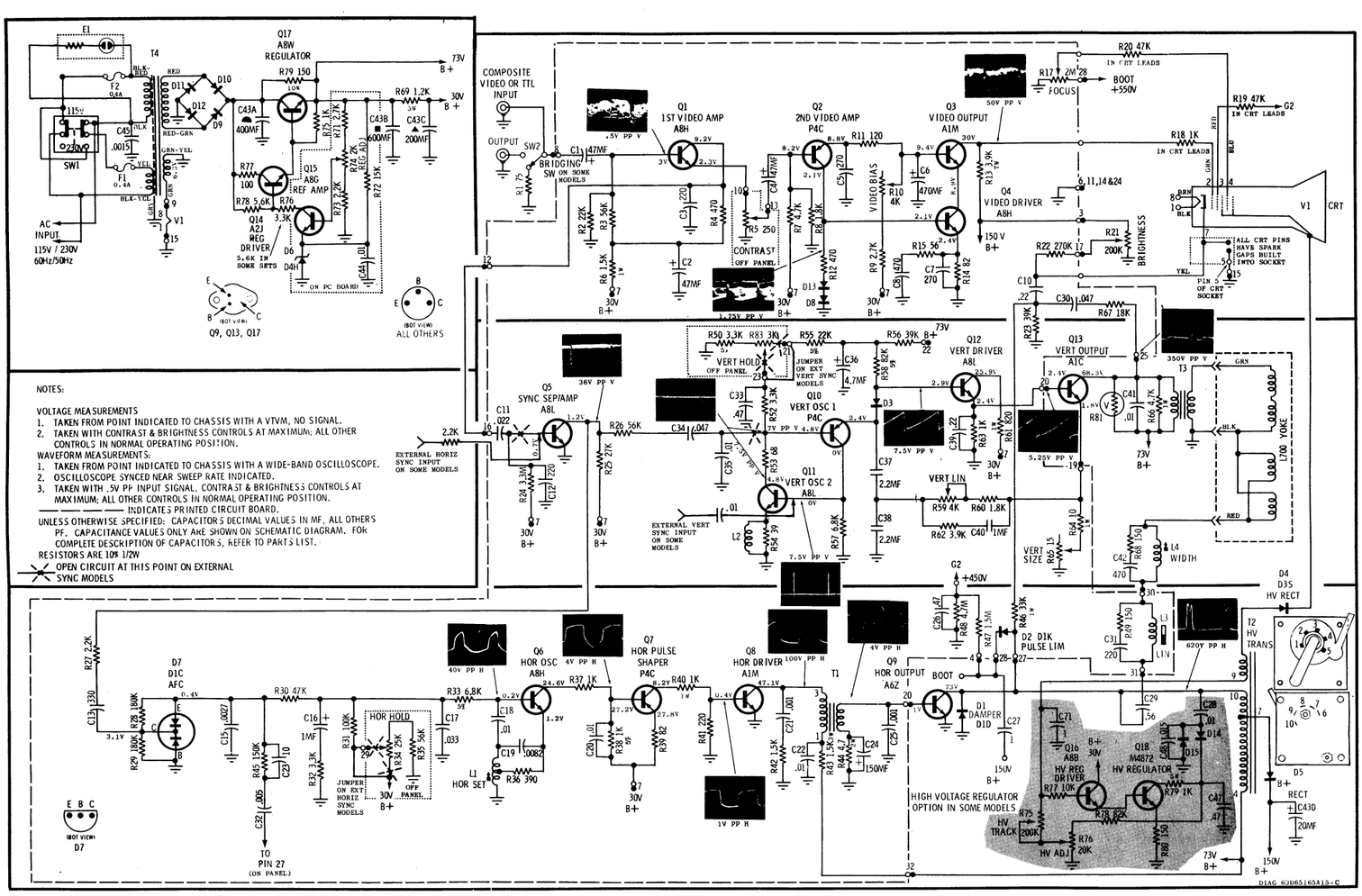
TOL. EX. AS NOTED
XX ± — FRAC. ± —
XXX ± — ANG. ± — FINISH √

SCALE 1:1 | SHT 1 OF 1

TITLE KEYBOARD & BEARING PLATE ASS'Y

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
271-1130	D	6621-090	2

D 050-1299



MOTOROLA VIDEO PCB SCHEMATIC

PICTORIAL SCHEMATIC DIAGRAM SHOWING RELATION BETWEEN COMPONENTS LOCATED ON OFF THE PANEL. (TYPICAL DISPLAY SHOWN)

REMEMBER . . . . REPLACING THE PANEL IS A QUICK & EFFECTIVE WAY TO REPAIR A DISPLAY OR ISOLATE THE DEFECTIVE CIRCUITRY. JUST PLUG IT IN! (FEATURED ON MOST MODELS)

BOOT

VIDEO OUT

HIGH VOLTAGE REGULATOR INPUT (SOME MODELS)

COMPOSITE VIDEO INPUT

HORIZ LIN L3

HIGH VOLT REGULATOR (SOME MODELS)

V. BIAS R10

V. LIN

R17 FOCUS

R65 VERT SIZE

CONTRAST R5

COMP VIDEO TO SYNC SEP.

+450V G2 VOLTAGE

R83 VERT HOLD

R50

Q13 VERT OUTPUT

C29 .56

T3

L5 YOKE

GRN

BLK

RED

+73V

BOOT +550V

2ND ANODE

D4 H.V. RECT

T2 H.V. TRANS

L4 WIDTH

R68 150

C42 470

BOOT DAMPER D1 D1D

Q9 HOR OUTPUT

C27 .1MF

C28 VARIES WITH MODELS

D5 B+ RECT.

+150V

C43D 20MF

R19 (IN CRT LEAD)

R18 1K IN CRT LEADS

R20 (IN CRT LEAD)

V1 CRT

R21 200K BRIGHTNESS

ALL CRT PINS HAVE SPARK GAPS BUILT INTO SOCKET

PIN 5 OF CRT SOCKET

2ND ANODE

R34 HORIZONTAL HOLD

R35

CRT FILAMENT

E1 PILOT LIGHT ASSEMBLY (ON SOME MODELS)

T4

F2

F1

SW1

115V

230V

TO AC INPUT

AC INPUT 115V / 230V 60Hz/50Hz

TO PIN 9 ON PANEL

SHIELD NOT ON ALL MODELS

Q16 REGULATOR

Q14 REG DRIVER

R79 150 10W

R69 1.2K 5W

C43A 400MF

C43B 600MF

C43C 200MF

R75 1K

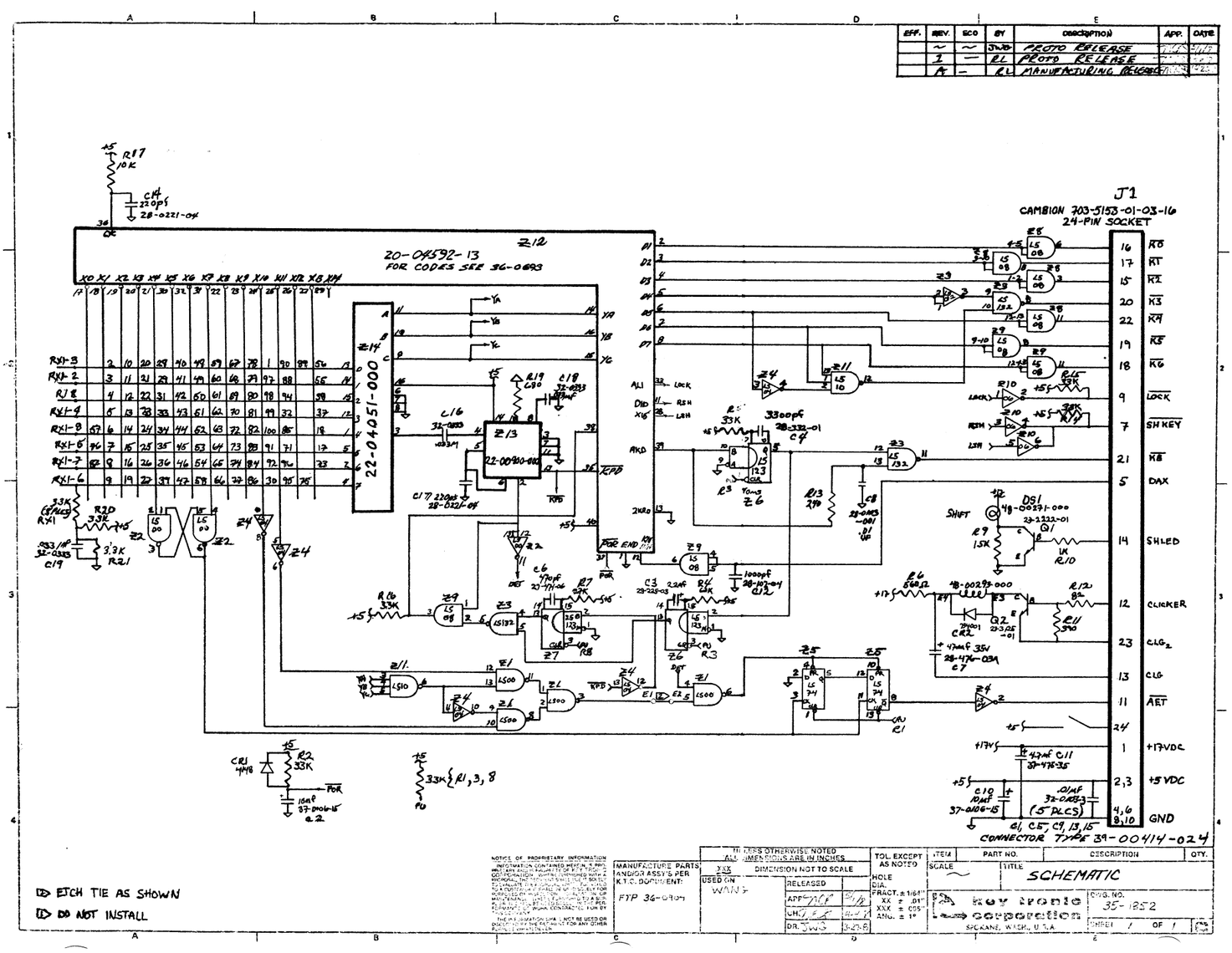
R76 3.3K

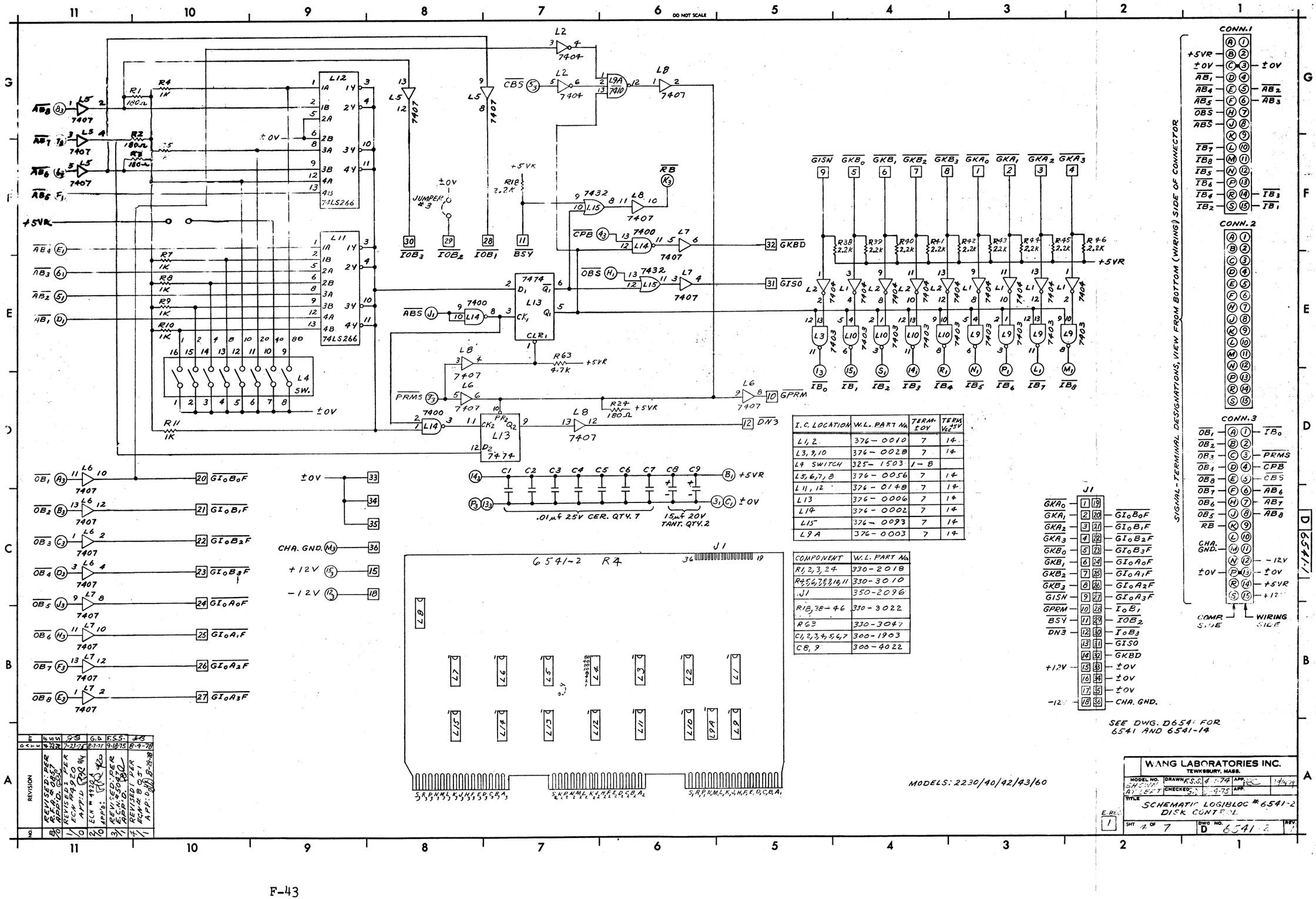
R77 100

R78 5.6K

D10 D11 D12 D9

MOTOROLA DISPLAY INTERCONNECTION DIAGRAM


J1
CAMBION 703-5153-01-03-16
24-PIN SOCKET
20-04592-13
FOR CODES SEE 36-0693
22-04051-000
CONNECTOR 77-PIN 39-00414-024
SCHEMATIC
SCALE
SIZE
DWG. NO. 35-1852
SHEET 1 OF 1
ETCH TIE AS SHOWN
DO NOT INSTALL



I.C. LOCATION	W.L. PART No.	TERM. ±0V	TERM. V_{cc} ±5V
L1, 2	376-0010	7	14
L3, 9, 10	376-0028	7	14
L4 SWITCH	325-1503	1-8	
L5, 6, 7, 8	376-0056	7	14
L11, 12	376-0148	7	14
L13	376-0006	7	14
L14	376-0002	7	14
L15	376-0093	7	14
L9A	376-0003	7	14

COMPONENT	W.L. PART No.
R1, 2, 3, 24	330-2018
R4, 5, 6, 7, 8, 9, 10, 11	330-3010
J1	350-2096
R18, 38-46	330-3022
R63	330-3047
C1, 2, 3, 4, 5, 6, 7	300-1903
C8, 9	300-4022

NO.	REVISION	BY	DATE
B	REVISED PER ECN #4920 ADDED J1	MS	7-23-74
1	REVISED PER ECN #4920 APP: D 8-2-74	MS	8-7-74
2	ECN #4920 APP'D:	RC	8-7-74
3	REVISED PER ECN #4980	MS	9-18-75
4	REVISED PER ECN #4980 APP: D 8-29-76	MS	8-9-76

WANG LABORATORIES INC.
TEWKSBURY, MASS.

MODEL NO. SHOWN ANY TEXT — DRAWN F.S.S. 4-1-74 APP. — CHECKED 4-9-75 APP. — 1/4/74

TITLE: SCHEMATIC LOGIBLOC #6541-2 DISK CONT'L.

SHT 4 OF 7 — DWG NO. D 6541-2 — REV. 4

E.REV 1

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DO NOT SCALE

CHAR. BUFF

LINE BUFF

L5 DO NOT LOAD

1702 ROM DELAY

3.345

L-RESET

B-RESET

LINE BUFF FLAG

CHAR. BUFF FLAG

ENABLE FLAG

RESET FLAG

CASE FLAG

LINE BUFF STROBE

SET-UP STROBE

LATCH CASE

CLEAR LINE BUFF

EXT. DEVICE STROBE

.9 μs

.5 μs

2 μs

RDY

BSY

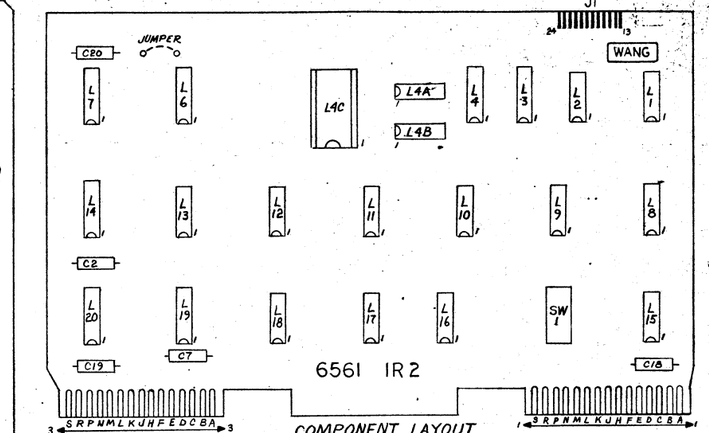
MYLAR

MICA

TYP 8

J1

13	1	RI (LSB)
14	2	R2
15	3	R2A
16	4	R5
17	5	T1
18	6	T2 (MSB)
19	7	STROBE
20	8	RB
21	9	
22	10	
CH GND	23	11	±0V
±0V	24	12	+12V



COMPONENT LAYOUT

HOLE LEGEND	HOLE DIA.	TOL.
DRILLED OR PUNCHED HOLE TOLERANCES	.0135 to .125	±.001
	.126 to .250	±.001
	.251 to .500	±.003

IDENT.	DESCRIPTION	QTY.
A.		

CONN.

A	1	
B	2	+5VR
C	3	±0V
D	4	AB1
E	5	AB4 — AB2
F	6	AB5 — AB3
H	7	OB5
J	8	AB6
K	9	
L	10	
M	11	
N	12	
P	13	
R	14	
S	15	

CONN. 2

A	1	TP1
B	2	
C	3	TP6
D	4	
E	5	
F	6	
H	7	
J	8	
K	9	TP3
L	10	
M	11	
N	12	TP8
P	13	TP3
R	14	TP2
S	15	TP4

CONN. 3

A	1	OB1
B	2	OB2
C	3	OB3 — RESET
D	4	OB4
E	5	OB8
F	6	OB7 — AB6
H	7	OB6 — AB7
J	8	OB5 — AB8
K	9	RB
L	10	
M	11	
N	12	CH. GND — -12
P	13	+20V
R	14	+5VR
S	15	+12V

SIGNAL-TERMINAL DESIGNATIONS, VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

LOCATION	W.I. PART NO.	TERM. NO. ±0V	TERM. NO. Vcc, +5VR
L4C	377-0156	—	24
L1,2	376-0128	7	14
L3,4	376-0151	12	5
L6,7	376-0119	8	16
L8,12	376-0006	7	14
L9	376-0016	7	14
L10	376-0010	7	14
L11	376-0002	7	14
L13,9A,4B	376-0055	7	14
L14,19,20	376-0104	8	16
L15,16	376-0148	7	14
L17	376-0036	7	14
L18	376-0028	7	14
L4C SKT.	376-9003	—	—

COMPONENT	W.I. PART NO.
R1, 14, 31, 33-43	330-3022
R3-8, 12, 15, 32	330-3010
R9	330-4047
R10, 16, 2022-29	330-3047
R11	330-2022
R13, 30	330-2039
R17, 19	330-4012
R18	330-4018
R21, 44-51	330-3068
C2, 18, 19, 20	300-4022
C3, 6, 8, 9	300-5004
C4	300-5006
C5, 10	300-1470
C7	300-2033
C11-17	300-1902
SW. 1 CAP	325-9047
SW. 1	325-1503
J1	350-1025

REV.	NO	ER	C.D.	E.B.A.
	12-3-74	5-14-75	5-21-75	6-26-75

REVISION

CHANGED PER DCR-339 APP'D:

REV. PER ECN-4871 APP'D:

REVISED PER ECN-5371 APP'D:

WANG PART NO.	ITEM	QTY.	NAME
FIRST USED ON / ASSY USED ON			
2201			
2202			
2212			
2232			

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL

FINISH

MODEL NO. SEE CHART

SEE ENGRG SPECIFICATIONS No.

TOL. EX. AS NOTED .XX ± .010 FRAC. ± 1/64 .XXX ± .005 ANG. ± 1°-30' FINISH √

SCALE — SHT 4 OF 8

MATERIAL	DESCRIPTION			
BY	DATE	APPROVED BY	DATE
DWN SR	10-8-74	E ENGR	11-4
CHK		M ENGR	
E. C. CONTROL		MFG ENGR	

TITLE SCHEMATIC LOGIBLOC 6561 DOUBLE BUFFERD TYPEWRITER/PLOTTER

210-6561 | D | 6561 | 4

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.

E REV. 1

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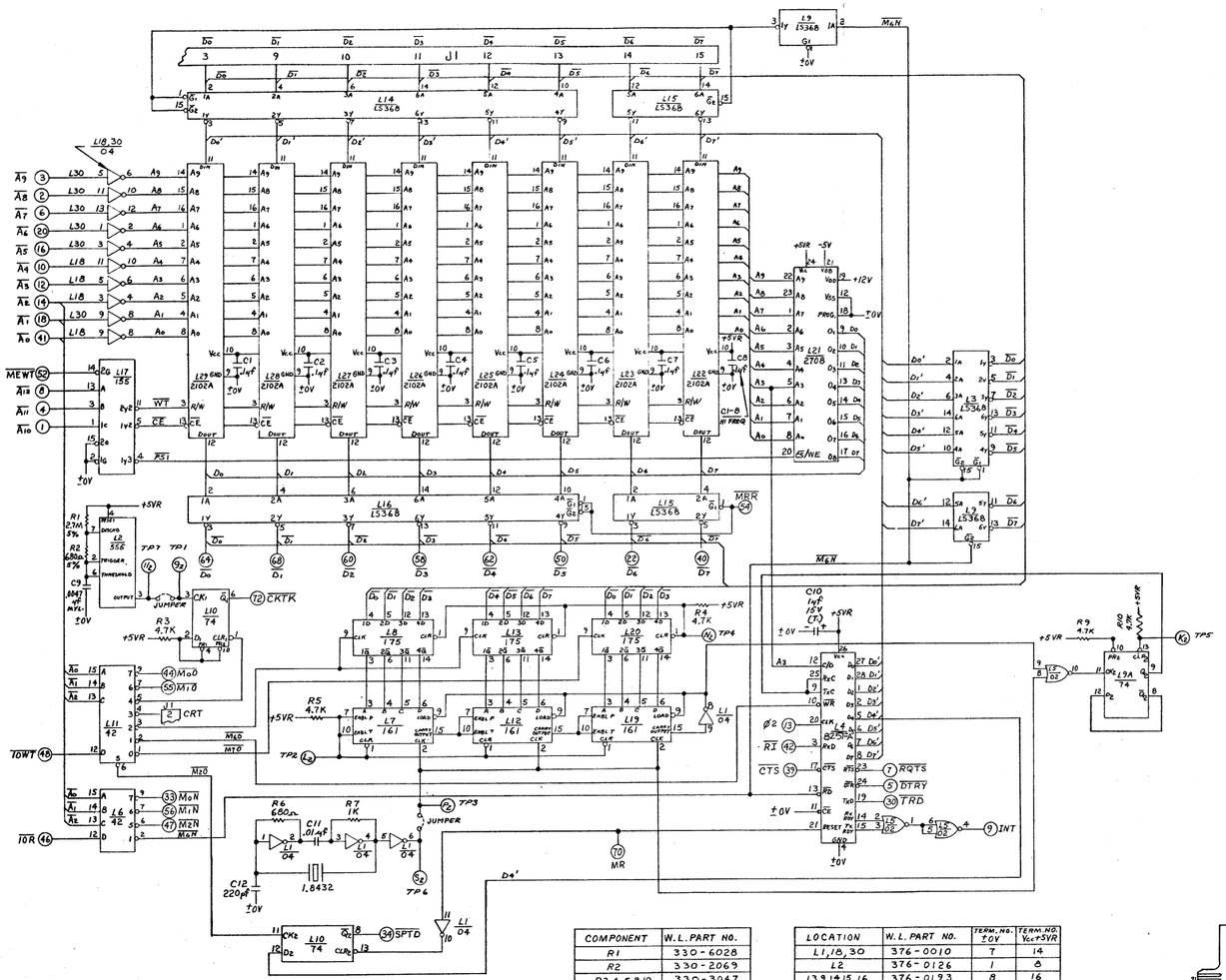
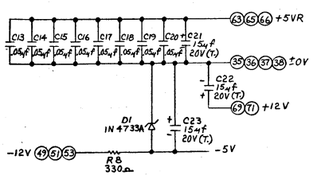
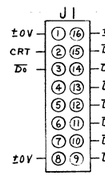
DO NOT SCALE

HOLE LEGEND	HOLE DIA.	TOL.
DRILLED OR PUNCHED HOLE TOLERANCES:	.0135 to .125	±.002
	.126 to .250	±.003
	.251 to .500	±.004
	.501 to .750	±.005

IDENT.	DESCRIPTION	QTY.
A		

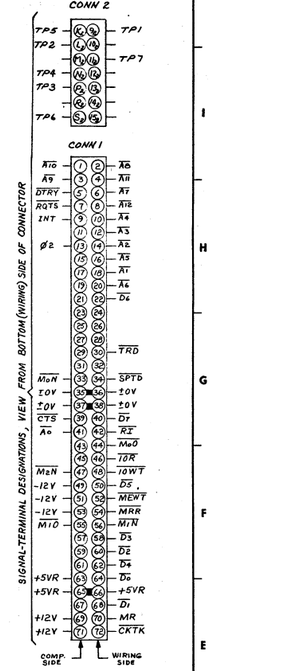




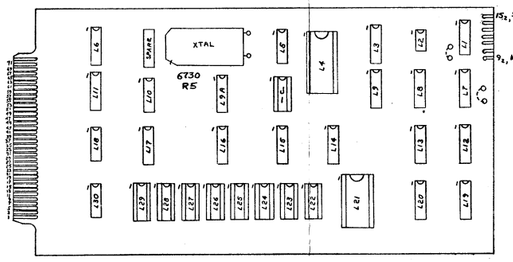


COMPONENT	W.L.PART NO.
R1	330-6028
R2	330-2069
R3,4,5,9,10	330-3047
R6	330-2068
R7	330-3010
R8	330-2033
C1-8	300-1930
C9	300-2047
C10	300-4000
C11	300-1903
C12	300-1220
C13-20	300-1900
C21,22,23	300-4022
D1	380-2052
XTAL	321-0015
J1	376-9002

LOCATION	W.L. PART NO.	TERM.NO. ±0V	TERM.NO. Vcc+5VR
L1,18,30	376-0010	7	14
L2	376-0126	1	8
L3,9,14,15,16	376-0193	8	16
L4	377-0352	4	26
L5	376-0016	7	14
L6,11	376-0008	8	16
L7,12,19	376-0094	8	16
L8,13,20	376-0119	8	16
L9A,10	376-0006	7	14
L17	376-0049	8	16
L21	378-2015R6	12	24
L22-29	377-0069	9	10
L22-29	376-9002		
L21	376-9003		
L4	376-9015		



LOCATION	TYPE	SPARES
L1	7404	1
L5	7402	1
L18	7404	2
L9A	7474	1



NOTES
1. ALL CHIPS ARE 7400 SERIES UNLESS OTHERWISE SPECIFIED.

REVISION	DRWG.	ECO
A	ORIG. PER	
B	REVISED PER	ECO #5152
C	REVISED PER	ECO #5194
D	REVISED PER	ECO #5233
E	REVISED PER	ECO #5252

E-REV 0

WANG PART NO.	ITEM	QTY.	NAME	MATERIAL	DESCRIPTION
DO NOT USE	FIRST USED ON	ASSY USED ON	WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.		
			MODEL NO. 2227B	BY / DATE / APPROVED BY / DATE	
				DWN EK 4-12-76 E ENGR	
				CHK G.D. 6-9-76 M ENGR	
				E.C. CONTROL / MFG ENGR	
			MATERIAL	TITLE A-SYNC T.C.	
			FINISH	SEE ENGRG SPECIFICATIONS	
				TOL. EX. AS NOTED .X = ±.010 FRAC. = 1/64 .XX = ±.005 ANG. = 1°30' FINISH √	
				SCALE 2/1 SHT 1 OF 1	210-6730 WANG PART NUMBER / E SIZE / 6730 DRAWING NUMBER / 9 REV.

E 6730

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DO NOT SCALE

HOLE LEGEND

DRILLED OR PUNCHED HOLE TOLERANCES:	HOLE DIA.	TOL.
	.0135 to .125	± .005
	.136 to .250	± .006
	.251 to .500	± .007

IDENT.	DESCRIPTION	QTY.
A		

LOCATION	W.L. PART NO.	TERM. NO. ±0V	TERM. NO. Vcc +5VR
L1	376-0051	7	14
L2	376-0006	7	14
L3	376-0005	11	4
L4,6	376-0081	7	14
L4A, L5	376-0002	7	14
L7,8	376-0148	7	14
L9	376-0010	7	14
L10	376-0056	7	14
L11-15	376-0189		
L9A	376-0028	7	14
L6A	376-0139	7	14

COMPONENT	W.L. PART NO.
SW 1	325-1503
J2	350-2097
J1	350-2096
R1-10,23,27-29	330-3047
R11	333-0017
* R12-22,24-26	330-1047
C1	300-5006
C2-5	300-1903
C6,7	300-4022
C8	300-1913
D1-4	380-0001
D5,6	380-1001
RLY 1,2	320-0047

CONN.1

+5VR	A 1	B 2	+5VR
±0V	C 3	D 4	±0V
$\overline{ABI}$	E 5	F 6	$\overline{AB2}$
$\overline{AB4}$	H 7	J 8	$\overline{AB3}$
$\overline{OBS}$	K 9	L 10	
$\overline{ABS}$	M 11	N 12	
$\overline{IB7}$	P 13	R 14	$\overline{IB3}$
$\overline{IB8}$	S 15	T 16	$\overline{IB1}$
$\overline{IB5}$	U 17	V 18	
$\overline{IB6}$	W 19	X 20	$\overline{IB2}$

SIGNAL - TERMINAL DESIGNATIONS, VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

CONN.3

$\overline{OBI}$	A 1	B 2	$\overline{IBS}$
$\overline{OB2}$	C 3	D 4	$\overline{PRMS}$
$\overline{OB3}$	E 5	F 6	$\overline{CPB}$
$\overline{OB4}$	H 7	J 8	$\overline{OBS}$
$\overline{OB5}$	K 9	L 10	$\overline{AB6}$
$\overline{OB6}$	M 11	N 12	$\overline{AB7}$
$\overline{OB5}$	P 13	R 14	$\overline{AB8}$
$\overline{RB}$	S 15	T 16	
±0V	U 17	V 18	±0V
+5VR	W 19	X 20	+5VR
+12V	Y 21	Z 22	+12V

COMP. SIDE — WIRING SIDE

SPARES		
TYPE	LOC.	SP
7408	L6	1
7414	L6A	2

J1 — J2

TP2 O

L6A L6 L5 L4 L3 L2 L1A L1 L10 L9A L9 L7 L8 L11 L15 L14 L13 L12 L11 RLY 2 RLY 1 S1

6786 R6

3 R P N M L K J H F E D C B A — 1 3 R P N M L K J H F E D C B A

COMPONENT LAYOUT

NOTE: * FOR 6786-1 ONLY. DELETE R12 THRU R26 AND REPLACE THEM WITH JUMPERS.

REVISION	BY	DATE	APPROVED BY	DATE
A	ECO-6786-1 ADDED	7-23-75		
B	REVISED PER ECO 11782 ADDED	8-15-75		
C	REVISED PER ECO 11818 ADDED	9-15-75		
D	REVISED PER ECO 11818 ADDED	10-15-75		
E	REVISED PER ECO 11818 ADDED	10-15-75		
F	REVISED PER ECO 11818 ADDED	11-5-75		
G	REVISED PER ECO 11818 ADDED	11-19-75		
H	REVISED PER ECO 11818 ADDED	12-19-75		
J	REVISED PER ECO 11818 ADDED	1-9-76		
K	REVISED PER ECO 11818 ADDED	1-29-76		
L	REVISED PER ECO 11818 ADDED	2-23-76		
M	REVISED PER ECO 11818 ADDED	3-19-76		
N	REVISED PER ECO 11818 ADDED	4-9-76		

WANG PART NO.	ITEM	QTY.	NAME	MATERIAL	DESCRIPTION
FIRST USED ON	ASSY USED ON		WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.	BY	DATE / APPROVED BY / DATE
			MODEL NO. 2230 MXB	DWN CR 1-23-75 / ENGR	
			SEE ENGG SPECIFICATIONS No.	CHK C.D. 2-6-75 / M ENGR	
				I. C. CONTROL	MFG ENGR
			FINISH	TOL. EX. AS NOTED XX ± .010 FRAC. ± 1/64 XXX ± .005 ANG. ± 1/30'	TITLE DAISY CHAIN MUX SLAVE
				SCALE — SHT. 1 OF 1	210-6786 / E / 6786 / 12
					WANG PART NUMBER / SIZE / DRAWING NUMBER / REV.

6786-1 E-REV 4 — 6786 E-REV 2

E 6786

PRELIMINARY

COMPONENT LAYOUT
VARIATION CHART SECTION 2

MODEL	210	209	L18	L19	L20
2200	7042-1-M	7042-1	378-0611	378-0612	
2200 CHINESE	7042-1-N	7042-1	378-0613	378-0614	
2200 GERMAN	7042-1-P	7042-1	378-0615	378-0616	

VARIATION CHART SECTION

MODEL	210	209	L18	L19	L20
2200	7042-1	7042-1	378-0370	378-1371	377-0240
2200 CHINESE	7042-1-M	7042-1	378-0611	378-0612	
2200 GERMAN	7042-1-N	7042-1	378-0613	378-0614	
2200 FRENCH	7042-1-P	7042-1	378-0615	378-0616	

NOTE: FOR 209-7042, DELETE R67, SOCKET L18, L19, JUMPER #2
FOR 209-7042-1, DELETE L18, L19, R67, SOCKET L20, JUMPERS #1 & #2

LOCATION	W.L. PART NO.	TERM. NO. +0V	TERM. NO. +5VR
L1	376-0158	8	16
L2, 5I	376-0010	7	14
L3, 6, 7, 9	376-0069	7	14
L5	376-0047	8	16
L8, 29, 37	376-0055	7	14
L7	377-0000	—	5
L8, 9	376-0011	10	5
L10, 11	376-0119	8	16
L12, 13, 14, 15	376-0176	8	16
L16, 23, 35	376-0104	8	16
L18, 19	SEE CHART	7	14
L20	SEE CHART	14	24
L21, 46	376-0081	7	14
L22, 24, 31	376-0056	7	14
L25, 27	376-0093	7	14
L26, 28	376-0060	7	14
L29, 35, 44, 45	376-0056	7	14
L30, 34	376-0016	7	14
L33	376-0113	16	5
L38	376-0065	10	5
L39, 47	376-0069	7	14
L40, 42	376-0093	7	14
L41	376-0056	7	14
L43	376-0093	7	14
L48	376-0069	7	14

COMPONENT	W.L. PART NO.
R1-11, 13, 15-24, 32-34, 62, 63, 65-73	336-3322
R12, 25, 33	336-4733
R14	330-4733
R26-31, 36, 38-61, 64	330-2733
C28, 29	300-1507
C1	300-4002
C4, 7	300-1027
C11, 16, 17	300-5005
C2, 12, 25, 26	300-5006
C3	300-1033
C5, 6	300-4010
C8, 10	300-5004
C9, 21-23, 27	306-4005
C14	375-1914
C18-20	375-1904
C12	340-1038
J1	376-9003
C15	375-1902
J2	376-9007
C24	300-4017

* SEE CHART

NAME	DATE
DWN	2-10-77
CHK S.D.	7/26/76
E.C. CONTROL	
MFG ENGR	
M ENGR	
APPROVED BY	

MATERIAL
FINISH
TOL. EX. AS NOTED
XX ± .03 ANG. ± 1°
XXX ± .005 ANG. ± 1/2°
SCALE NON SHT 1 OF 1

WANG LABORATORIES, INC. Tewksbury, Mass. U.S.A.

MODEL NO 2200
SEE ENGR'G SPECIFICATIONS

TITLE
KEYBOARD/PRINTER/FLOPPY CONNECTOR

SERIAL INTERFACE JUMPER CHART

SIZE E | DRAWING NUMBER 7042

WANG PART NUMBER

REV

7042 E-REV 3

7042-1 E-REV 3

SIGNAL-TERMINAL DESIGNATIONS VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

COMP SIDE | WIRING SIDE

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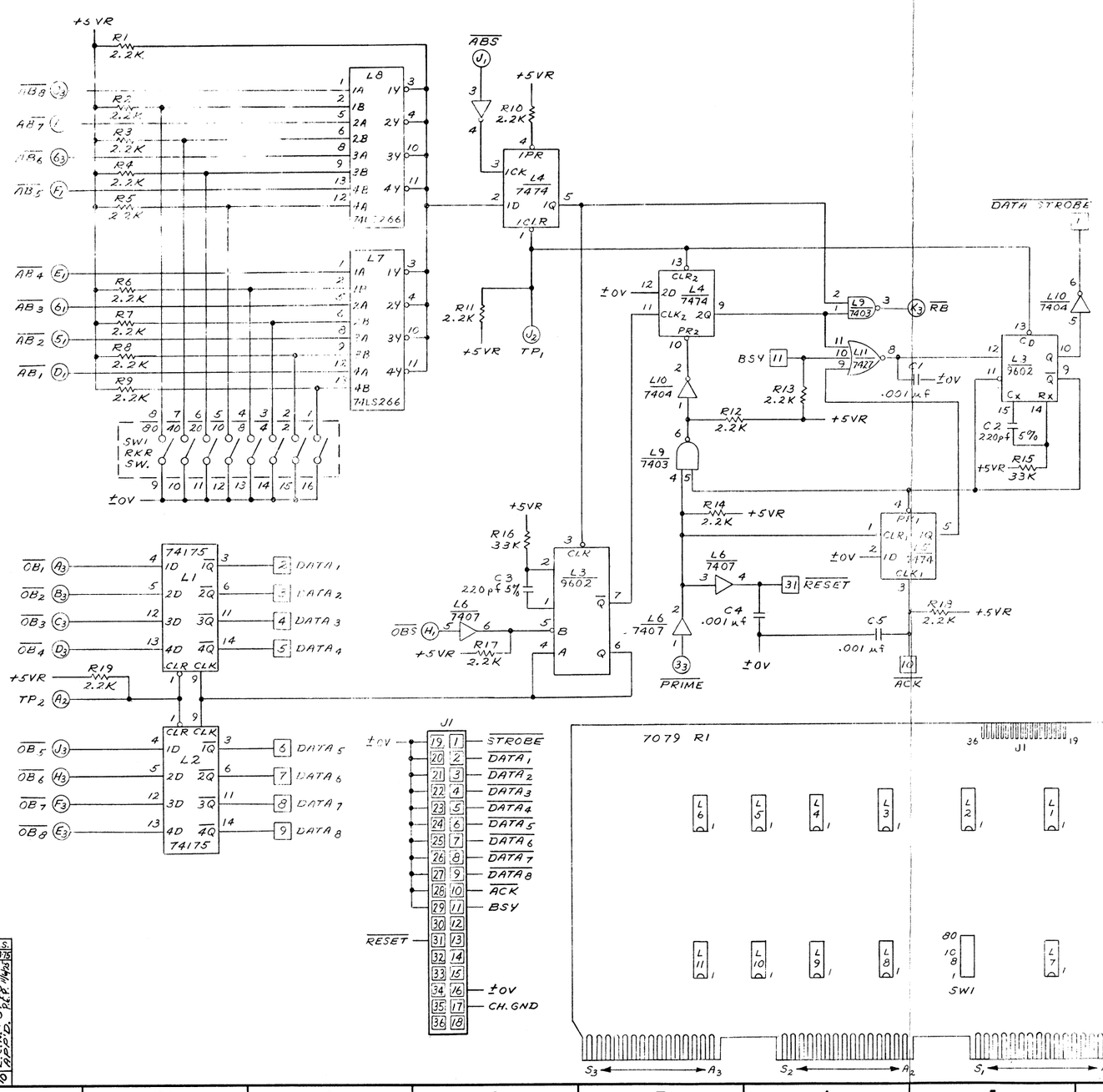
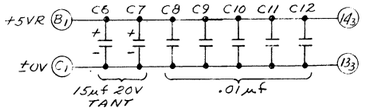




I.C. LOCATION	W.L. NO.	TERM. FOR ±0V	TERM. FOR VCC +5VR
L1, 2	376-0119	8	16
L3	376-0104	8	16
L4,5	376-0006	7	14
L6	376-0056	7	14
L7,8	376-0148	7	14
L9	376-0028	7	14
L10	376-0010	7	14
L11	376-0125	7	14

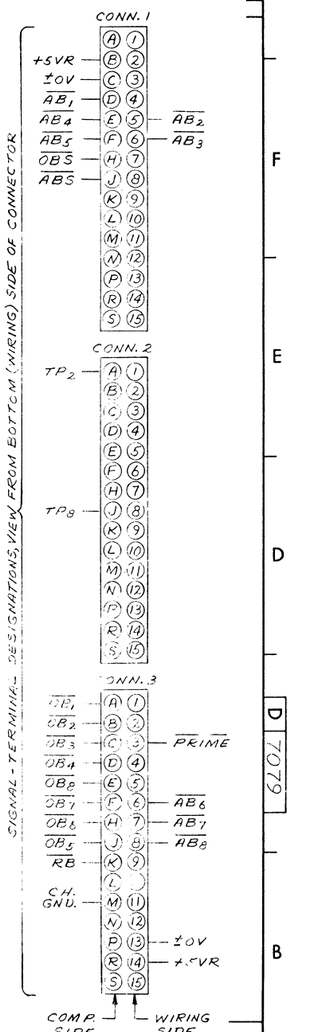
COMPONENT	W.L.NO.
R1-14, 17-19	330-1038
R15, 16	330-4033
C1,4,5	300-1906
C2,3	300-5004
C6,7	300-4022
C8-12	300-1903
SW1	325-1503
SW1-CAP	325-9047
J1 CONN.	350-1038

I.C. TYPE	LOCATION	SPARES
7407	L6	3
7403	L9	2
7404	L10	2
7427	L11	2

HOLE LEGEND

	HOLE DIA	TOL
DRILLED OR PUNCHED HOLE TOLERANCES	0135 to 125	+.003 −.001
	126 to 250	+.004 −.001
	251 to 500	+.005 −.001

IDENT	DESCRIPTION	QTY
A		



NO	REVISION	BY	DATE
0	ORIGINATED PER ECO # E0	F.S.S.	10-1-75
1	REVISED PER E.C.N. # 51 APPD. P.E.P.	F.S.S.	10-23-75

E-REV 0

WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION

Qty. Per Unit	FIRST USED ON	ASSY USED ON

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL

FINISH

MODEL NO. 2221-W

SEE ENGRG SPECIFICATIONS No.

TOL EX AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG. ± 1°30' FINISH 125

SCALE SHT OF

BY	DATE	APPROVED BY	DATE
DWN F.S.S.	10-1-75	E ENGR P.E.P.	11/6/75
CHK G.D.	11/6/75	M ENGR	
E.C. CONTROL		MFG ENGR	

TITLE SCHEMATIC LOGIBLOC MATRIX PRINTER CONTROLLER

210-7079 | D | 7079 | 1

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

7079

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DO NOT SCALE

LOCATION	W.L. PART NO.	TERM. NO. ±0V	TERM. NO. Vcc +5VR
L1,8,12,22,23	376-0006	7	14
L1A,10,17	376-0093	7	14
L2	376-0016	7	14
L3,4	376-0056	7	14
L5,26,27	376-0080	8	16
L6,7	376-0119	8	16
L9	376-0055	7	14
L11,16,19	376-0081	7	14
L13,28	376-0010	7	14
L14,15	376-0204	8	16
L18	376-0128	7	14
L20	376-0002	7	14
L21	376-0003	7	14
L23,24	376-0148	7	14
L29,30	376-0008	8	16
L31,32	376-0160	8	16
L33	376-0194	7	14

LOCATION	TYPE	SPARES
L1A	7432	1
L2	74OE	1

COMPONENT	W.L. PART NO.
R1-8,9,10,15,20,23, 26,27, 34,36	330-3010
R11	330-4019
R12,13,14,16,25,30, 33,36,38,39,43	330-2022
R14,17,19,24,29,32, 35,40,41,44,45	330-2033
R21	330-4013
R22	330-3069
R31	330-4040
R37	330-4034
R42	330-4023
C1-6	300-5005
C7-18	300-1900
C19,20	300-4022
SW. 1	325-1503
J1,J2	350-2097
CONN. 4	350-0022

HOLE LEGEND

DRILLED OR PUNCHED HOLE TOLERANCES:	HOLE DIA.	TOL.
	.0125 to .125	±.002
	.126 to .250	±.003
	.251 to .500	±.005

IDENT.	DESCRIPTION	QTY.
A		

CONN. 1

+5VR	A1 B2	+5VR
±0V	C3	±0V
DB7	D4	
DB4	E5	DB2
DB5	F6	DB3
DB5	G7	
DB7	J8	
DB6	K9	
DB4	L10	
DB2	M11	
DB0	N12	
DB1	P13	
DB3	R14	DB3
DB2	S15	DB1

CONN. 2

TP1	A1 B2	TP11
TP2	C3	TP12
	D4	TP13
	E5	TP14
	F6	TP15
TP4	H7	
TP5	J8	
TP6	K9	
TP7	L10	
TP8	M11	
TP9	N12	
TP3	P13	
TP10	R14	
	S15	

CONN. 3

DB1	A1 B2	IBS
DB2	C3	IB9
DB3	D4	PRMS
DB4	E5	CBS
DB5	F6	RB6
DB6	H7	RB7
DB7	J8	RB8
R/B	K9	
	L10	
GND	M11	
-12V	N12	-12V
±0V	P13	±0V
+5VR	R14	+5VR
+12V	S15	+12V

CONN. 4

RD8	A1 B2	RD1
RD7	C3	RD3
RD4	D4	RD5
RD6	E5	RD7
DO1	F6	DO6
DO7	H7	DO8
WE	J8	DO4
DO3	K9	DO2
DO5	L10	RDL
T1	M11	T2
CTADD	N12	DI8
DI7	P13	DI4
DI5	R14	DI1
COMPARE	S15	DIEN
ME	T16	CLR
DI2	U17	DI6
DI3	V18	DI0B
	W19	
-12V	X20	-12V
±0V	Y21	±0V
+5VR	Z22	+5VR
+12V		+12V

COMP. SIDE — WIRING SIDE

SIGNAL-TERMINAL DESIGNATIONS, VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

COMPONENT LAYOUT

REVISION	BY	DATE	APPROVED BY	DATE
A ORIGINATED PER DWG # 210-7141	ER	4-28-77		
B REVISED PER ECO # 1	ER	5-26-77		
C REVISED PER ECO # 2	ER	6-21-77		
D REVISED PER ECO # 3	ER	7-15-77		
E REVISED PER ECO # 4	ER	7-20-77		

WANG PART NO.	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
ON "M" PART USED ON	ASSY USED ON				

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL

MODEL NO. 2209A

SEE ENGRG SPECIFICATIONS No.

FINISH

TOL. EX. AS NOTED .XX ± .010 FRAC. ± 1/64 ANG. ± .005 AND ± 1° 30' FINISH √

BY	DATE	APPROVED BY	DATE
DWN ER	4-28-77	E ENGR	7-20-77
CHK		M ENGR	
E.C. CONTROL		MFG ENGR	

TITLE 1600 BPI 9 TRACK TAPE DRIVE CONTROLLER MB

SCALE	SHT 1 OF 1	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
		210-7141	E	7141	5

E-REV 4

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DO NOT SCALE

LOCATION	TYPE	SPARES
L20	7408	2
L21	7404	1
L23	7402	2
L25	7404	3
L31	7474	1
L33	7400	2
L35	7432	2

COMPONENT	W.L. PART NO.
C1	300-1903
C2,44	300-4000
C3	300-4002
C4-11	300-1930
C12-19	300-1931
C20,43	300-1270
C21-41	300-1900
R1,2	330-2047
R3-7,26,35	330-3010
R8,9	330-1011
R10-17	330-2022
R18-25	330-2033
R27-34	330-3022
C42-44	300-4022
Q1	374-0002
Q2	375-1050
J1	376-9002
XTAL	321-0008

LOCATION	W.L. PART NO.	TERM. NO ±0V	TERM. NO. V_{CC}+5VR
L1,2	376-0119	8	16
L3-10	377-0314	18	
L11,27	376-0098	8	16
L12,13	376-0204	8	16
L19,15	376-0160	8	16
L16,34	376-0082	8	16
L17,18,19	376-0087	8	16
L20	376-0081	7	14
L21,25	376-0010	7	14
L22,24	376-0011	10	5
L23	376-0016	7	14
L26,28,29,32	376-0053	8	16
L30	376-0097	8	16
L31	376-0006	7	14
L33	376-0002	7	14
L35	376-0093	7	14
L36	376-0178	7	14
L3-10	376-9014		

HOLE LEGEND

	HOLE DIA.	TOL.
DRILLED OR PUNCHED HOLE TOLERANCES	.0135 to .125	±.003 ±.005
	.126 to .250	±.004 ±.005
	.251 to .500	±.005 ±.005

IDENT.	DESCRIPTION	QTY.
A		

SIGNAL-TERMINAL DESIGNATIONS VIEW FROM BOTTOM (WIRING) SIDE OF CONN.

$\overline{RD0}$	A 1	2	$\overline{RD1}$
$\overline{RD2}$	B 2	3	$\overline{RD3}$
$\overline{RD4}$	C 3	4	$\overline{RD7}$
$\overline{RD4}$	D 4	5	D06
D01	E 5	6	D08
D07	F 6	7	D09
WE	H 7	8	D02
D03	J 8	9	D02
D05	K 9	10	ROL
T1	L 10	11	T2
$\overline{CY}$ RDO	M 11	12	$\overline{DI0}$
$\overline{DI1}$	N 12	13	$\overline{DI4}$
$\overline{DI5}$	P 13	14	$\overline{DI}$
COMP. PARE	R 14	15	DI EN
ME	S 15	16	CLR
$\overline{DI2}$	T 16	17	$\overline{DI6}$
$\overline{DI3}$	U 17	18	$\overline{DI0B}$
-12V	W 19	19	-12V
±0V	X 20	20	±0V
+5VR	Y 21	21	+5VR
+12V	Z 22	22	+12V

COMPONENT LAYOUT

REVISION	BY	DATE
ORIGINATED PER ECN # 6594	AR	5-27-77
ADD D-DEL (1mH) ECN # 6594	AR	7-11-77

E-REV 0

WANG PART NO.	ITEM	QTY	NAME
PC. No.	FIRST USED ON	ASSY USED ON	

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MODEL NO. 2209A

SEE ENGRG SPECIFICATIONS No.

FINISH

TOL. EX. AS NOTED XX = .010 FRAC. ± 1/64 .XXX = .005 ANG. ± 1° 16 FINISH

SCALE: 4/1 SHT 4 OF 5

MATERIAL	DESCRIPTION
BY	DATE
DWN AR	5-27-77
CHK	
E C CONTROL	
MFG ENGR	
TITLE	1600 BPI 9 TRACK TAPE MEMORY DAUGHTER BOARD
210-7142	E 7142 1
WANG PART NUMBER	SIZE DRAWING NUMBER REV

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DO NOT SCALE

I.C. LOCATION

I.C. LOCATION	W.L. NO.	TERM. FOR ±0V	TERM. FOR VCC +5VR
L18, 21	376-0081	7	14
L1, 28	376-0010	7	14
L2	376-0059	7	14
L3, 4	376-0077	8	16
L5, 15	376-0076	4	
L6	SEE CHART	12	24
L7	377-0269	2	20
L8, 17, 18, 26, 27, 29	376-0193	8	16
L9, 12, 19, 22	376-0062	7	14
L10, 13, 25	376-0180	7	14
L11	376-0073	10	5
L13, 23	376-0003	7	14
L16	376-0178	7	14
L16A, 36, 39	376-0006	7	14
L20, 38	376-0016	7	14
L24	376-0192	8	16
L30	376-0108	8	16
L31	376-0158	8	16
L32, 33	376-0148	7	14
L34, 35, 41, 42	376-0183	8	16
L37	376-0093	7	14
L40	376-0104	8	16
L43	376-0098	8	16
L6 SKT.	376-9003		
L7 SKT.	376-9011		

TYPE	I.C. LOCATION	SPARES
7408	L1A	2
7400	L9	1

COMPONENT	W.L. NO.
R1	330-3010
R2-16, 18, 27, 30, 31, 33-41, 43, 46	330-4010
R17, 22	330-2018
R19, 24, 32, 42, 45	330-3047
R20, 21	330-2022
R23	330-3018
R25, 26	330-1010
R28	331-2012
R29	330-4012
R44	330-3082
R47	330-4015

COMPONENT	W.L. NO.
C1	300-1082
C2	300-1913
C3, 7-19	300-1900
C4, 6, 20-22	300-4022
C5	300-1903
Q1, 2	375-1050
Q1, 2 TRAN. PAD. (SM)	375-9004
D1	350-2052
XTAL	321-0008
SW1	325-1503
SW1 CAP	325-9047
CONN. J1	350-0029 M

VARIATION CHART			
210 = 209 + 377 or 378			
MODEL	209	210	LL
2228B	7223	7223-A	378-2060-10
2228C	7223	7223 C	378-9001

HOLE LEGEND		
DRILLED OR PUNCHED HOLE TOLERANCES:	HOLE DIA.	TOL.
	.0135 to .125	+.002 −.000
	.126 to .350	+.003 −.000
	.351 to .500	+.003 −.000

IDENT.	DESCRIPTION	QTY.
A		

REVISION	DESIGNATED PER	DWN	CHK	APP	DATE
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B	REVISED PER ECN 9555A				
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XN	REVISED PER ECN 10093				
XP	REVISED PER ECN 10094				
XQ	REVISED PER ECN 10095				
XR	REVISED PER ECN 10096				
XS	REVISED PER ECN 10097				
XT	REVISED PER ECN 10098				
XU	REVISED PER ECN 10099				
XV	REVISED PER ECN 10100				
XW	REVISED PER ECN 10101				
XX	REVISED PER ECN 10102				
XY	REVISED PER ECN 10103				
XZ	REVISED PER ECN 10104				
YA	REVISED PER ECN 10105				
YB	REVISED PER ECN 10106				
YC	REVISED PER ECN 10107				
YD	REVISED PER ECN 10108				
YE	REVISED PER ECN 10109				
YF	REVISED PER ECN 10110				
YG	REVISED PER ECN 10111				
YH	REVISED PER ECN 10112				
YJ	REVISED PER ECN 10113				
YK	REVISED PER ECN 10114				
YL	REVISED PER ECN 10115				
YM	REVISED PER ECN 10116				
YN	REVISED PER ECN 10117				
YP	REVISED PER ECN 10118				
YQ	REVISED PER ECN 10119				
YR	REVISED PER ECN 10120				
YS	REVISED PER ECN 10121				
YT	REVISED PER ECN 10122				
YU	REVISED PER ECN 10123				
YV	REVISED PER ECN 10124				
YW	REVISED PER ECN 10125				
YX	REVISED PER ECN 10126				
YY	REVISED PER ECN 10127				
YZ	REVISED PER ECN 10128				
ZA	REVISED PER ECN 10129				
ZB	REVISED PER ECN 10130				
ZC	REVISED PER ECN 10131				
ZD	REVISED PER ECN 10132				
ZE	REVISED PER ECN 10133				
ZF	REVISED PER ECN 10134				
ZG	REVISED PER ECN 10135				
ZH	REVISED PER ECN 10136				
ZJ	REVISED PER ECN 10137				
ZK	REVISED PER ECN 10138				
ZL	REVISED PER ECN 10139				
ZM	REVISED PER ECN 10140				
ZN	REVISED PER ECN 10141				
ZP	REVISED PER ECN 10142				
ZQ	REVISED PER ECN 10143				
ZR	REVISED PER ECN 10144				
ZS	REVISED PER ECN 10145				
ZT	REVISED PER ECN 10146				
ZU	REVISED PER ECN 10147				
ZV	REVISED PER ECN 10148				
ZW	REVISED PER ECN 10149				
ZX	REVISED PER ECN 10150				
ZY	REVISED PER ECN 10151				
ZZ	REVISED PER ECN 10152				

E-REV. 3

WANG PART NO.	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
FIRST USED ON	ASSY USED ON		WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		
			MODEL NO. 2228B	BY: DWN F.S.S	DATE: 11-17-76
			SEE ENGRG SPECIFICATIONS	CHK: G.D.	APPROVED BY: E ENGR: 5-31-77
				E.C. CONTROL	MFG ENGR
			TITLE: BI-SYNC B-VERSION MOTHERBOARD		
			FINISH	SCALE	SHT / OF /
			TOL. EX. AS NOTED .XX ± .010 FRAC. ± 1/64 .XXX ± .005 ANG. ± 1°30'	210-7223	E 7223 8
				WANG PART NUMBER	SIZE DRAWING NUMBER REV.

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DO NOT SCALE

HOLE LEGEND

DRILLED OR PUNCHED HOLE TOLERANCES	HOLE DIA.	TOL.
	.0135 to .125	±.002
	.126 to .250	±.003
	.251 to .500	±.004

SIGNIT	DESCRIPTION	QTY.
A		

SIGNAL-TERMINAL DESIGNATIONS, VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

COMP SIDE			WIRING SIDE
	COMN		
A10	1	2	A8
A9	3	4	A11
DTRY	5	6	A7
RQTS	7	8	A12
INT	9	10	A4
	11	12	A5
Ø2	13	14	A2
	15	16	A3
	17	18	A1
	19	20	A6
	21	22	D4
MIO	23	24	RFEB
RDY	25	26	RECK
A13	27	28	TXCR
WO	29	30	TRO
MEN	31	32	CE
	33	34	SPTD
+5V	35	36	+5V
+5V	37	38	+5V
	39	40	D7
	41	42	R1
TP1	43	44	M60
TP2	45	46	TOR
MIN	47	48	IOWT
-12V	49	50	D1
-12V	51	52	MEWT
MIO	53	54	MRR
	55	56	MIN
TP4	57	58	D3
+5V	59	60	D5
+5V	61	62	D6
MEMR	63	64	D0
+12V	65	66	MR
+12V	67	68	CKTK

J1

D1	9	8	+5V
D2	10	7	TP1
D3	11	6	TP6
D4	12	5	
D5	13	4	D0
D6	14	3	CRT
D7	15	2	+5V
+5V	16	1	+5V

COMPONENT	W.L. PART NO.
R1,2,13-17	330-4010
R3,4,19-24	330-3022
R8	330-6028
R9	330-2069
R10	330-2068
R11,5	330-3010
C1-8,21	300-1930
C9-12,14-17	300-1931
C13,18	300-4017
C22	300-2047
C23	300-1903
C24	300-1220
C25-34,19	300-1900
C35,20	300-4022
C36	300-4020
R18	331-2033
XTAL	321-0015
Q1,2	375-1050
DI	380-2052
J1	376-9005
R6,7	330-1011

LOCATION	TYPE	SPARES
L2	7408	1
L11	74LS368	2
L21	7404	1

LOCATION	W.L. PART NO.	TERM.NO. 10V	TERM.NO. Vcc+5VR
L1	376-0093	7	14
L2	376-0081	7	14
L3,30,42	376-0082	8	16
L4,5	376-0094	8	16
L6,43	376-0005	11	4
L7	376-0006	7	14
L8	376-0126	1	8
L9,18	376-0002	7	14
L10	376-0049	8	16
L11,12,13,16,17	376-0193	8	16
L14,15	376-0119	8	16
L18A,21	376-0010	7	14
L19,20	376-0008	8	16
L22-29,34-41	377-0314	18	
L32	377-0352	4	26
L33	376-0178	7	14
L22-29,34-41	376-9014		
L31	376-0011	10	5
L32	376-9015		

1. ALL I.C. CHIPS ARE 7400 SERIES. UNLESS OTHERWISE SPECIFIED.

NOTES

REVISION	BY	DATE	APPROVED
ORIGINATED PER DWR E.C.O. #1340	DWR	11-1-74	
REVISED PER RPA #1395	RPA	12-11-74	
REVISED PER RPA #1340	RPA	12-11-74	
REVISED PER ECN #1340	RPA	12-11-74	
REVISED PER ECN #1714	RPA	3-10-75	
REVISED PER ECN #1728	RPA	3-10-75	
REVISED PER ECN #1904	RPA	3-31-75	

WANG PART NO.	ITEM	QTY.	NAME	MATERIAL	DESCRIPTION
			WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.		
MATERIAL			MODEL NO. 2228B		
			SEE ENGRG SPECIFICATIONS No.		
FINISH			TOL. XX AS NOTED .XX ± .010 FRAC. ± 1/64 .XXX ± .005 ANG. ± 1°-30'		
			SCALE NONE SHT 1 OF 1		

BY	DATE	APPROVED BY	DATE
DWN DR	5/4/76	E ENGR RAC	10/4/76
CHK G. D.	6-4-76	IM. ENGR	
E. C. CONTROL		MFG ENGR	

TITLE SCHEMATIC LOGIBLOC TRANSMITTER/RECEIVER MEMORY BOARD

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
210-7224-	E	7224	5

E-REV 2

E 7224

COMPONENT LAYOUT

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DO NOT SCALE

HOLE LEGEND

	HOLE DIA.	TOL.
• DRILLED ON	.0135 to .125	± .001
"PUNCHING" = HOLE	.126 to .350	± .002
TOLERANCES:	.351 to .500	± .003

IDENT	DESCRIPTION	QTY.
A	-	-

J1

SIP-1 SIP-2 SIP-3 SIP-4 SIP-5

J2

CONN.1 CONN.2 CONN.3

SIGNAL-TERMINAL DESIGNATIONS, VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

NOTE: I CUT TRACK AS SHOWN AND ADD JUMPERS FOR 2260C ONLY.

7287 R3

COMPONENT LAYOUT

LOCATION	W. L. PART NO.
R1-11,R13,21,22,23,30	330-3047
R20,24	330-4047
R13	330-2022
R15	330-4011
R16,17,25	330-4023
R23	330-4028
R14,26,31	333-2047
R12	330-2033
C14,20,21,22	333-1903
C10,16	300-5005
C13,19	300-1904
C11,12,18	300-5006
C4-9,23-27	300-1900
C17	300-1901
J1	350-2094
J2	350-2097
SW1	325-1503
C15	300-1902
SIP4-6	333-0807
C2,3	300-4022
SIP1-3	333-0808
C1	300-1904

LOCATION	W.L. PART NO.	TERM. NO. -10V	TERM. NO. Vcc=5VR
L1,16	376-0139	7	14
L2,26	376-0010	7	14
L3	376-0048	8	16
L4,8,9,30,31,34,35	376-0182	8	16
L5	376-0049	8	16
L6,7	376-0137	7	14
L10,36,15A	376-0056	7	14
L11,18,21	376-0066	7	14
L12	376-0003	7	14
L13	376-0125	7	14
L14,15,32	376-0124	8	16
L19,23	376-0005	11	4
L20,25,12A	376-0002	7	14
L22,24,33	376-0081	7	14
L27	376-0080	8	16
L28,29	376-0148	7	14
L17	376-0028	7	14

LOCATION	TYPE	SPARES
L1	7414	3
L2	7404	1
L16	7414	1
L9	8797	4
L13	7437	2
L15A	7407	2
L22	7408	3
L24	7408	1
L32	9602	1

REVISION	BY	DATE	APPROVED
A	ORIGINATED PER DWR E 8181	5-29-78	5-29-78
B	REVISED PER ECN M 8237	5-29-78	5-29-78
C	REVISED PER ECN M 8435 APP'D 7-18-78	7-18-78	7-18-78
D	REVISED PER ECN M 8435 APP'D 7-28-78	7-28-78	7-28-78
E	REVISED PER ECN M 8435 APP'D 8-4-78	8-4-78	8-4-78
F	REVISED PER ECN M 8435 APP'D 10-16-78	10-16-78	10-16-78
G	REVISED PER ECN M 8435 APP'D 11-19-79	11-19-79	11-19-79
H	REVISED PER ECN M 8435 APP'D 11-24-79	11-24-79	11-24-79
J	REVISED PER ECN M 8435 APP'D 12-12-79	12-12-79	12-12-79
K	REVISED PER ECN M 8435 APP'D 12-19-79	12-19-79	12-19-79
L	REVISED PER ECN M 8435 APP'D 1-30-80	1-30-80	1-30-80

WANG PART NO.	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
FIRST USED ON	ASSY USED ON			BY	DATE / APPROVED BY / DATE

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

DWN [illegible] CHK E C CONTROL MFG ENGR E ENGR [illegible] 11-22-77

MATERIAL — MODEL NO. 9016A — SEE ENGRG SPECIFICATIONS No. —

FINISH — TOL. EX. AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG. ± 1°30' FINISH

TITLE MASTER DISK MUX

210-7287 | E | 7287 | 11

SCALE — | SHT 1 OF 1 | WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.

E 7287

7287 E. REV. 7

7287-1 E-REV 7

7287-2 E-REV 7

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DO NOT SCALE

NOTE JUMPER FOR 7290 IS 6
JUMPER FOR 7290-1 IS 5

COMPONENT	W.L. PART NO.
R1,2,3	330-4010
R4-9,11,13,14,16, 18,20,21,22,24,26	330-3047
R10,17,19,25	332-1068
R12,15,23	330-4033
C1,2,5,7	300-4022
C3,4,6	300-5005
C8-21	330-1900
SW.1	325-1501
SW. 2,3,4	325-1503
J5	350-0029M
J6	376-9016
J6	376-9017
J1-4	350-1051
L22-25	376-9015
Q1,3,5,7	375-1012
Q2,4,6,8	375-1014

LOCATION	W.L. PART NO.	TERM. NO. +5V	TERM. NO. GND
L1,33	376-0104	8	16
L2,18,17	-0094	8	16
L3,5,16	-0077	8	
L4	-0193	8	16
L6-9,12-15	-0076	4	8
L17, 26	-0008	8	16
L20	-0010	7	14
L21	376-0211	7	14
L22-25	377-0352	4	26
L27,30,33,42	376-0119	8	16
L28,36,40,47	-0192	8	16
L29,37,38,41,50	-0183	8	16
L31	-0222	8	16
L32	-0056	7	14
L34	-0092	8	16
L35	-0160	8	16
L43	-0093	7	14
L44	-0002	7	14
L45,46	-0006	7	14
L48	-0120	8	16
L49	376-0225	7	14

LOCATION	TYPE	SPARES
L1	9602	1
L4	74LS368	2
L20	7404	3
L21	74LS32	2
L36	74LS367	2
L32	7407	2
L34	7425	1
L44	7400	1

HOLE LEGEND

DRILLED OR PUNCHED HOLE TOLERANCES:	HOLE DIA.	TOL.
	.0135 to .125	±.003
	.126 to .250	±.004
	.251 to .500	±.005

IDENT.	DESCRIPTION	QTY.
A		

SIGNAL-TERMINAL DESIGNATIONS VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

COMPONENT LAYOUT

E 7290

WANG PART NO.	ITEM	QTY	NAME	MATERIAL	DESCRIPTION

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN		4-17-71	E ENGR	
CHK		4.21.71	M ENGR	
E. C. CONTROL			MFG ENGR	

MATERIAL — MODEL NO - A1 X C / 2236 - A1 X D — SEE ENGRG SPECIFICATIONS No.

FINISH — TOL. EX. AS NOTED .XX ± .010 .XXX ± .005 ANG. ± 1/2° FINISH

TITLE: 8080 INTERACTIVE TERMINAL

210-7290 | E | 7290 | 9

SCALE: 1/1 | SHT 1 OF 1 | WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.

T290 E-REV | 7290-1 E-REV

REVISION	BY	DATE	APPROVED
ORIGINATED PER DWR E-2145			
REVISED PER ECN #6682			
REVISED PER ECN #6833			
REVISED PER ECN# 6986			
REVISED PER ECN# 7077			
REVISED PER ECN# 7277			
REVISED PER ECN# 7290			
REVISED PER ECN# 7290-1			

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DO NOT SCALE

HOLE LEGEND		
	HOLE DIA.	TOL.
DRILLED OR PUNCHED HOLE	.015 to .125	± .002
	.126 to .250	± .003
TOLERANCES:	.251 to .500	± .004

IDENT.	DESCRIPTION	QTY.
A		

LOCATION	W.L. PT. NO	GND	VCC
L1	377-0337	8	16
L2	376-0004	7	14
L3, L2A	376-0081	7	14
L4	376-0006	7	14
L5	376-0010	7	14
L6	376-0104	8	16
L12	376-0002	7	14
L8	377-0338	14	28
L9	376-0160	8	16
L10	376-0059	7	14
L11	376-0178	7	14
L13	376-0049	8	16
L14	376-0093	7	14
L15,16,17,32	SEE CHART	12	
L18	377-0269	2	20
L19,30,33	376-0192	8	16
L20	376-0065	11	4
L21,35	376-0082	8	16
L22-29,34-43	SEE CHART	18	
L31	376-0008	8	16
L34	376-0011	10	5
L7	376-0207	7	14

COMPONENT	W.L. PT. NO
Q1	395-0013
Q2,3	395-1050
Q4	374-0002
XTAL 1	321-0022
D1, 2	380-1001
L15-17, 32	376-7003
L18 (SOCKET)	376-9015
L18 (SOCKET)	376-9011
L22-29,34-43 (SOCKET)	376-9014
R21, 22	330-4047
R12,3,4-14,16-20,23-25,27-31	330-3047
R4,5	330-1011
R32	330-3022
R15	320-2033
L1	376-9002
R26	330-3010
C1-8, 27	300-1930
C9-24, 31, 32	300-1931
C25, 46	300-4019
C26	300-4020
C28	300-1068
C30	300-6016
C33-43,	300-1960
C44	300-6022
C29	300-9008
C47	300-1901

VARIATION CHART 210 - 209 - 371 OR 378							
	L15	L16	L17	L22-29	L32	L34-43	
210	378-2080	378-2079	378-2018		378-2077	377-0314	
209	378-2142/82	378-2142/82	378-2142/82	330-3141-45	3 1B-3140-46	377-0314	
371	378-2180	378-2179	378-2178		378-2177	377-0314	
378	378-2084	378-2083	378-2082	377-0314	378-2081	377-0314	
MODEL							
2236 MXC 4K 4 PORT	378-2080	378-2079	378-2018	377-0314	378-2077	377-0314	
2236 MXD 4K 4 PORT	7291-A	7291-D	7291-E	7291-A	7291-D	7291-E	
2236 MXD 2K DMA	7291	7291	7291	7291	7291	7291	
2236 MXC BK 8 PORT	7291-A	7291-D	7291-E	7291-A	7291-D	7291-E	
2236 MXC 8K 8 PORT	7291-B	7291-B	7291-B	7291-B	7291-B	7291-B	

SPARES		
LOCATION	TYPE	SPARES
L4	7474	1
L6	9602	1
L7	74LS00	1
L14	7432	3
L2A	7408	3
L2	7420	1

PROM TYPE	JUMPERS NEEDED
1K	J1,J3,J5,J7
2K	J2,J4,J6,J8

CONN 1

MR	01	
-12V	02	-12V
Ø2	03	INT
3/ON	04	TP1
3/OR	05	
OSC	06	
	07	
TP2	08	
	09	
	10	
	11	
	12	
±0V	13	±0V
±0V	14	±0V
-5V	15	-5V
A0'	16	A0'
A9'	17	A9'
A8'	18	A8'
A6'	19	A6'
A5'	20	A5'
+12V	21	+12V
+12V	22	+12V
D0	23	
D1	24	
D2	25	
D3	26	
D4	27	
D5	28	
D6	29	
D7	30	
+5V	31	+5V
+5V	32	+5V
CIRCUIT SIDE	33	COMP SIDE

J1

TWR	A1	RESET
TDA	B2	RESTDA
	C3	
RES	D4	
SYNC	E5	Ø1
±0V	F6	Ø2
D1	M7	WO
	J8	D0
DS	K9	M1
OUT	L10	D4
D3	M11	MEMR
	N12	D6
D3	P13	STW
	K14	D2
A1	T15	A2
A2	T16	A0
A10	P17	A4
A7	P18	A6
A3	M19	A8
A5	M20	A10
A11	T21	A13
A12	P22	A14
	CIRCUIT SIDE	
	COMP SIDE	

WANG PART NO.	ITEM	QTY.	NAME	MATERIAL	DESCRIPTION
FIRST USED ON	ASSY USED ON		WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.		BY / DATE / APPROVED BY / DATE
			MATERIAL	DWN 454 3-8-77	E ENGR. P. Cote 11-2-77
			MODEL NO. 2236 MXC	CHK 11-2-77	M ENGR.
			SEE ENGRG SPECIFICATIONS No.	E.C. CONTROL	MFG ENGR.
			FINISH	TITLE 8080 INTERACTIVE TERMINAL MEMORY DAUGHTER BOARD	
			TOL EX AS NOTED .XX ± .010 FRAC ± 1/64 .XXX ± .005 ANG ± 1° 30' FINISH	210-7291	E 7291 11
			SCALE	SHT 1 OF 1	WANG PART NUMBER / SIZE / DRAWING NUMBER / REV.

7291 2 7291-1 2

REV	ECN #	BY	DATE	APPROVED
A	3-8-77			
B	4-26-77		10-27-77	10-27
C	5-31-77		8-5-77	8-5
D	6-21-77		8-26-77	8-26
E	7-20-77		9-20-77	9-20
F	8-8-77		10-5-77	10-5
G	8-31-77		10-25-77	10-25
H	9-30-77		11-15-77	11-15
J	10-31-77		12-15-77	12-15
K	11-30-77		1-10-78	1-10
L	12-30-77		1-30-78	1-30
M	1-31-78		2-28-78	2-28
N	2-28-78		3-10-78	3-10
P	3-31-78		4-11-78	4-11
R	4-28-78		5-4-78	5/4/78
S	5-31-78		5-31-78	5/31/78
T	6-30-78		6-15-78	6-15
U	7-31-78		8-1-78	8-1
V	8-31-78		8-29-78	8-29
W	9-30-78		10-12-78	10-12

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DO NOT SCALE

PRELIMINARY

-NOTES-

1. ALL RESISTORS 2.2KΩ 1/4W UNLESS OTHERWISE SPECIFIED

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN [illegible]	5-17-79	E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. 22C11			MFG ENGR	
	SEE ENGRG. SPECIFICATIONS' No.	TITLE	PRINTER DISK CONTROLLER		
FINISH	TOL EX. AS NOTED XX ± FRAC. ± XXX ± ANG. ± FINISH √	210-7342	D	7342	1
	SCALE NONE SHT 1 OF 2	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.

D 7342

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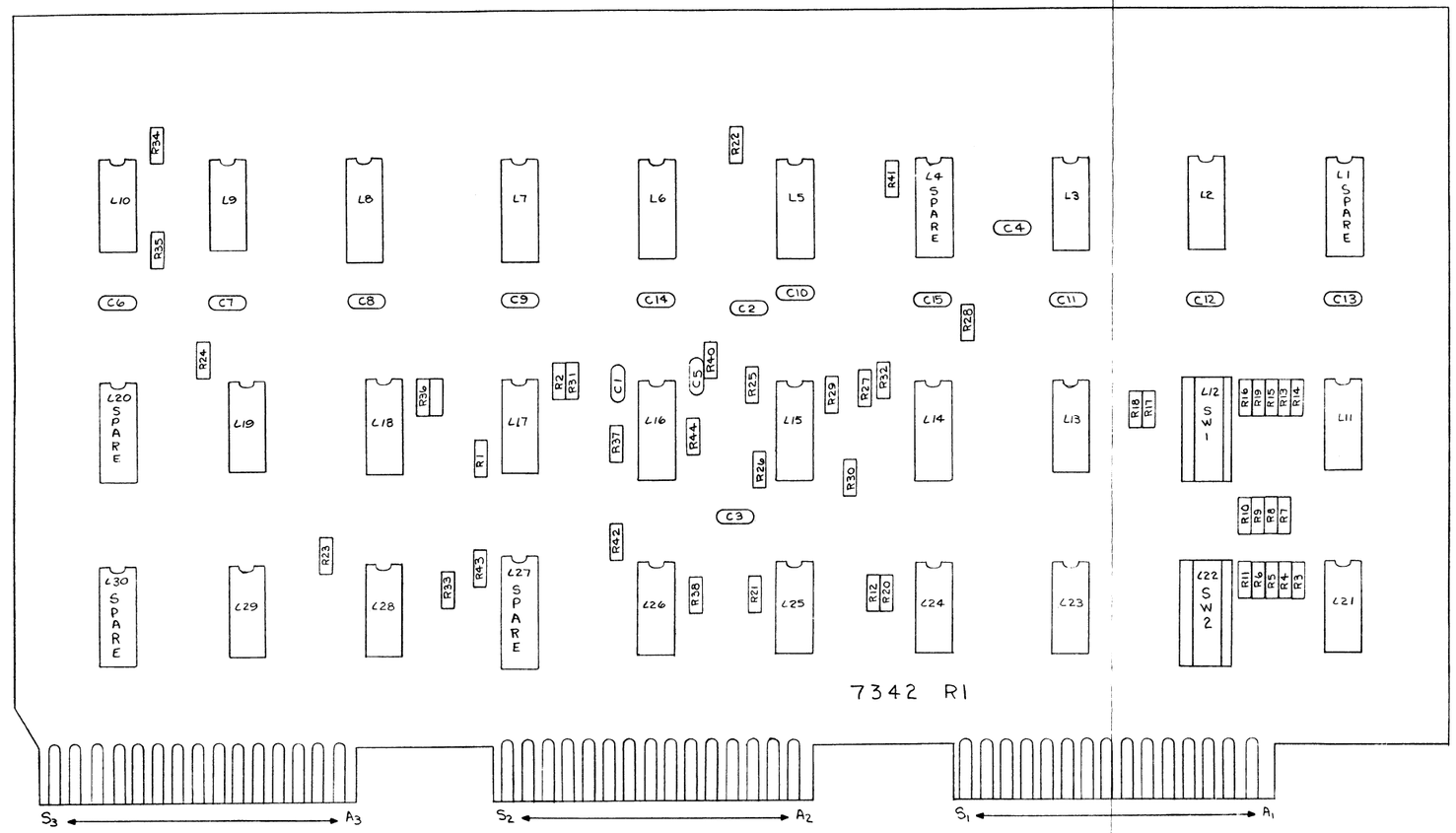
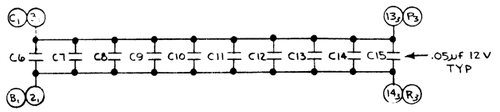
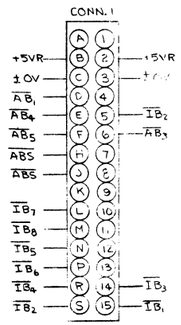
DO NOT SCALE

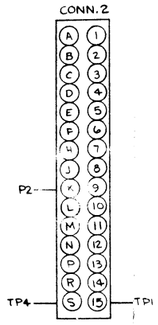
I.C. LOCATION	TYPE	W.L. NO.
L2	7404	376-0010
L3,10	7432	376-0093
L5,6	74175	376-0119
L7,8,14,15	8097	376-0176
L9,17,28	7401	376-0056
L11,13,21,23	74LS266	376-0148
L12,22	8 BANK ROCKER SW	325-1503
L16	9602	376-0104
L18	7406	376-0055
L19	74LS74	376-0155
L24,26	7474	376-0006
L25	7403	376-0028
L29	7400	376-0002

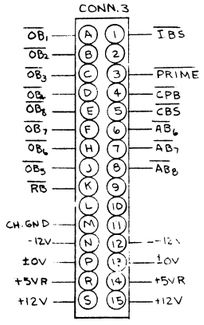
COMPONENT	TYPE	W.L. NO.
R1-36,37-43	2.2K Ω 10% 1/4W	330-3022
R37,44	33K Ω 10% 1/4W	330-4033
C1,5	220pf 500V 5% MICA	300-5004
C2	.001μf 500V 10% (K)	300-1906
C3,4	1000pf 100V 5% MICA	300-5006
C6-15	.05μf 12V +80%-20%	300-1900











PRELIMINARY

DATE	BY	REVISION	NO
8/29/79	LP	ORIGINATED PER PWR#1355 ASPD.	0
9/29/79	LP	REVISED PER ECN#10347 APPD.	1

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY	DAT
	DWN		E ENGR	
	CHK		M ENGR	
			MFG ENGR	

MATERIAL — MODEL NO. 22-C11 — SEE ENGRG. SPECIFICATIONS No.

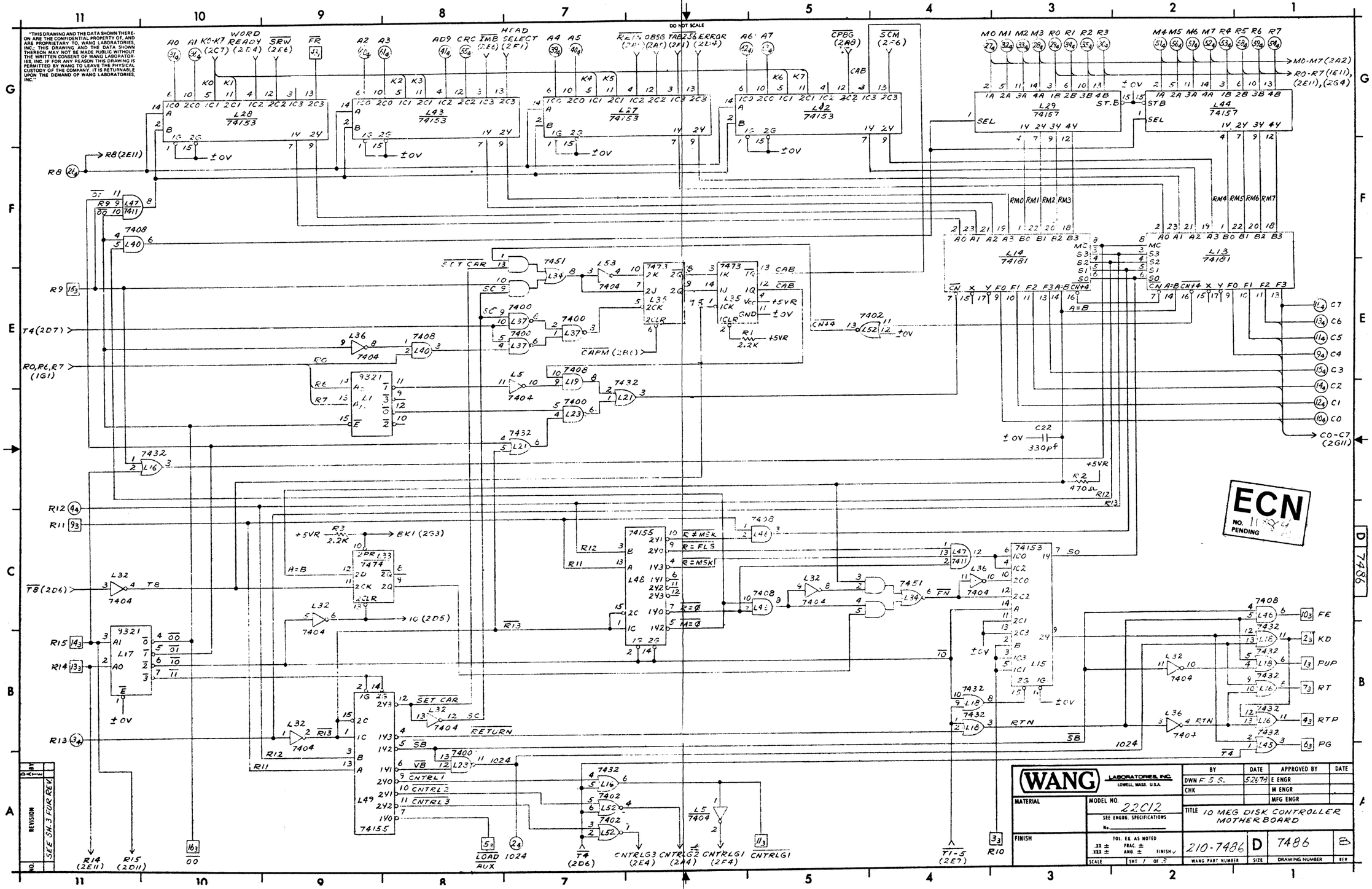
FINISH — TOL EX. AS NOTED .XX ± FRAC ± .XXX ± ANG ± FINISH √

SCALE — SHT 2 OF 2

TITLE: PRINTER DISC CONTROLLER

210-7342 (WANG PART NUMBER) | D (SIZE) | 7342 (DRAWING NUMBER) | 1 (REV)

7342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DO NOT SCALE
A0 A1 K0-K7 WORD READY (2C7) SRW (2E6) FR
A2 A3
AD9 CRC IMB HEAD SELECT (2E6) (2F1)
A4 A5
RESET OBSG TAB256 ERROR (2A1) (2F1) (2E4)
A6 A7
CPBG (2A8)
SCM (2-6)
M0 M1 M2 M3 R0 R1 R2 R3
M4 M5 M6 M7 R4 R5 R6 R7
M0-M7 (2A2)
R0-R7 (1E11), (2E11), (2G4)
L28 74153
L43 74153
L27 74153
L42 74153
L29 74157
L44 74157
L47 74111
L40 7408
L34 7451
L53 7473
L35 7473
L37 7400
L36 7404
L5 7404
L19 7408
L21 7432
L23 7400
L16 7432
L17 9321
L49 74155
L52 7402
L32 7404
L41 7408
L48 74155
L38 7451
L47 7411
L36 7404
L15 74153
L46 7408
L16 7432
L18 7432
L45 7432
L14 74181
L13 74181
C22 330pf
R1 2.2K
R2 470Ω
R3 2.2K
+5VR
±0V
SET CAR
SC
CAPM (2B6)
CN+4
A=B
RETURN
1024
LOAD AUX
CNTRLG3 (2E4)
CNTRLG2 (2A4)
CNTRLG1 (2F4)
CNTRLG1
C7 C6 C5 C4 C3 C2 C1 C0
C0-C7 (2G11)
FE KD PUP RT RTP PG
RTN
T4(2D7)
RO,R1,R7 (1G1)
T8(2D6)
R8 R9 R11 R12 R13 R14 R15
R14 (2E11)
R15 (2D11)
EK1 (2G3)
1C (2D5)
T1-5 (2E7)
R10
00
SEE SH.3 FOR REV.
REVISION
DATE
NO.
ECN NO. 11[illegible] PENDING
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
MATERIAL
FINISH
MODEL NO. 22C12
SEE ENGRG. SPECIFICATIONS
No.
TOL. EX. AS NOTED
.XX ± FRAC ± .XXX ± ANG ± FINISH √
SCALE SHT 1 OF 3
TITLE 10 MEG DISK CONTROLLER MOTHER BOARD
BY DWN F.S.S. 5/26/79
CHK
APPROVED BY E ENGR M ENGR MFG ENGR
DATE
210-7486 WANG PART NUMBER
D SIZE
7486 DRAWING NUMBER
B REV
7486

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DO NOT SCALE

ECN NO. (illegible) PENDING

BY	DATE	APPROVED BY	DATE
DWN F.S.S.	5/24/78	E ENGR	
CHK		M ENGR	
		MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL

MODEL NO. 22212
SEE ENGRG. SPECIFICATIONS
No.

FINISH

TOL. EX. AS NOTED
XX ± FRAC ±
XXX ± ANG. ± FINISH √

SCALE | SHT 2 OF 3

TITLE 10 MEG DISK CONTROLLER MOTHERBOARD

210-7486 | D | 7486 | B

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.

REVISION	BY	DATE
SEE SH. 3 FOR REV'S		

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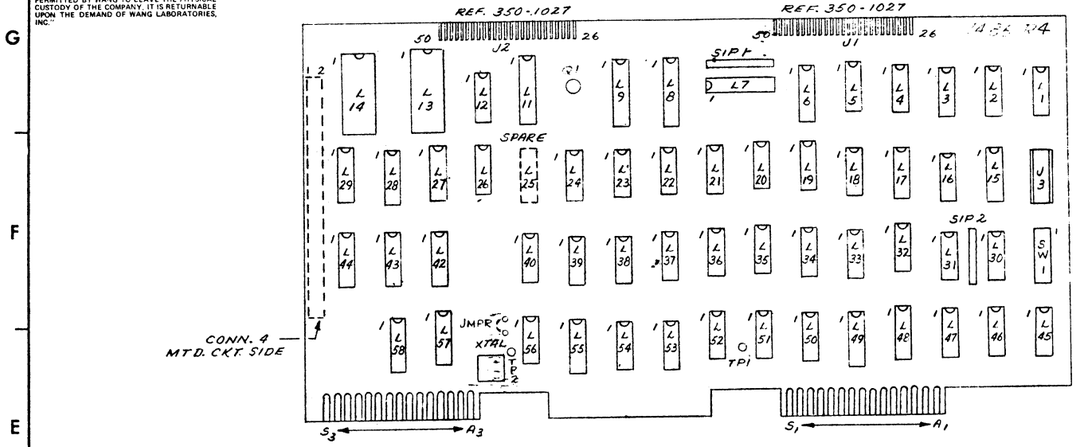
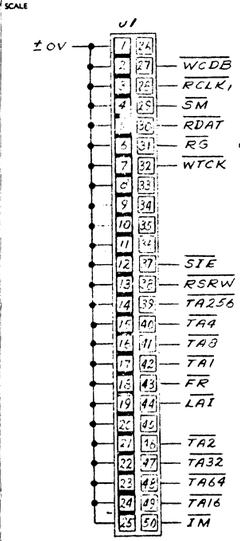
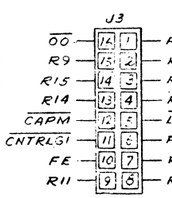
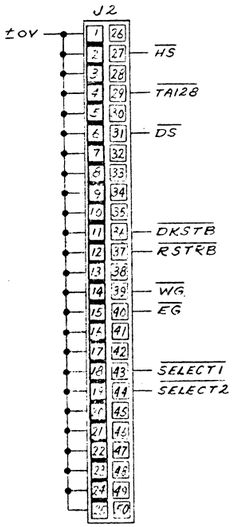
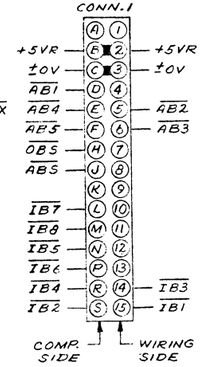
DO NOT SCALE

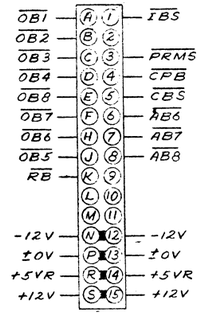


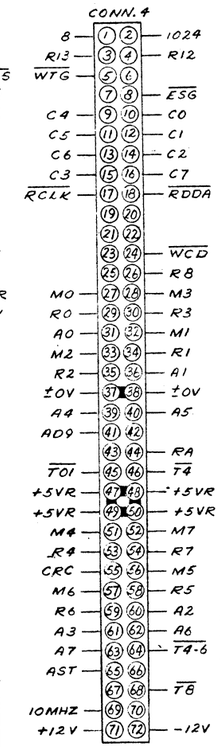










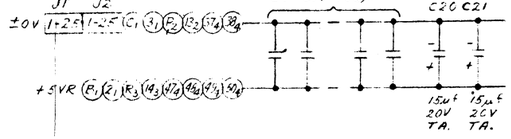


I.C. LOCATION	TYPE	W.L.NO.
L1,4,33	7474	376-0006
L2	7410	376-0003
L3,23,37	7400	376-0002
L5,32,36,53,56	7404	376-0010
L6	7476	376-0007
L10,41	NOT USED	
L7-9,11	74LS244	376-0288
L12,20,26,35	7473	376-0005
L13,14	74181	376-0099
L15,27,28,42,43,55	74153	376-0048
L16,18,21,38,45,54	7432	376-0053
L17	9321	376-0096
L19,40,45	7408	376-0081
L22,47	7411	376-0154
L24	LM339	376-0240
L25	SPARE	
L29,44	74157	376-0082
L30,31	74LS266	376-0148
L34	7451	376-0012
L39	74164	376-0102
L48,49	74155	376-0049
L50,51	7403	376-0020
L52	7402	376-0019
L57,58	74253	376-0138

LOCATION	TYPE	SPARES
L2	7410	1
L3	7400	1
L4	7474	1
L5	7404	1
L22	7411	2
L24	LM339	2
L45	7432	3
L46	7408	1

COMPONENT	TYPE	W.L.NO.
R1,3,11-13,16,22 C1,23,24	2.2K	330-3022
R2,10	470Ω	330-2047
R4,6	220Ω	330-2022
R5	180Ω	330-2018
R7	1.8K	330-3018
R8	4.7K	330-3047
R9	27K	330-4027
R14	270Ω	330-2027
R15	150Ω	330-2015
R17	3.3K	330-3033
R18	1.5K	330-3015
R19	120K	330-4012
R22	47Ω	330-2047
SIP1	330Ω/10 pin	330-2037
SIP2	7.5K	330-3075
C1	.002μf	300-1913
C8	.1μf	300-1903
C9	.05μf	300-1905
C11,20,21	15μf 20V TA.	300-1435
C4,7	.01μf	300-1901
C12,C	330pf 1KV	300-1844
C5-10	.05μf	300-1905
C22	330 pF	300-1830

COMPONENT	TYPE	W.L.NO.
D1,3	5V1.	340-1001
D2	INS250 ZEN.	350-2049
SW1	CRANK RKR SW.	325-1503
XTAL	10 MHZ	321-0008
Q1	2N2222A	375-1005
U1,2,9	SN74S00	350-1027
U3	16 PIN SKT.	376-0129
CONN.	251-10336-2	350-5029M



ECN NO. 11854 PENDING

NMEMONIC	COORD.
A0,A7	1G6
ABI-AB8	2C11
ABS	2C11
AD9	1G8
AST	2G8
CO-C7	1E1
CAPM	2A5
CBS	2A7
CNTRLG1	1A5
CPB	2A8
CRC	1G8
DKSTB	2G1
DS	2E1
EG	2E1
ESG	2G2
FE	1C1
FR	1G9
HS	2E1
IBI-IB8	2B1
IBS	2F1
IM	2G6
KD	1B1
LAI	2G5
LOAD AUX	1A8
M0-M7	1G2

NMEMONIC	COORD.
JET-OB8	2G9
OBS	2A6
OO	1A10
PG	1A1
PRMS	2D11
PUP	1B1
RO-R7	1G2
R8	1F11
R9	1E11
R10	1A3
R11,12	1C11
R13-15	1B11
RA	2D11
RB	2G1
RCLK	2G5
RCLK1	2G5
RDAT	2G6
RDDA	2G4
RDG	2G3
RC	2E1
RSTRB	2G1
RSRW	2G6
RT	1B1
RTP	1B1
SELECT1	2F1
SELECT2	2E1
SIE	2G5
SM	2G6

NMEMONIC	COORD.
TA1-TA128	2D1
TA256	2E1
T01	2A4
T4	2A4
T4-6	2A4
T8	2A4
WCD	2G2
WCDB	2G1
WG	2A5
WTCK	2G5
WTG	2G2
5	2D11
10 MHZ	2D11
1024	1A7

E-REV. 4

NO.	REVISION	BY	DATE
01	ORIGINATED PER LWR #5267	FSS	5/26/78
02	REVISED PER ECN #5282 & APPD. ADDITIONS	FSS	6/2/78
03	REVISED PER ECN #5284 & APPD. ADDITIONS	FSS	11-16-78
04	REVISED PER ECN #5332 & APPD. ADDITIONS	FSS	11-16-78
05	REVISED PER ECN #5282 & APPD. ADDITIONS	FSS	11-16-78
06	REVISED PER ECN #5328 & APPD. ADDITIONS	FSS	11-16-78
07	ADDED PWR. CONN. J3	TCB	1-9-79
08	DELETED SHUNT ON J3	TCB	7-4-79
09	REVISED PER ECN 11854	MDC	1-21-80

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY	DATE
	DWN F.S.S.	5/26/78	E ENGR DILLON	10/1/78
	CHK G.D.	10-16-78	M ENGR	
			MFG ENGR	
MATERIAL	MODEL NO. 22012		TITLE 10 MEG DISK CONTROLLER MOTHERBOARD	
	SEE ENGRG. SPECIFICATIONS No.			
FINISH	TOL. EX. AS NOTED .XX ± FRAC ± .XXX ± ANG. ± FINISH √		210-7486	D 7486 9
	SCALE	SHT 3 OF 3	WANG PART NUMBER	SIZE DRAWING NUMBER REV.

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DO NOT SCALE

R_0 R_1 R_2 R_3 R_4 R_5 R_6 R_7 R_8 R_9 R_{10} R_{11} R_{12} R_{13} R_{14} R_{15}

FE (10) PUP (1) CAPM (12) 1024 (2) RT (7) PG (6) RS (70) RTP (4) T4 (46) (1G6) KD (2)

CAPM (2F11)

L18 2911 — L5 2911 — L6 2911

L10 2708 — L2 2708

L1 74LS377 — L3 74LS377

L13 7404 — L40 7404

L15 9321

L7 74193 — L8 74193 — L9 74193

L20 2114 — L21 2114

L22 74LS377

L31 74157 — L43 74157

L19 74LS244

L14 7400 — L29 7432 — L37 7402 — L41 7427

LOAD AUX (5) — T_4 (1C11) — $\overline{T_{01}}$ (45) — $\overline{T_{01}}$ (2G7)(1E7)

AD_9 (41) — AD_0 (2G11) — AD_9 (2F11)(2D3)

$M_0 - M_7$ (2A10): M_7 (52) M_6 (57) M_5 (56) M_4 (51) M_3 (28) M_2 (33) M_1 (32) M_0 (27)

$R_3 - R_7$ (2F11) — R_7 (2E11) — ADI (2G5) — $\overline{ADI}$ (2G5) — STW (2F9) — RDG (2B7)

$A_0 - A_7$ (2A4) — $C_0 - C_7$ (2C11)

Q1 7905 COM. — C1 1 MF 35V (T) — C2 15 MF 20V (T) — −5VR

−12V (12) — ØØ (16) — T_B (68) — $\overline{T_{3-7}}$ (62)

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY	DATE
	DWN		E ENGR	
	CHK		M ENGR	
			MFG ENGR	
MATERIAL	MODEL NO. 2202C — SEE ENGRG SPECIFICATIONS No.	TITLE 10MEG DISK CONTROLLER DAUGHTER BOARD		
FINISH	TOL. EX. AS NOTED XX ± FRAC ± XXX ± ANG ± FINISH √	210-7431A	D	7497	9
	SCALE — SHT 1 OF 3	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.

NO.	REVISION	BY	DATE
	SEE SHT 3		

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DO NOT SCALE

RDG (8) · ESG (8) · WTG (5) · 10MHz (69) · WCD (24)

AD0 (1G3) · AD9 (1G3) · CAPM (1G10) · R0-R3 (1E7) · R7 (1E7) · CNT RLG1 (11) · AST (65) · RDDA (16) · RCLK (17) · C0-C7 (1B3) · M0-M7 (1G2) · WTG (2G9)

WTG (2B10) (2E4) · STW (1D5) · RD/WT · WT · TP1 · TP2 · BK1 (2B5) · BK2 (2D3) · BK3 (2E8) · BK4 (2G8) · BK4 (2F2) · BK3 (2E3) · R CLK (2E3) · PRC (2E3) (2C7) · PRC (2E8) · RCLK (2E10) · SYNC · RDG (1C3) · T01 (1G2) · ADI (1D6) · ADI (1D6) · WD · CRC · BK1 (2E10) · A0-A7 (1B3)

L4 74195 · L11 7476 · L17 7476 · L16 7404 · L13 7404 · L23 7408 · L24 9401 · L25 7400 · L26 7408 · L27 7410 · L28 74193 · L30 74151 · L32 74298 · L33 74157 · L34 7474 · L35 7476 · L36 7432 · L37 7474 · L38 7474 · L39 7402 · L42 74164 · L44 74298 · L45 74157 · L126 7408 · L127 7410 · L134 7474 · L135 7476 · L136 7432 · L137 7474

R2.2K7 · R5 2.2K · R6 10K · R7 2.2K · R8 2.2K · R9 2.2K

(31) A0 · (36) A1 · (60) A2 · (61) A3 · (39) A4 · (40) A5 · (62) A6 · (63) A7

DATE	BY	REVISION	NO.
		SEE SHT 3	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

BY	DATE	APPROVED BY	DATE
DWN		E ENGR	
CHK		M ENGR	
		MFG ENGR	

MATERIAL · FINISH · MODEL NO. 2260C · SEE ENGRG. SPECIFICATIONS No. ____ · TOL. EX. AS NOTED XX ± FRAC. ± XXX ± ANG. ± FINISH √ · SCALE FULL · SHT 2 OF 3

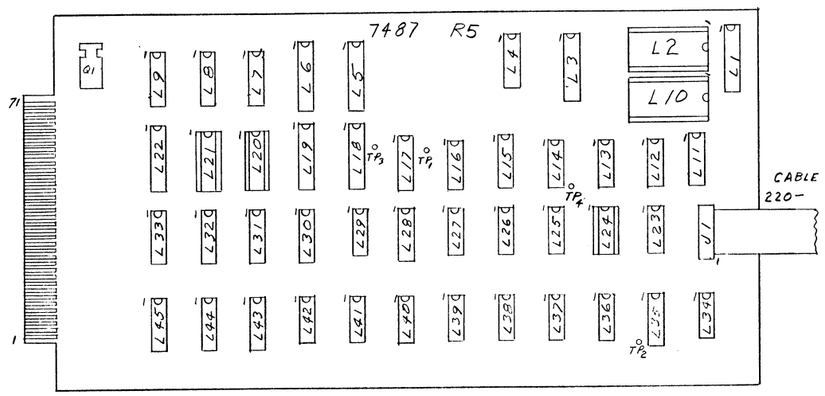
TITLE 10 MEG DISK CONTROLLER DAUGHTER BOARD

210-7487A · WANG PART NUMBER · D · SIZE · 7487 · DRAWING NUMBER · 9 · REV.

"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF, AND ARE PROPRIETARY TO, WANG LABORATORIES, INC. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."

DO NOT SCALE

MNEMONIC	COORDINATE
A0-A7	2A6
AD9	1G4
AST	2E11
C0-C7	1A4
CAPM	1G11
CNT RLG1	2E11
CRC	2E1
ESG	2G9
FE	1G11
KD	1B11
LOAD AUX	1G6
M0-M7	1F2
PG	1F11
PUP	1G11
R0-15	1G9
R CLK	2D11
RDDA	2D11
RDG	2G10
RS	1E11
RT	1F11
RTP	1C11
T4	1C11
T8	1A6
T01	1G3
T3-7	1A6
WCD	2G3
WTG	2G9
ØØ	1A7
8	2C3
1024	1F11
10 MHz	2G7



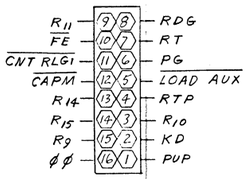
210 = 209 + 377 OR 378

MOD II	209	210	L2	L10
2260C 10 MEG	7487	7487A	378-2210-R5	378-2211-R5
2260C 5 MEG	7487	7487B	378-2212-R5	378-2213-R5
2260C 2.5 MEG	7487	7487C	378-2214-R5	378-2215 R5

LOCATION	W. L. PART No	TYPE
L1, 3, 22	376-0313	74LS377
L2, 10	SEE CHART	2708
L4	376-0097	74195
L5, 6, 18	377-0347	2911
L7, 8, 9, 23	376-0053	74193
L11, 17, 35	376-0007	7476
L12, 29, 36	376-0093	7432
L13, 16, 40	376-0010	7404
L14, 25, 37	376-0002	7400
L15	376-0096	9321
L19	376-0288	74LS244
L20, 21	377-0341L	2114
L23, 26	376-0081	7408
L24	376-0250	9401
L27	376-0003	7410
L30	376-0047	74151
L31, 33, 43, 45	376-0082	74157
L32, 44	376-0138	74298
L34, 38	376-0006	7474
L39	376-0016	7402
L41	376-0125	7427
L42	376-0102	74164

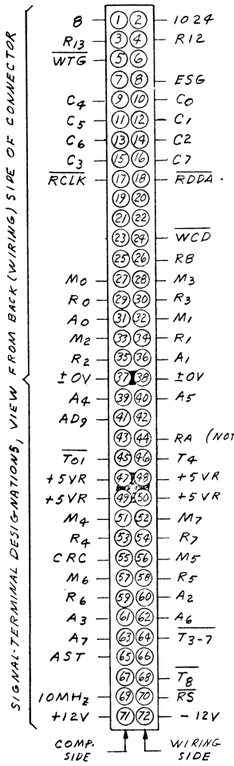
IC TYPE	LOCATION	STAKE
7400	L37	3
	L14	1
7402	L39	1
7404	L40	5
7432	L12	2
9321	L15	1

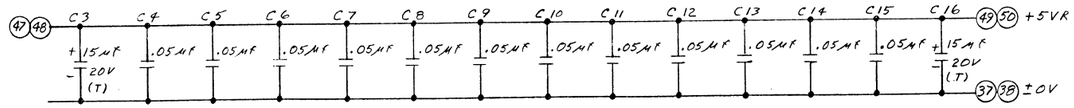
J1



COMPONENT	W.L. PART No.	TYPE
R1-5, 7-9	330-4022	2.2K 1/4W 10%
R6	331-4010	10K
C1	300-4000	1MF 35V (T)
C2, 3, 16	300-4022	15MF 20V (T)
C4-15	300-1900	.05MF CER
Q1	374-0002	7905 REG
L2, 10	376-9003	SOCKET 24 PIN
L20-21	376-9014	SOCKET 18 PIN
L24	376-9001	SOCKET 14 PIN
J1	376-9024	SOCKET 16 PIN
L5, 6, 18	376-9020	SOCKET 20 PIN

SIGNAL-TERMINAL DESIGNATIONS, VIEW FROM BACK (WIRING) SIDE OF CONNECTOR





E- REV
[2]

NO.	REVISION	BY	DATE
6	ORG. PER DWR 503 APP'D		4/27/78
7	REVISED PER ECN A 763 APP'D		4/27/78
8	REVISED PER ECN A 890 APP'D		5/31/78
9	REVISED PER ECN B 115 APP'D		6/30/78
10	REVISED PER ECN B 1078 APP'D		7/31/78
11	REV. PER ECN B 1345 APP'D		9/13/78
12	REV. PER ECN B 1398 APP'D		9/13/78
13	REV PER ECN B 1129 APP'D		10/13/78
14	REV PER ECN B 1169 APP'D		11/13/78
15	REV PER ECN B 1178 APP'D		11/13/78
16	REV PER ECN B 1178 APP'D		11/13/78
17	REV PER ECN B 1178 APP'D		11/13/78
18	REV PER ECN B 1178 APP'D		11/13/78
19	REV PER ECN B 1178 APP'D		11/13/78
20	REV PER ECN B 1178 APP'D		11/13/78
21	REV PER ECN B 1178 APP'D		11/13/78
22	REV PER ECN B 1178 APP'D		11/13/78
23	REV PER ECN B 1178 APP'D		11/13/78
24	REV PER ECN B 1178 APP'D		11/13/78
25	REV PER ECN B 1178 APP'D		11/13/78
26	REV PER ECN B 1178 APP'D		11/13/78
27	REV PER ECN B 1178 APP'D		11/13/78
28	REV PER ECN B 1178 APP'D		11/13/78
29	REV PER ECN B 1178 APP'D		11/13/78
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42	REV PER ECN B 1178 APP'D		11/13/78
43	REV PER ECN B 1178 APP'D		11/13/78
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69	REV PER ECN B 1178 APP'D		11/13/78
70	REV PER ECN B 1178 APP'D		11/13/78
71	REV PER ECN B 1178 APP'D		11/13/78
72	REV PER ECN B 1178 APP'D		11/13/78

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN		7-27-78	E ENGR DILLON	10/16/78
CHK G.D.		10/13/78	M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO. 2260C

SEE ENGRG. SPECIFICATIONS No.

FINISH

TOL EX. AS NOTED
XX ± FRAC ±
XXX ± ANG. ± FINISH √

SCALE — SHT 3 OF 3

TITLE 10 MEG DISK CONTROLLER DAUGHTER BOARD

210-7497A | D | 7487 | 9

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.

7487

"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF, AND ARE PROPRIETARY TO, WANG LABORATORIES, INC. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."

DO NOT SCALE

PRELIMINARY

ECN NO. 11884 PENDING

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY	DATE
	DWN		E ENGR	
	CHK		M ENGR	
			MFG ENGR	

MATERIAL	MODEL NO. 2260 B/C	TITLE DISK/MUX CONTROLLER MOTHERBOARD			
	SEE ENGRG. SPECIFICATIONS No.				
FINISH	TOL. EX. AS NOTED .XX ± FRAC. ± .XXX ± ANG. ± FINISH √	210-7488	D	7488	6
	SCALE SHT 1 OF 3	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.

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DO NOT SCALE

PRELIMINARY

ECN NO. 11887 PENDING

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY	DATE
	DWN	7-11-8	E ENGR	
	CHK		M ENGR	
MATERIAL	MODEL NO. 2260B/C		MFG ENGR	
	SEE ENGRG. SPECIFICATIONS No.	TITLE	DISK/MUX CONTROLLER MOTHER BOARD	
FINISH	TOL. EX. AS NOTED .XX ± FRAC. ± .XXX ± ANG. ± FINISH √	210-7488	D 7488	6
	SCALE	SHT 2 OF 3	WANG PART NUMBER	SIZE DRAWING NUMBER REV.

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DO NOT SCALE

COMPONENT	W.L. PART NO.	TYPE
Q1	375-1005	2N2222A
J4	350-0029 M	72 PIN CONN.
D1,3	380-1001	SIL. DIODE
D2	380-2048	IN5230 ZENER
J1,2	350-2097	50 PIN CONN.
J3	350-2096	36 PIN CONN.
J5	376-9024	16 PIN CONN.
SIP1	333-0807	330/220Ω RES.
SIP2,3	333-0813	470 RES.
R1,2,16,19-24,28	330-3022	2.2K. ¼W 10%
R8,10,12,17,25-27	330-2047	470Ω
R3,5	330-2022	220Ω
R4	330-2018	180Ω
R7	330-4027	27K
R6	330-3018	1.8K
R9	330-3047	4.7K
R11	330-2010	100Ω
R13	330-3033	3.3K
R14	330-3015	1.5K
R15	330-5010	100K ¼W 10%
C1	300-1913	.002μF
C7	300-1903	.01μF
C20	300-1130	330pF
C2	300-1010	10PF
C3,18,19	300-4022	15μF 20V TANT
C6,8	300-1906	.001μF
C4,5	300-4045	220μF 15V TANT
C9-17	300-1900	.05μF 12V
XTAL	321-0008	10MHz
R18	330-1047	47Ω ¼W 10%

1330

LOCATION	W.L. PART NO	TYPE
L1,24,25,39,40,51	376-0048	74153
L2,20,34	-0002	7400
L3,22,30	-0006	7474
L4,29,33,49,52	-0010	7404
L5	-0007	7406
L6,7,8,9	-0288	74LS244
L10,17,23,32	-0005	7473
L11,12	-0099	74181
L13,15,18,35,50	-0093	7432
L14	-0096	9321
L16,37,42	-0081	7408
L19,43	-0194	7411
L21	-0240	LM 339
L26,41	-0082	74157
L36	-0102	74164
L44,45	-0049	74155
L46,47	-0028	7403
L48	-0016	7402
L53,54	-0138	74298
L31	376-0012	7451
L27,28		SPARES
L38	NOT USED	

LOCATION	TYPE	SPARES
L2	7400	1
L4	7404	2
L18	7432	1
L19	7411	2
L21	LM339	2
L22	7474	1
L42	7408	1

CONN. 4

B	1	1024	2
R13	3	R12	4
WTG	5		6
	7	ESG	8
C4	9	C0	10
C5	11	C1	12
C6	13	C2	14
C3	15	C7	16
RCLR	17	RDDA	18
	19		20
	21		22
	23	WCD	24
	25	R8	26
M0	27	M3	28
R0	29	R3	30
A0	31	M1	32
M2	33	R1	34
R2	35	A1	36
±0V	37	±0V	38
A4	39	A5	40
AD9	41		42
	43	RA	44
T01	45	T4	46
+5VR	47	+5VR	48
+5VR	49	+5VR	50
MA	51	M7	52
R4	53	R7	54
CRC	55	M5	56
M6	57	R5	58
R6	59	A2	60
A3	61	A6	62
A7	63	T4-6	64
AST	65		66
	67	T6	68
10MHZ	69		70
+12V	71	-12V	72

MNEMONICS	COORDINATES
A0-A7	1G7
ABS, ABB	2C11
ABT	2A8
AST	1G6
C0-C7	2B4
CNTRL	2A9
CNTRLGT	1A5
CPBB	1G5
CRC	1G8
DS	2E1
DKSTB	2G1
ESG	2E1
ESG	2G2
FE	1B1
FR	1G9
+5VR	2E1
+5VR	2G1
+5VR	2F1
+5VR	2G6
IBS	1B1
IO	2G5
LAT	1A6
LOAD AUX	1G2
M0-M7	1A10
OO	2G9
OBT-OB6	2A8
OBS	1A1
P6	2B11
PRMS	1E1
PUP	1B1
R0-R7	1G2
R8	1F11
R9	1E11
R10	1A4
R11,12	1C11
R13,14,15	1B11
RA	2D11
RB	2F1
RCLK	2A5
RDAT	2G5
RDDA	2A6
P6S	2G3
RG	2D1
RSTRB	2G6
RTP	1B1
RTP	1B1
SELECT	2E1
SELECT1	2E1
SLE	2G5
SM	2G6
T01	2A6
T4	2A6
T4-6	2A5
T6	2A6
TA1-TA128	2D1
TA 256	2E1
WCD	2G2
WCDB	2G1
WG	2A9
WTCK	2G5
WTG	2G2
8	2A5
1024	2A7
10MHZ	2B11

NO.	REVISION	BY	DATE
0	ORIGINATED PER DWR # 2003		7-11-78
1	REVISED PER ECN # 3220		8-8-78
2	REVISED PER ECN # 3330		9-14-78
3	REVISED PER ECN # 3550		10-16-78
4	ADDED P/O 2260 ASSY		2-8-79
5	REVISED PER ECN # 3725		4-27-79
6	ECN # 10265		1-15-79

PRELIMINARY (E-REV 6)

	BY	DATE	APPROVED BY	DATE
DWN	ER	7/20/78	E ENGR DILLON	8-8-78
CHK	G.D.	8-8-78	M ENGR	
			MFG ENGR	

WANG LABORATORIES INC. LOWELL, MASS. U.S.A.

MATERIAL

MODEL NO. 2260 B/C

SEE ENGRG. SPECIFICATIONS No.

FINISH

TOL. EX. AS NOTED XX ± FRAC. ± XXX ± ANG. ± FINISH √

SCALE — SHT 3 OF 3

TITLE DISK/MUX CONTROLLER MOTHERBOARD

210-7488 | D | 7488 | 6

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.

ECN NO. 11884 PENDING

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DO NOT SCALE

WORD READY (2C7) · SRW (2E6) · FR · HEAD SELECT (2F1) · REIN (2A11) · OBSG (2A5) · TAB256 ERROR (2D4) · CPBG (2A9) · SCM (2E6) · CAB

M0 M1 M2 M3 R0 R1 R2 R3 · M4 M5 M6 M7 R4 R5 R6 R7

→ M0-M7 (2A2)
→ R0-R7 (1E11), (2E11), (2G4)

L28 74153 · L42 74153 · L27 74153 · L41 74153 · L29 74157 · L43 74157 · L14 74181 · L13 74181

→ K8 (2E11)

SET CAR · SC · CAPM (2B6) · CN+4 · A=B

→ T4 (2D7)

→ R0, R6, R7 (1G1)

→ T8 (2D6)

→ 10 (2D5)

→ BK1 (2G3)

R12 · R11 · R13 · R9 · R15 · R14

SET CAR · SC · RETURN · SB · VB · CNTRL1 · CNTRL2 · CNTRL3 · 1024

L32 7404 · L36 7404 · L5 7404 · L52 7404 · L45 7408 · L40 7408 · L20 7408 · L34 7451 · L37 7400 · L24 7400 · L22 7432 · L17 7432 · L51 7402 · L46 7411 · L33 7474 · L18 9321 · L35 7473 · L16 74153 · L19 7432 · L44 7432

RM0 RM1 RM2 RM3 · RM4 RM5 RM6 RM7

C28 150pf · R1 2.2K · R2 470Ω · R3 2.2K

C7 C6 C5 C4 C3 C2 C1 C0 → C0-C7 (2G11)

FE · KD · PUP · RT · RTP · PG · RTN

T1-5 (2E7) · R10 · R14 (2E11) · R15 (2D11) · 00 · LOAD AUX · T4 (2D6) · CNTRLG3 (2E4) · CNTRLG2 (2H4) · CNTRLG1 (2F4) · CNTRLG1

+5VR · ±0V

NO.	REVISION	BY	DATE
A	SEE SH. 3 FOR REV.		

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN			E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO. 2260C
SEE ENGRG. SPECIFICATIONS
No.

TITLE 10 MEG DISK CONTROLLER MOTHER BOARD

FINISH

TOL. EX. AS NOTED
XX ± FRAC ± XXX ± ANG ± FINISH √

SCALE · SHT 1 OF 2 · 210-7686 WANG PART NUMBER · D SIZE · 7686 DRAWING NUMBER · 1 REV

D 7686

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DO NOT SCALE

BY	DATE	APPROVED BY	DATE
DWN JD	1.25.M	E ENGR	
CHK		M ENGR	
		MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL

MODEL NO. 2260C
SEE ENGRG. SPECIFICATIONS
No.

FINISH

TOL. EX. AS NOTED
XX ± FRAC ±
XXX ± ANG. ± FINISH √

TITLE 10 MEG DISK CONTROLLER MOTHERBOARD

210-7686 | D | 7686 | 1
WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.

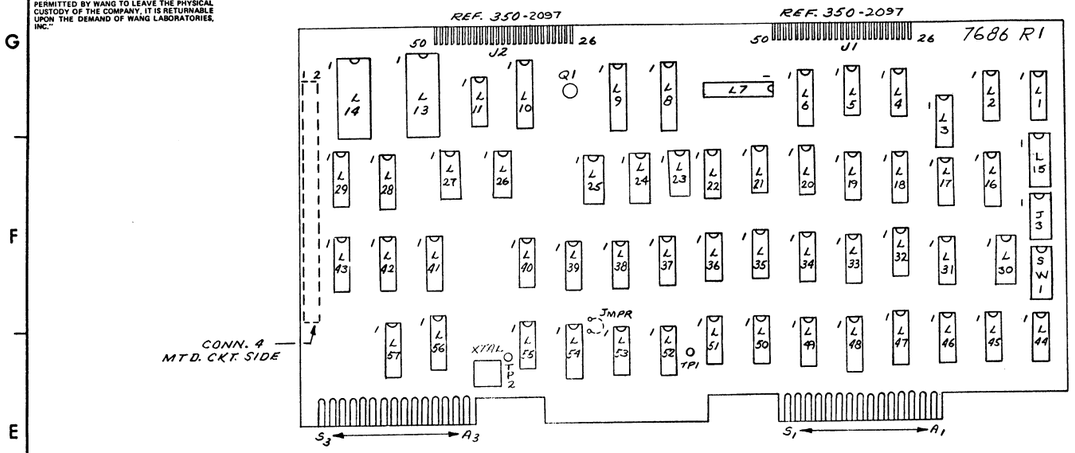
SCALE | SHT 2 OF 3

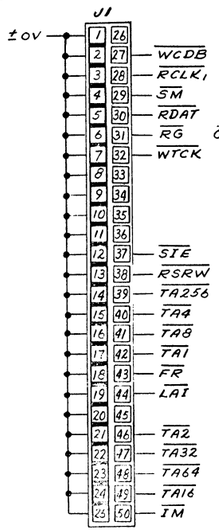
NO.	REVISION	BY	DATE
A	SEE SH. 3 FOR REV.		

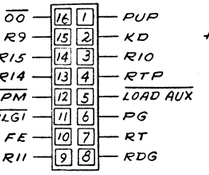
D 7686

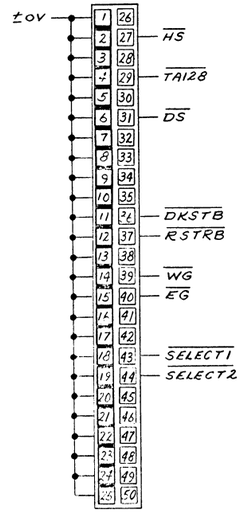
"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF, AND ARE PROPRIETARY TO, WANG LABORATORIES, INC. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."

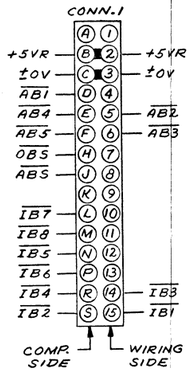
DO NOT SCALE

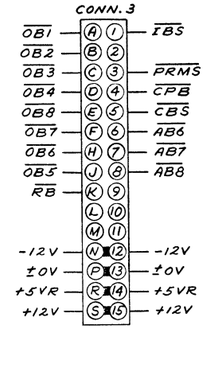


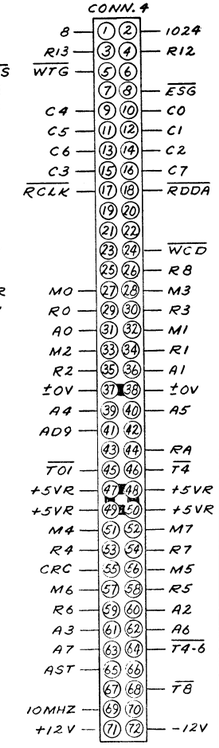










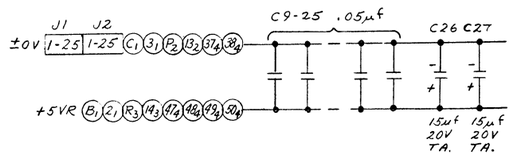


I.C. LOCATION	TYPE	W.L.NO.
L1,4,33	7474	376-0006
L2	7410	376-0003
L3,24,37	7400	376-0002
L5,32,36,52,55	7404	376-0010
L6	7476	376-0007
L12	NOT USED	
L7-10	74LS244	376-0288
L11, 21,26,35	7473	376-0005
L13,14	74181	376-0099
L16,27,28,41,42,54	74153	376-0048
L17,19,22,38,44,53	7432	376-0093
L18	9321	376-0096
L20,40,45	7408	376-0081
L23,46	7411	376-0194
L25	LM339	376-0240
L15	SPARE	
L29,43	74157	376-0082
L30,31	74LS266	376-0148
L34	7451	376-0012
L39	74164	376-0102
L47,48	74155	376-0049
L49,50	7403	376-0028
L51	7402	376-0016
L56,57	74298	376-0138

LOCATION	TYPE	SPARES
L2	7410	1
L3	7400	1
L4	7474	1
L5	7404	1
L23	7411	2
L25	LM 339	2
L44	7432	3
L45	7408	1

COMPONENT	TYPE	W.L. NO.
R1,3,27-36,41 43,44,46,47	2.2K	330-3022
R2,26	470Ω	330-2047
R4-11	330Ω	330-2033
R12-19,20,22	220Ω	330-2022
R21	180Ω	330-2018
R23	1.8K	330-3018
R24	4.7K	330-3047
R25	27K	330-4027
R37	270Ω	330-2027
R38	100Ω	330-2010
R39	3.3K	330-3033
R40	1.5K	330-3015
R42	100K	330-5010
R45	47Ω	330-1047
C1	.002μf	300-1913
C8	.01μf	300-1903
C2	10pf	300-1010
C3,26,27	15μf 20V TA.	300-4022
C4,7	.001μf	300-1906
C5,6	220μf 15V TA.	300-4045
C9-25	.05μf	300-1900
C28	150pf	300-1150

COMPONENT	TYPE	W.L.NO.
D1,3	SIL.	380-1001
D2	IN5230 ZEN.	380-2048
SW1	8BANK RKR SW.	325-1503
XTAL	10 MHZ	321-0008
Q1	2N2222A	375-1005
J1,2	5740500	350-2097
J3	16 PIN SKT.	376-9024
CONN.4	241-10036-2	350-0029



NMEMONIC	COORD.
A0-A7	1G8
AB1-AB8	2C11
ABS	2C11
AD9	1G8
AST	2G8
C0-C7	1E1
CAPM	2A5
CBS	2A7
CNTRLG1	1A5
CPB	2A8
CRC	1G8
DKSTB	2G1
DS	2E1
EG	2E1
ESG	2G2
FE	1C1
FR	1G9
HS	2E1
IB1-IB8	2B1
IBS	2F1
IM	2G6
KD	1B1
LAI	2G5
LOAD AUX	1A8
M0-M7	1G2

NMEMONIC	COORD.
OE1-OB8	2G9
OBS	2A6
OO	1A10
PG	1A1
PRMS	2D11
PUP	1B1
R0-R7	1G2
R8	1F11
R9	1E11
R10	1A3
R11,12	1C11
R13-15	1B11
RA	2D11
RB	2G1
RCLK	2G5
RCLK1	2G5
RDAT	2G6
RDDA	2G4
RDG	2G3
RG	2E1
RSTRB	2G1
RSRW	2G6
RT	1B1
RTP	1B1
SELECT1	2E1
SELECT2	2E1
SIE	2G5
SM	2G6

NMEMONIC	COORD.
TAI-TA128	2D1
TA256	2E1
TOI	2A4
T4	2A4
T4-6	2A4
T8	2A4
WCD	2G2
WCDB	2G1
WG	2A5
WTCK	2G5
WTG	2G2
8	2D11
10 MHZ	2D11
1024	1A7

NO.	REVISION	BY	DATE
0	ORIGINATED PER DWR# 1502 APPD. 3-13-79	SD	1-25-79
1	REV. PER ECN # 1150 APPD. 5/16/79	SD	3/13/79

E-REV. 0

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY	DATE
	DWN SD	1-25-79	E ENGR DOOLEY	3/13/79
	CHK G.D.	3-13-79	M ENGR	
			MFG ENGR	
MATERIAL	MODEL NO. 2260C SEE ENGRG. SPECIFICATIONS No.		TITLE 10 MEG DISK CONTROLLER MOTHER BOARD	
FINISH	TOL. EX. AS NOTED XX ± FRAC. ± XXX ± ANG. ± FINISH √		210-7631	D 7686 1
	SCALE	SHT 3 OF 3	WANG PART NUMBER	SIZE DRAWING NUMBER REV.

D 7686

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DO NOT SCALE

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

BY	DATE	APPROVED BY	DATE
DWN		E ENGR	
CHK		M ENGR	
		MFG ENGR	

MATERIAL

MODEL NO. 2260B/C
SEE ENGRG. SPECIFICATIONS
No.

FINISH

TOL. EX. AS NOTED
.XX ± FRAC ±
.XXX ± ANG. ± FINISH √

TITLE DISK/MUX CONTROLLER MOTHERBOARD

SCALE SHT 1 OF 3

210-7688 | WANG PART NUMBER | D | SIZE | 7688 | DRAWING NUMBER | C | REV.

NO.	REVISION	BY	DATE
A	ECN 7696	DEW	12-15-77

"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF, AND ARE PROPRIETARY TO, WANG LABORATORIES, INC.; THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."

DO NOT SCALE

C0-C7 (1D1)

50BS (2A7)

R4 (1G1)

R8 (1F11)

R5 (1G1)

R14 (1B11)

R15 (1C11)

T4 (2D6)

RA

10 MHZ

XTAL 10MHZ

JMPR

TP2

TP1

PRMS

SOBS (2A7)

REW (1G6)

BK1 (2E3)

BK3 (2E1)

BK5 (2C7)

CAPM (1E6)

+12V SIL.

+5VR

±0V

IMB (1G8)

SCM (1G9)

SRW (1G9)

T1-5 (1A4)

T4-6

T8 (1C11)

T4 (1E8)

T4 (1A7) (2D11) (1A2)

T4 (1C8)

ERROR (1G6)

WORD READY (1G10)

CNTRLG1 (1A6)

CNTRLG 3 (1A6)

CNTRLG2 (1A6)

BK1 (2B10)

TAB256 (1G6)

DISK SELECT

HEAD SELECT

DN3 (2A6)

DN3 (2E2)

BK6 (2F2)

BK5 (2F10)

OBSG (1G6)

SOBS (2F11) (2A11)

K0-K7 (1G10) (2C2)

K0-K7 (2F8)

M0-M7 (1G1)

RO-R7 (1G1)

BK4 (1C9)

BK6 (2B2)

RDG

WTG

ESG

WCD

DKSTB

RSTRB

WCDB

RB

IBS

HEAD SELECT (1G7)

TAB 256 (1G6)

SELECT 1

SELECT 2

DS

HS

EG

BK3 (2C10)

RG

TA1 J1

TA2 J1

TA4 J1

TA8 J1

TA16 J1

TA32 J1

TA64 J1

TA128 J2

IB1

IB2

IB3

IB4

IB5

IB6

IB7

IB8

RDDA

RCLK

8

REVISION	BY	DATE	NO.

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	S D	1-25-79	E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO. 2260B/C
SEE ENGRG. SPECIFICATIONS
No.

TITLE DISK/MUX CONTROLLER PRINTED BOARD

FINISH

TOL. EX. AS NOTED
XX ± FRAC. ±
XXX ± ANG. ± FINISH √

SCALE SHT 2 OF 3

210-7685 WANG PART NUMBER | D SIZE | 7688 DRAWING NUMBER | D REV

7688

"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF, AND ARE PROPRIETARY TO, WANG LABORATORIES, INC.; THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."

DO NOT SCALE

COMPONENT	WLI #	TYPE
C1	300-1150	150 pf 500V
C2	300-1913	.002 uf 500V
C3	300-1010	10 pf 500V
C4, 24, 25	300-4022	15 uf 20V (T)
C5, 8	300-1906	.001 uf 500V
C6, 7	300-4045	220 uf 15V (T)
C9	300-1903	.01 uf 25V
C10-23	300-1900	.05 uf 12V
XTAL1	321-0008	10 MHZ
R1,4-12, 35-38,43,46,48	330-2047	470Ω 1/4W 10%
R2,3,42,45,49-54	330-3022	2.2K 1/4W 10%
R13-20	330-2033	330Ω 1/4W 10%
R21,-30	330-2022	220Ω 1/4W 10%
R31	330-2018	180Ω 1/4W 10%
R32	330-3018	1.8K 1/4W 10%
R33	330-3047	4.7K 1/4W 10%
R34	330-4027	27K 1/4W 10%
R39	330-2010	100Ω 1/4W 10%
R40	330-3033	3.3K 1/4W 10%
R41	330-3015	1.5K 1/4W 10%
R44	330-5010	100K 1/4W 10%
R47	330-1047	47Ω 1/4W 10%
J1, 2	350-2097	50 PIN CONN.
J3	350-2096	36 PIN CONN.
J4	350-1029 M	72 PIN CONN.
J5	376-9024	16 PIN SKT.
Q1	375-1005	2N2222
D1,3	380-1001	SI4.
D2	380-2048	HNS230C 4.7V

LOCATION	W.L. PART NO.	TYPE
L1, 3, 6, 22	376-0338	74LS244
L2, 33	376-0194	7411
L4, 15, 44	376-0081	7408
L5, 17, 26, 31, 42	376-0010	7404
L7, 21, 47	376-0006	7474
L8, 13, 19, 25, 29	376-0093	7432
L9, 12	376-0028	7403
L10, 11	376-0138	74298
L14, 39	376-0049	74155
L16	376-0007	7476
L18	376-0102	74164
L20, 43, 45	376-0002	7400
L23, 24	376-0099	74181
L27, 32, 48-51	376-0048	74153
L28	376-0012	7451
L30	376-0096	9321
L34, 35, 37, 41	376-0005	7473
L36, 38	376-0082	74157
L40	376-0016	7402
L46	376-0240	LM339

CONN: 4

B	1	1024	2
R13	3	R12	4
WTG	5		6
	7	E36	8
C4	9	C0	10
C5	11	C1	12
C6	13	C2	14
C3	15	C7	16
RCLK	17	RDDA	18
	19		20
	21		22
	23	WCB	24
	25	R8	26
M0	27	M3	28
R0	29	R3	30
A0	31	M1	32
M2	33	R1	34
R2	35	A1	36
±0V	37	±0V	38
A4	39	A5	40
ADD	41		42
	43	RA	44
T01	45	T4	46
+5VR	47	+5VR	48
+5VR	49	+5VR	50
M4	51	M7	52
R4	53	R7	54
CRC	55	M5	56
M6	57	R5	58
R6	59	A2	60
A3	61	A6	62
A7	63	T4-6	64
AST	65		66
	67	T8	68
10 MHZ	69		70
+12V	71	-12V	72

LOCATION	TYPE	SPARES
L4	7408	1
L17	7404	2
L29	7432	1
L33	7411	2
L45	7400	1
L46	LM339	2
L47	7474	1

MNEMONIC	COORDINATE
A0-A7	1G7
ABUS_ABS	2C11
ADD	2A8
AST	1G8
C0-C7	1D1
CAPM	2A9
CNTRLG1	1A5
CP86	1G5
CRC	1G6
D3	2E1
DRSTB	2C1
E6	2E1
E36	2G2
FE	1B1
FR	1G9
H3	2E1
I81-I88	2B1
I83	2F1
IM	2G6
KD	1B1
LAE	2G5
LOADAUX	1A8
M0-M7	1G2
M3	1A10
OB-OB8	2A9
OBS	2A8
P6	1A1
PRMS	2B11
PUP	1B1
R0-R7	1G3
R8	1F11
R9	1E11
R10	1A4
R11,12	1C11
R13,14,15	1B11
RA	2D11
R8	2E1
RCLK	2A5
RDAT	2G6
RDDA	2A5
RF6	2A3
RSRD	2G6
RSTRB	2A6
RT	1B1
RTD	1B1
SELECT	2E1
SELECT1	2E1
SIZE	2G5
SM	2G6
TOT	2A6
T4	2A6
T4-6	2A6
T8	2A6
TA-2,3,8	2E1
WCB	2G2
WCD0	2G1
WCD1	2A9
WTC	2G5
WTG	2G2
8	2A5
1024	1A7
10MHZ	2D11

LOCATION	MNEMONIC	COORDINATE
J1	IM	2A6
	TA16	2A6
	TA64	2A6
	TA32	2A6
	TA2	2A6
	LAE	2E1
	FR	2G2
	TA1	2A6
	TA8	2A6
	TA4	2A6
	TA256	2A6
	RSRW	2A6
	SIZE	2G5
	WTCK	2G2
	RG	2A6
	RDAT	2A5
	SM	2G6
	RCLK	2A5
	WCDB	2G1
J2	SELECT2	2E1
	SELECT1	2E1
	P6	1A1
	WG	2G2
	RSTRB	2A6
	DRSTB	2G1
	D3	2E1
	TA32	2A6
	H3	2E1
J3	IOV	
	CP86	1G5
	ABS	2A8
	OB6	2A8
	OB7	2A8
	OB4	2A8
	OB5	2A8
	OB3	2A8
	OB2	2A8
	OB1	2A8
	OB8	2A8
	IB7	2A5
	IB6	2A5
	IB5	2A5
	IB4	2A5
	IB3	2A5
	IB2	2A5
	IB1	2A5
	IB8	2A5
J5	PUP	1B1
	KD	1B1
	R10	1A4
	R14	1B11
	R13	1B11
	CAPM	2A9
	CNTRLG1	1A5
	FE	2E1
	R11	1C11
	R6	1G3
	RT	1B1
	ROG	1A4

E-REV 0

REVISION	BY	DATE
ORIGINATED PER DWG # 5523 APPD # 5524	SD	1-26-79

BY	DATE	APPROVED BY	DATE
DWN SD	1-26-79	E ENGR DOOLEY	3-12-79
CHK G.D.	3-12-79	M ENGR	
		MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL	MODEL NO. 2260 B/C SEE ENGRG. SPECIFICATIONS No.	TITLE DISK/MUX CONTROLER MOTHERBOARD		
FINISH	TOL. EX. AS NOTED .XX ± FRAC. ± .XXX ± ANG. ± FINISH √	210-7688	D	7688	0
	SCALE 1/1 SHT 3 OF 3	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.

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DO NOT SCALE

NOTES:
1. SOLDER DRAIN WIRE TO ITEM #7
2. ASSEMBLE WIRES PER CHART.
3. PRINTER LABEL NOT USED ON 220-0105-2, 220-0105-3, 220-0167
4. ON 220-0105-3 SPLIT EXISTING WIRE INTO TWO EQUAL BRAIDS, TIN, THEN SOLDER TO GROUND STRAPS

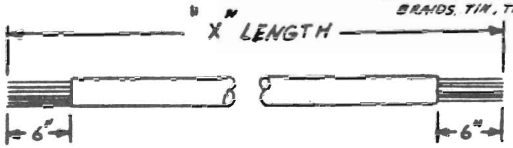
DRILLED OR PUNCHED HOLE TOLERANCES:

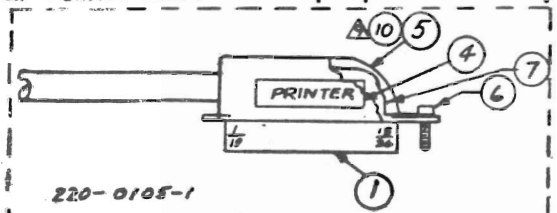
HOLE DIA.	TOL.
.0135 to .125	±.002
.126 to .250	±.003
.251 to .500	±.005

IDENT.	DESCRIPTION	QTY.
A		

DETAIL "A"

CONNECTOR (350-2082) ('WIRING SIDE')



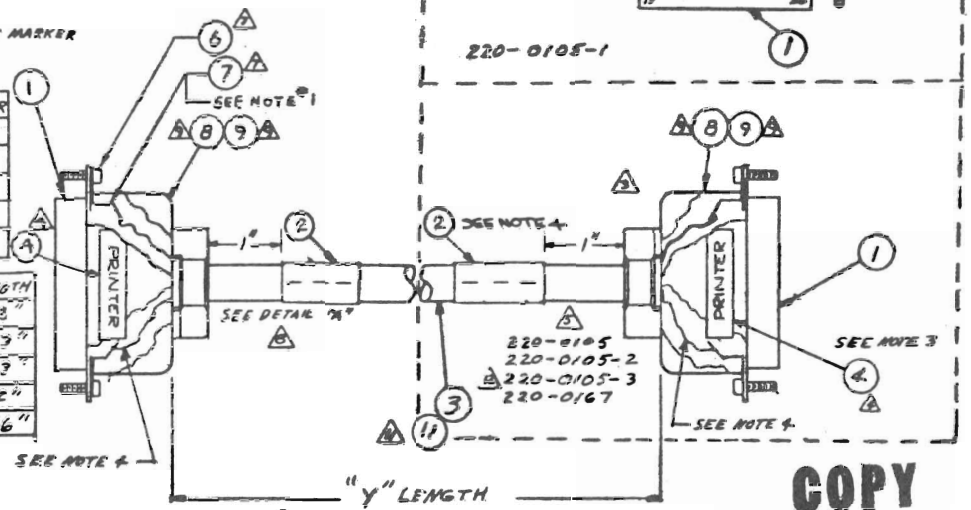


CONN. PIN NO.	WIRE COLOR	TWISTED PAIR	SIGNAL NAME	CONN. PIN NO.
1 / 19	RED GRN	PAIR	OTR SIDE	1 / 19
2 / 20	RED BRN	PAIR	DATA 1	2 / 20
3 / 21	RED GRY	PAIR	DATA 2	3 / 21
4 / 22	RED ORN	PAIR	DATA 3	4 / 22
5 / 23	RED BLU	PAIR	DATA 4	5 / 23
6 / 24	ORN WHT	PAIR	DATA 5	6 / 24
7 / 25	ORN YEL	PAIR	DATA 6	7 / 25
8 / 26	ORN BLK	PAIR	DATA 7	8 / 26
9 / 27	GRN YEL	PAIR	DATA 8	9 / 27
10 / 28	GRN WHT	PAIR	ACKNLG	10 / 28
11 / 29	GRN BLK	PAIR	BUSY	11 / 29
12 / 30	BLU YEL	PAIR	——	12 / 30
13 / 31	BLU BLK	PAIR	RESET	13 / 31
14 / 32	BLU WHT	PAIR	——	14 / 32
15 / 33	BRN WHT	PAIR	——	15 / 33
16 / 34	BRN BLK	PAIR	+5V	16 / 34
17 / 35	GRY WHT	PAIR	CHA. GND	17 / 35
18 / 36	GRY BLK	PAIR	+5V	18 / 36

NOTE:
4. ONLY HEATSHRINK SLEEVE MARKER 606-0167 USED ON THIS END

ASSY	SLEEVE MARKER
220-0105	606-0105
220-0105-1	606-0105-1
220-0105-2	606-0105-2
220-0105-3	606-0105-3
220-0167	606-0167

W.L. PART NO	"X" LENGTH	"Y" LENGTH
220-0105	13'±3"	12'±3"
220-0105-1	13'±3"	12'±3"
220-0105-2	13'±3"	12'±3"
220-0105-3	7'±2"	6'±2"
220-0167	51'±6"	50'±6"



COPY
JUL 20 1979
JUL 20 1979

220-0105-3	220-0105-2	220-0167	220-0105-1	WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
5FT	13FT			420-0059	11		CABLE 18 TP SHIELDED		
1	1	1	1	350-4231-G	10		90° STRAIN RELIEF COVER 36 POS.		GROOVE HALF
2	2	2	1	350-4233-T	9	2	180° STRAIN RELIEF COVER 36 POS.		TONGUE HALF
2	2	2	1	350-4233-G	8	2	180° STRAIN RELIEF COVER 36 POS.		GROOVE HALF
4	2	2	2	458-0361	7	2	GROUND STRAP		CGB15-28
4	4	4	3	350-4234	6	4	CAPTIVE SCREW		AMP
			1	350-4231-T	5		90° STRAIN RELIEF COVER		TONGUE GROOVE
			2	615-1297	4	2	PRINTER CONN. LABEL		
5FT	13FT		3	420-0058	3	13FT	CABLE SHIELDED		26 G, 36 COND. T.P.
			1	SEE CHART	2	1	HEATSHRINK MARKER		1/2" DIA.
			2	350-2082	1	2	36 POS. PLUG ASSY.		AMP

REVISION	BY	DATE	APPROVED BY	DATE
1 REV PER ECN# 3912 11-14-73				
2 REV PER ECN# 4105 4-1-74				
3 REV. PER ECN# 4737 MRA 8-1-75				
4 REV PER ECN 5362 DRC 4/17/76				
5 REV. PER ECN# 5603 JMS 8-18-76				
6 REV PER ECN# 5864 LMH 11-5-76				
7 REV. PER ECN# 6147 PWS 3/24/77				
8 REV. PER ECN# 6263 JMS 7-11-77				
9 REVISED PER ECN# 6519 APPROVED 5-2-78				
10 REV PER ECN# 6519 JMS 5-9-78				
11 REV PER ECN# 6519 JMS 5-9-78				
12 REV PER ECN# 6519 JMS 5-9-78				
13 REV PER ECN# 6939 8-8-78				
14 REV PER ECN# 6936 8-10-78				
15 REV PER ECN# 6939 8-8-78				
16 REV PER ECN# 6939 8-8-78				

WANG PART NO	FIRST USED ON	ASSY USED ON
-		

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL:

FINISH:

MODEL NO 2221

SEE ENGRG SPECIFICATIONS No.

TOL. EX AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG. ± 1° RF FINISH 125

SCALE NONE | SHT 1 OF 1

BY	DATE	APPROVED BY	DATE
DWN F.E. SOUSA	4-25-78	E ENGR.	4-26-78
CHK G.D.	5-11-78	M ENGR.	
E.C. CONTROL		MFG ENGR.	

TITLE: LINE PRINTER CABLE

SEE CHART	C	6422-129	16
WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.

621-2260 D

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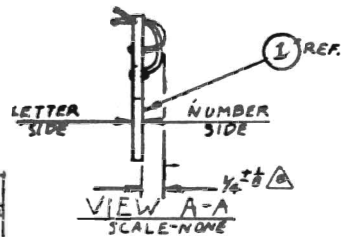
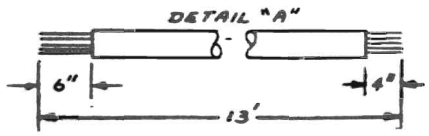
DO NOT SCALE



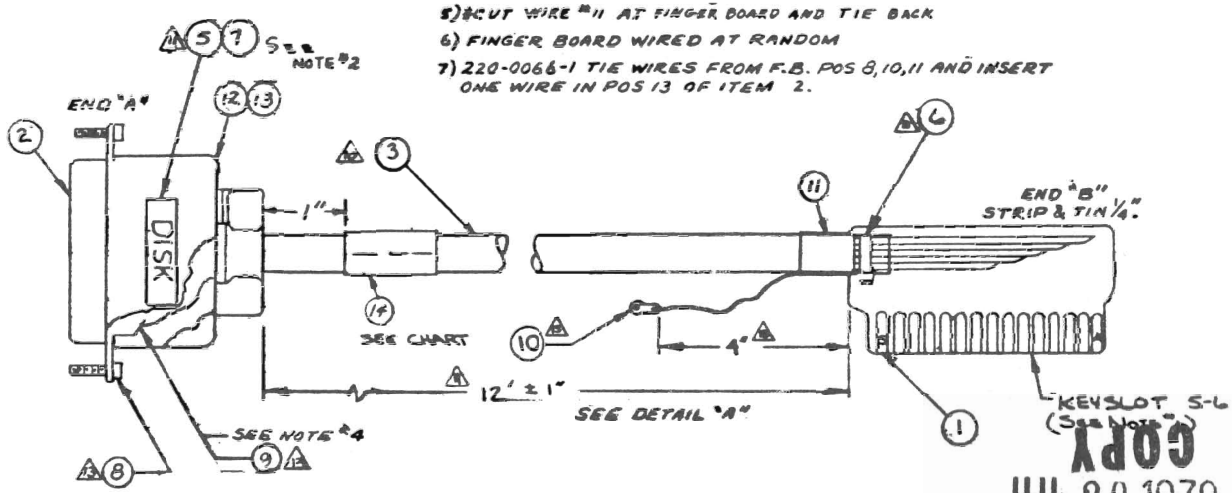


HOLE LEGEND		
	HOLE DIA.	TOL.
DRILLED OR PUNCHED HOLE TOLERANCES:	.0135 to .125	± .005
	.126 to .250	± .007
	.251 to .500	± .010

SYMBOL	DESCRIPTION	QTY
A		

Notes:

1) KEYSLOT BETWEEN 5 & 6 NEEDED ON 220-0066-3, 220-0066-4 ONLY
2) ITEM #5 LABEL USED ON 220-0066 & 220-0066-4; 220-0066-3 ONLY, ITEM #7 LABEL USED ON 220-0066-2 ONLY.
3) XX ADD JUMPERS BETWEEN POSITIONS 8,10,11 & 13 ON FINGER BOARD 5223C FOR 220-0066-1 ONLY.
4) SOLDER DRAIN WIRE TO ITEM 9.
5) CUT WIRE #11 AT FINGER BOARD AND TIE BACK
6) FINGER BOARD WIRED AT RANDOM
7) 220-0066-1 TIE WIRES FROM F.B. POS 8,10,11 AND INSERT ONE WIRE IN POS 13 OF ITEM 2.



WIRING RUN LIST

5223 FINGER BOARD		220-0066 2230/2260 2240/2242 2243 350-2067	220-0066-1 630/730 640/740 350-2067	220-0066-2 2209 350-2067	220-0066-3 WCS 350-2067	220-0066-4 2210/2270A 350-2067
1		6	7	6	6	6
2		7	6	7	7	7
3		1	1	1	1	1
4		3	3	3	3	3
5		5	5	5	5	5
6		2	2	2	2	2
7		4	4	4	4	4
8		9	XX 13	9	9	9
9		12	12	16	12	12
10		11	XX 13	19	11	11
11		#	XX 13	11	18	18 #
12		36	36	36	36	36
13		33	33	33	33	33
14		34	34	34	34	34
15		35	35	35	35	35
A		8	8	8	8	8
B		20	20	20	20	20
C		21	21	21	21	21
D		22	22	22	22	22
E		23	23	23	23	23
F		24	24	24	24	24
H		25	25	25	25	25
J		26	26	26	26	26
K		10	10	10	10	10
L		31	31	31	31	31
M		32	32	32	32	32
N		30	30	30	30	30
P		27	27	27	27	27
R		28	28	#	28	28
S		29	29	#	15	15

CHART

CABLE NO.	HEATSHRINK MARKER No.
220-0066	606-0066
220-0066-1	606-0066-1
220-0066-2	606-0066-2
220-0066-3	606-0066-3
220-0066-4	606-0066-4

WANG PART NO.	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
SEE CHART	14	1	HEATSHRINK MARKER		3/16" DIA
350-4228-G	13	1	180° STRAIN RELIEF COVER		36 POS GROOVE HALF
350-4228-T	12	1	180° STRAIN RELIEF COVER		36 POS TONGUE HALF
605-0132	11	A/R	HEATSHRINK TUBING		3/8" CLEAR 1 1/4" LONG
654-1006	10	1	GROUND LUG		#6
158-0361	9	1	GROUND STRAP		C6815-28
350-4234	8	2	CAPTIVE SCREW		4-40 X 3/8
615-1293-50	7	P/L	2250 CONN. LABEL		
605-1004	6	1	TY-RAP		
615-1298	5	P/L	DISK CONN. LABEL		
420-0055	3	A/R	CABLE 30 CONDUCTOR		#26 GA. SHIELDED
350-2082	2	1	36 POS. PLUG ASSY.		SCREW MT.
570-5223C	1	1	30PIN FINGER BOARD		

FIRST USED ON	ASSY USED ON
1 H-0935	

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL: //

FINISH: //

MODEL NO. DISKS

SEE ENGRG SPECIFICATIONS No. ES-1 3

TOL. EX. AS NOTED XX ± .010 FRAC. ± 1/64 XXX ± .005 ANG. ± 1° 30' FINISH 125

SCALE N.T.S. SHT 1 OF 1

BY	DATE	APPROVED BY	DATE
DWN P.D.G.	11/22/71	E ENGR	
CHK		M ENGR	
E C CONTROL		MFG ENGR O.K.	3/25/72

TITLE I.O. CABLE ASSY. (WANG 2156 C-ES-14-0866-3)

SEE CHART	C	6472-61	-
WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

6472-61 C

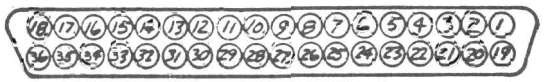
REV	DESCRIPTION	BY	DATE
14	REVISED PER IPLB RFA#0744		3-25-74
5	REVISED PER R.F.A. # 0847. APP'D		4/5/74
6	REVISED PER RFA#0959 & IRB 5-24-74		5-28-74
7	REV. PER ECN#4935 6-10-74		6/24/74
8	REV. PER ECN#4937 MARK 18-1.75		7/11/74
9	REV PER ECN # 5091 AAB 10/10/75		
10	REV. PER ECN#5402 BT. 4/3/76		
11	REV. PER ECN#5754 BLT 11/21/76		
12	REV. PER ECN#5907 PLOT 3/22/77		
13	REV PER ECN#5397 APP'D		4/11/77
14	REVISED PER ECN#6089 APP'D		9/1/77
15	REV. PER ECN#6169 AAB 8-8-78		8/10/78
16	REV PER ECN#6099 APP'D		8/31/78
17			

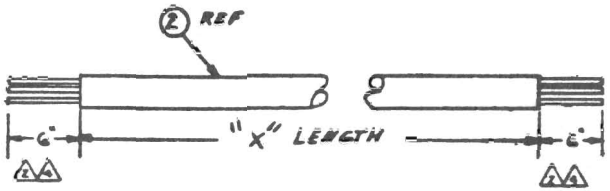
COPY JUL 20 1979

E-74

DO NOT SCALE

AR VIEW (WIRE SIDE) CONNECTOR ITEM°1





LEGEND

DRILLED OR PUNCHED HOLE TOLERANCES:	HOLE DIA.	TOL.
	.0125 to .125	±.003 ±.002
	.126 to .250	±.003 ±.002
	.251 to .500	±.003 ±.001

SYMBOL	DESCRIPTION	QTY.
A		

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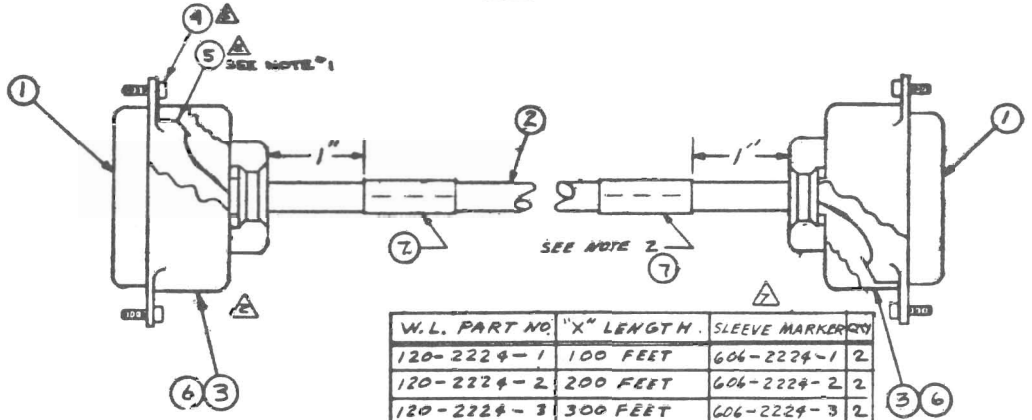

FROM CONN. No. ITEM°1	WIRE No.	TO CONN. No. ITEM°1
PIN 1	1	PIN 1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
13	13	13
14	14	14
15	15	15
16	16	16
17	17	17
PIN 18	18	PIN 18

FROM CONN. No. ITEM°1	WIRE No.	TO CONN. No. ITEM°1
PIN 19	19	PIN 19
20	20	20
21	21	21
22	22	22
23	23	23
24	24	24
25	25	25
26	26	26
27	27	27
28	28	28
29	29	29
30	30	30
31	31	31
32	32	32
33	33	33
34	34	34
35	35	35
PIN 36	36	PIN 36

W.L. PART NO.	"X" LENGTH	SLEEVE MARKER	QTY
120-2224-1	100 FEET	606-2224-1	2
120-2224-2	200 FEET	606-2224-2	2
120-2224-3	300 FEET	606-2224-3	2
120-2224-4	400 FEET	606-2224-4	2
120-2224-5	500 FEET	606-2224-5	2
220-0138	12 FEET	606-0138	1

NOTE:
1. SOLDER DRAIN WIRE TO ITEM°8
2. APPLY HEATSHRINK MARKER FOR CABLE 220-0138 ON THIS END.

COPY
JUL 20 1979

WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
SEE CHART	7	N/R	HEATSHRINK MARKER		3/8" DIA.
350-4228-G	6	2	180° STRAIN RELIEF COVER		GROOVE HALF
458-0361	5	2	GROUND STRAP		C6815-28
350-4234	4	4	CAPTIVE SCREW		AMP.
350-4228-T	3	2	180° STRAIN RELIEF COVER		TONGUE HALF
420-0054	2	N/R	CABLE (SHIELDED)		#26 GAUGE 36 CONDUCTOR
350-2082	1	2	36 POS. PLUG ASSY. (MALE)		AMP

REV	BY / DATE	DESCRIPTION	ECN	CHK	ENGR	M ENGR	MFG ENGR
1	PEARA 7-5-74	REVISED PER ECN #1054	4-30-74				
2	MRM 7-29-75	REV. PER ECN #4737	7-29-75				
3	LARRY T. 11-20-75	REV. PER ECN 1866	11-20-75				
4	LET 4-5-76	REV PER ECN 5402	4-5-76				
5	PWS. 3/4/77	REV. PER ECN #607	3/4/77				
6	8-2-78	REVISED PER ECN #9129 ADDED	8-2-78				
7	8-8-78	PER ECN #9129	8-8-78				
8	8-16-78	PER ECN #9129	8-16-78				

Qty Per Unit	FIRST USED ON	ASSY USED ON

WANG LABORATORIES, INC. TEWKSBURY MASS. U.S.A.

BY	DATE	APPROVED BY	DATE
DWN 28	9/8/74	E ENGR	
CHK		M ENGR	
E C CONTROL		MFG ENGR D.L.	9-11-74

MATERIAL: //

MODEL NO 6482

SEE ENGRG SPECIFICATIONS No ES-1001

FINISH: //

TOL EX AS NOTED .XX ± .010 FRAC ± 1/64 .XXX ± .005 ANG ± 1°30' FINISH √

SCALE NONE SHT 1 OF 1

TITLE: 2224 EXTENSION CABLE

SEE CHART	C	6482-16	B
WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

91-2849 D

F-75

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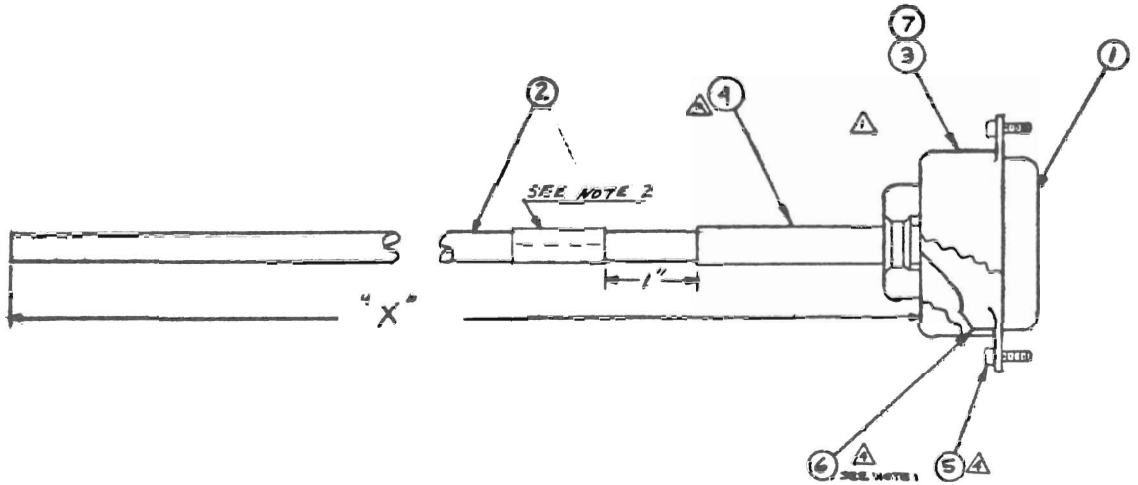
DO NOT SCALE

HOLE LEGEND		
DRILLED OR PUNCHED HOLE TOLERANCES:	HOLE DIA.	TOL.
	.0135 to .125	± .003 — .001
	.126 to .250	± .004 — .001
	.251 to .500	± .005 — .001

IDENT.	DESCRIPTION	QTY
A		



SIGNAL	CABLE WIRE NO.	CONN. PIN NO.
DATA 1	1	2
DATA 2	2	3
DATA 3	3	4
DATA 4	4	5
DATA 5	5	6
DATA 6	6	7
DATA 7	7	8
DATA 8	8	9
BUSY	9	11
ACKNLG	10	10
DATA STBE	11	1
I OV	12	16
CH. GND	13	17
+5VR	14	18
RESET	15	31

SLEEVE MARKER	W. L. PART NO.	1X" LENGTH	TOL.	
606-0130	220-0130	13 FT	± 1"	3
606-0131	220-0131	9 FT	± 1"	3

NOTE:
1. SOLDER DRAIN WIRE TO ITEM 6.
2. APPLY HEATSHRINK MARKER APPROX WHERE SHOWN (1 PER CABLE)

COPY

JUL 20 1979

	WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
6				HEATSHRINK MARKER		3/8" DIA
	350-4228-G	7	1	180° STRAIN RELIEF COVER 36 POS		GROOVE HALF
4 1	158-0361	6	1	GROUND STRAP		CGB15-28
4 1	350-4234	5	2	CAPTIVE SCREW		AMP
4 1	350-4105	4	1	BUSHING		#3
4 1	350-4228-T	3	1	180° STRAIN RELIEF COVER 36 POS.		TONGUE HALF
4	420-0068	2	A/R	CABLE (15 COND) SHIELDED		26 GAUGE
4 3 1	350-2082	1	1	36 POS. PLUG ASSY SCREW MT		AMP 552470-1

REV	FIRST USED ON	REVISION
1	[illegible]	[illegible]
2	[illegible]	[illegible]
3	6647	[illegible]
4	6647	[illegible]

REVISION	BY	DATE
REVISED PER ECN# 4937 MRM 8-4-75	[illegible]	[illegible]
REVISED PER ECN# 5193 AND D.C.O. [illegible]	[illegible]	[illegible]
REV. PER ECN# 5682 - B.T. 4/7/76	[illegible]	[illegible]
REVISED PER ECN# 6907 [illegible]	[illegible]	3/24/77
REVISED PER ECN# 8484 AND D.C.O. [illegible]	[illegible]	9/12/78
[illegible]	[illegible]	10-8-78

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

BY	DATE	APPROVED BY	DATE
DWN [illegible]	4/7/76	E ENGR	
CHK		M ENGR	
E C CONTROL		MFG ENGR [illegible]	[illegible]

MATERIAL

MODEL NO 2221 M

SEE ENGRG SPECIFICATIONS No ES-1001

FINISH

TOL EX AS NOTED XX ± .010 FRAC. ± 1/64 XXX ± .005 ANG. ± 1°30' FINISH √

TITLE CP & PRINTER CABLE

SCALE | SHT 1 OF 1 | SEE CHART | C | [illegible]-55 | 6

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

55-2897 D

F-76

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MILLIMETERS IN PARENTHESIS. TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

DO NOT SCALE

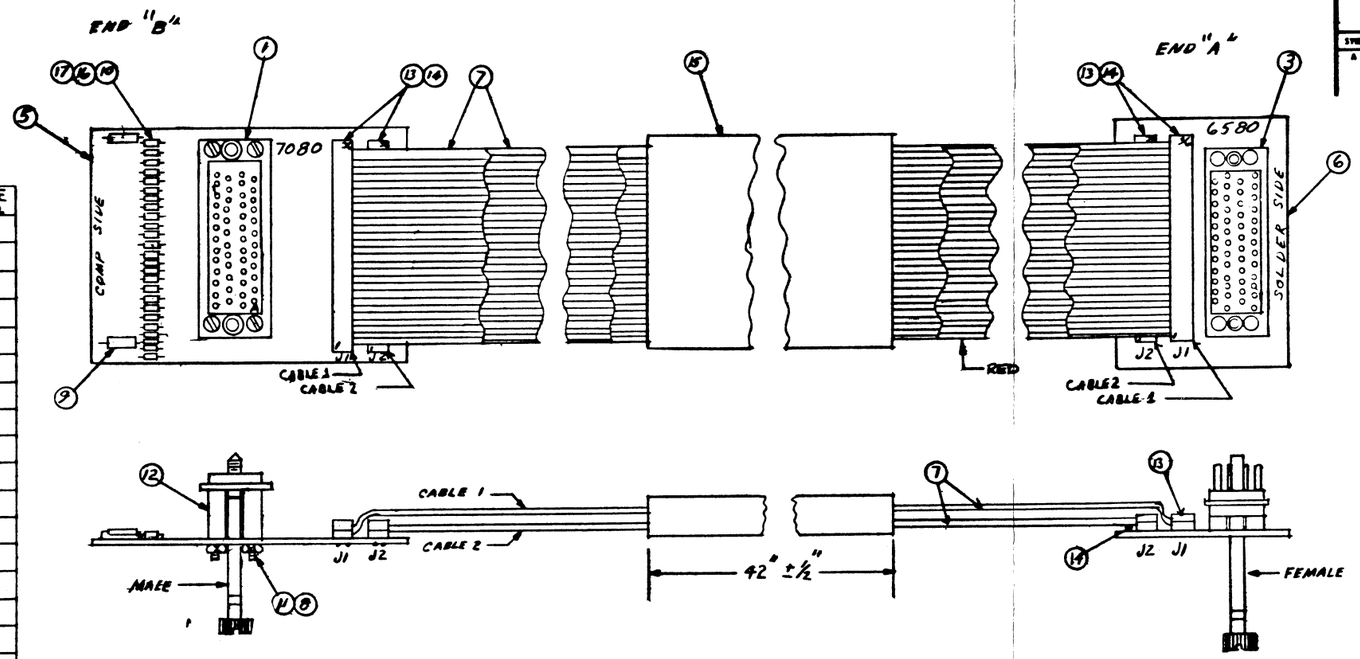
HOLE LEGEND & TOLERANCES	
HOLE DIA	TOLERANCE
.025 - .125	+ .003 - .001
.126 - .250	+ .004 - .001
.251 - .500	+ .005 - .001

SYM.	DESCRIPTION	QTY
A		

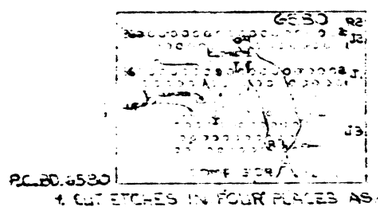
CONN. FEMALE PIN NO.			SIGNAL NAME	CONN. MALE PIN NO.
A			READ CLK	A
B			±0V	B
C			WRITE DATA	C
D			±0V	D
E			READ DATA	E
F			±0V	F
			±0V	
H			RFS	H
J			±0V	J
K			TA2	K
L			±0V	L
M			ORIGE CURR	M
N			±0V	N
P			SEL 0	P
R			±0V	R
S			TA0	S
T			±0V	T
U			SEL 1	U
V			±0V	V
W			TA3	W
X			±0V	X
Y			FAN	Y
Z			±0V	Z
a			SEL 2	a
b			±0V	b
c			SPB	c
d			±0V	d
e			TA4	e
f			±0V	f
h			ULH	h
j			±0V	j
k			TA5	k
m			±0V	m

CONN FEMALE PIN NO.			SIGNAL NAME	CONN. MALE PIN NO.
C			SECTOR BIT 1	C
E			±0V	E
F			WRITE GATE	F
H			±0V	H
J			TA4	J
L			±0V	L
M			WCLK	M
P			±0V	P
R			SECTOR BIT 2	R
S			±0V	S
U			SECTOR BIT 4	U
V			±0V	V
W			TA6	W
Y			±0V	Y
a			SECTOR BIT 8	a
b			±0V	b
d			ADDR ACK	d
e			±0V	e
f			TA1	f
h			±0V	h
j			050	j
k			±0V	k
m			51E	m
n			±0V	n
p			SECTOR BIT 16	p
r			±0V	r
s			RST	s
t			±0V	t
u			LAT	u
v			±0V	v
w			50B	w
y			±0V	y
AA			TA7	AA
BB			±0V	BB
CC			4.3V	CC
			±0V	

▲ INDICATES TIED TO GROUND BUSS, GROUND BUSS TIED TO PINS 3, X, M, CC
BAR, — UNDER LETTER INDICATES LOWER CASE.

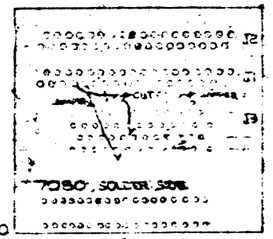


NOTES:
1) ADD BUSS JUMPER IN LOCATION JP AS NOTED ON ITEMS 5 & 6
2. CABLE 1 IS 55½" ± ½" (J1)
   CABLE 2 IS 94½" ± ½" (J2)
3. TRIM LAST CONDUCTOR OF BOTH CABLES ON END "A" CUT BACK 1½" AND OFFSET CABLES STARTING WITH PIN 2.



P.C.BD. 6580

1. CUT ETCHES IN FOUR PLACES AS SHOWN.
2. CONNECT WIRE FROM J3 PIN R TO TE PIN 10 FROM J3 PIN L TO TE PIN, FROM J3 PIN E TO PLATE THRU ABOVE J1, PINS 34 & 35.
3. WIRE #24 GAGE YELLOW TEFLON.



P.C.BD. 7080

1) CUT ETCH AS SHOWN.
2) CONN. WIRE FROM J3-V TO J1-PIN 7.

QTY.	ITEM	WANG PART NO.	DRAWING NO.	DESCRIPTION
2	17	330-2056		360 OHM ¼ W 10% .4 RESISTOR
2	16	330-2022		220 OHM ¼ W 10% .4 RESISTOR
A/R	15	605-0133		CABLE JACKET FLAT 3.5" WIDE
4	14	350-0401C		36 PIN FLAT CABLE CONN. COVER #3378
4	13	350-0401B		36 PIN FLAT CABLE CONN. BOTTOM #3378
4	12	462-0200		SPACER ¼ RDX ½ LG
4	11	652-2001		#4-40 HEX NUT NYLON
20	10	330-2010		100 OHM ¼W 10% R RESISTOR
2	9	300-4022		15 UF 20V 10% TANT CAPACITOR
4	8	650-2283		SCR #4-40 x 7/8 FILL HD.
A/R	7	420-0043		CABLE 36 CONDUCTOR FLAT (3M3409)
1	6	510-6580		P.C. BOARD 6580
1	5	510-7080		P.C. BOARD 7080
ED	4			
1	3	350-2080		CONN. 50 POS. (MALE)
ED	2			
1	1	350-2057		CONN. 50 POS. (FEMALE)

NEXT ASSY.

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	J B	7/14/77	E ENGR	
CHK			M ENGR	
	QTY/1		MFG ENGR	12/4/78

MATERIAL —

MODEL NO. 2260
SEE ENGRG SPECIFICATIONS No. ES-1001

TITLE: INTER DISC CABLE ASS'Y

FINISH —

TOL. EX. AS NOTED
XX ±.01 FRAC. ±1/64
XXX ±.005 ANG. ± 1° FINISH 63

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
220-0151	D	6482-112	6

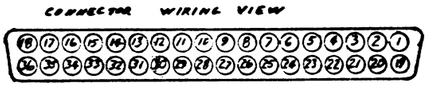
SCALE — SHT OF

REVISIONS						
1	REDRAWN (NSA) PER ECN # 7181 W.OTEY	G.D.	6-2-78	G.D.	6-5-78	
2	REV PER ECO # 7644 MLB 10-27-77					
3	REV PER ECO #8273 MLB 3-1-78					
4	REV PER ECO #8503 MLB 4-14-78					
5	REV PER ECO #9356 MLB 8-11-78					
6	REV PER ECO #9940 MLB 11/10/78					

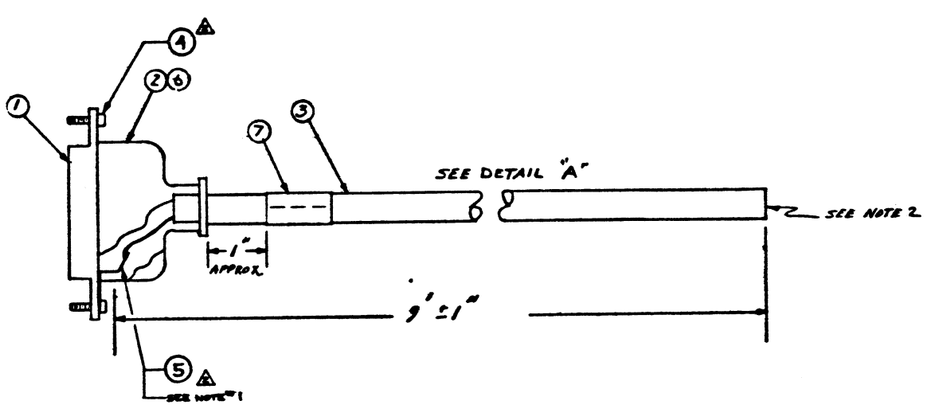
COPY

JUL 20 1979

CONNECTOR WIRING VIEW

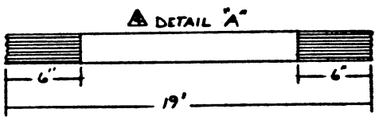


	CONN PIN. NO.	WIRE COLOR	TWISTED PAIR	SIGNAL NAME	P.C. BD 7091
	1 19	RED GRN	PAIR	DATA STROBE IOV	12 13
	2 20	RED BRN	PAIR	DATA 1 IOV	7 18
	3 21	RED GRY	PAIR	DATA 2 IOV	8 17
	4 22	RED ORN	PAIR	DATA 3 IOV	4 21
	5 23	RED BLU	PAIR	DATA 4 IOV	3 22
	6 24	ORN WHT	PAIR	DATA 5 IOV	5 20
	7 25	ORN BLK	PAIR	DATA 6 IOV	6 19
	8 26	GRN WHT	PAIR	DATA 7 IOV	2 23
	9 27	BLU BLK	PAIR	DATA 8 IOV	1 24
	10 28	BLU WHT	PAIR	ACK IOV	9 16
⚠1	11	BRN	*	BSY	10
	12 30	— —	—	— —	— —
	13 31	GRY WHT	PAIR	IOV PRIME	14 11
	14 32	— —	—	— —	— —
	15 33	— —	—	— —	— —
	16 34	— —	—	— —	— —
	17 35	— —	—	— —	— —
⚠1	18 36	WHT	*	+5V	+5V BIAS



NOTES:
⚠1. SOLDER DRAIN WIRE TO ITEM 5.
⚠2. CUT AFTER Q.C. TEST.

⚠ DETAIL "A"



COPY
JUL 20 1979

WANG PART NO	ITEM	QTY.	NAME	MATERIAL	DESCRIPTION
606-0156	7	1	HEATSHRINK MARKER		3/8" DIA
350-4228-G	6	1	COVER STRAIN RELIEF 180°		GROOVE HALF
⚠2 158-0361	5	1	GROUND STRAP		C4B5-28
⚠2 360-4234	4	2	CAPTIVE SCREW		AMP
420-0049	3	N/R	CABLE SHIELDED		12 TWISTED PAIR 26 GAUGE
350-4228-T	2	1	COVER STRAIN RELIEF 180°		TONGUE HALF
⚠2 350-2082	1	1	CONNECTOR 36 POS		AMP

REVISION	BY	DATE	APPROVED BY	DATE
ORIG. PUB. PER ECN L180				
REV. PER ECN L180 J.REQUIERS TC-15-2L	DAN	4/17/71		
REVISED PER ECN M407 REV PER ECN M407	DAN	5/21/71		
REVISED PER ECN M806 AND ECO 6284	DAN	10/18/71		
PER ECN M806 AMP ID: 350-4228-G	DAN	4/4/72		
REVISED PER ECN M2427 AS A-6-78	DAN	6/8/78		

	FIRST USED ON	ASSY USED ON
Qty. Per Unit		

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL

MODEL NO 2251

SEE ENGRG SPECIFICATION(S) No.

FINISH

TOL EX AS NOTED
XX ± .010 FRAC ± 1/64 1IN
XXX ± .005 ANG ± 1°30' FINISH √

SCALE — SHT 1 OF

	BY	DATE
DWN	[illegible]	7/11/72
CHK		
E C CONTROL		
E ENGR		
M ENGR		
MFG ENGR	B.J.	11/15/72

TITLE I/O CABLE ASS'Y (2251)

WANG PART NUMBER	SIZE	DWG NUMBER	REV
220-0156	C	6482-135	5

SCI-6847 D

DO NOT SCALE

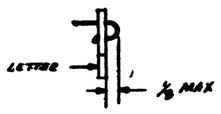
CONN. 350-2082

REAR VIEW

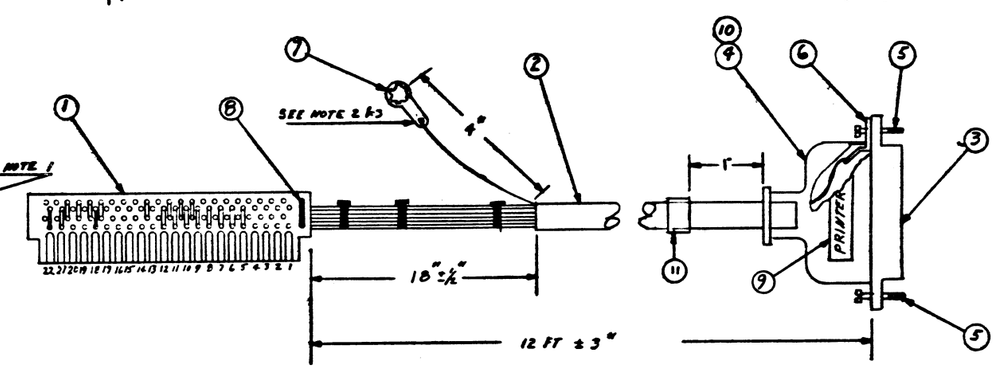
LEGEND

DRILLED OR PUNCHED HOLE TOLERANCES:	HOLE DIA.	TOL.
	.0135 to .125	±.003
	.126 to .350	±.004
	.351 to .500	±.005

IDENT.	DESCRIPTION	REV.
A		



CONN. PIN NO.	WIRE COLOR	TWISTED PAIR	SIGNAL NAME	PC. BD. 6703
1	RED	PAIR	DTA STBE	9
19	GRN		±0V	10
2	RED	PAIR	DATA1	K
20	BRN		±0V	12
3	RED	PAIR	DATA2	L
21	GRY		±0V	P
4	RED	PAIR	DATA3	M
22	ORN		±0V	R
5	RED	PAIR	DATA4	N
23	BLU		±0V	S
6	ORN	PAIR	DATA5	5
24	WHT		±0V	T
7	ORN	PAIR	DATA6	6
25	YEL		±0V	U
8	ORN	PAIR	DATA7	7
26	BLK		±0V	V
9	GRN	PAIR	DATA8	8
27	YEL		±0V	W
10	GRN	PAIR	ACKNLG	22
28	WHT		±0V	X
11	GRN	PAIR	BUSY	21
29	BLK		±0V	19
12	BLU	PAIR	—	
30	YEL			
13	BLU	PAIR	SELECT	1
31	BLK		PRIME	F
14	BLU	PAIR	—	
32	WHT			
15	BRN	PAIR	—	
33	WHT			
16	BRN	PAIR	±0V	20
34	BLK		—	
17	GRY	PAIR	CH GND	
35	WHT		—	
18	GRY	PAIR	+5V	4
36	BLK			



NOTE:

1. BUSS FINGERS 10, 12, 19, 20, P, R, S, T, U, V, W AND X TOGETHER ON FINGER BOARD 6703
2. SOLDER ITEMS 6 AND 7 TO DRAIN WIRE
3. TIN DRAIN WIRE FULL LENGTH

COPY

JUL 20 1979

6061-0161	11	1	HEATSHRINK MARKER		.12" DIA.
350-4233-G	10	1	STRAIN RELIEF COVER 180°		GROOVE HALF
660-0203		A/R	SOLDER		SN63-37
615-1297	9	1	PRINTER CONN. LABEL		A5300-1072
605-1004	8	5	TYRAP		
654-1006	7	1	GROUND LUG		#6
458-0361	6	1	GROUND STRAP		C6815-28
350-4234	5	2	SCREW CAPTIVE		
350-4233-T	4	1	STRAIN RELIEF COVER 180°		TONGUE HALF
350-2082	3	1	CONNECTOR 36MOS (MALE)		
420-0058	2	4/R	CABLE 36 CONDUCTOR T.P. SHIELDED		
510-6703	1	1	P.C. BOARD 6703		
WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION

QTY PER UNIT	FIRST USED ON	ASSY USED ON

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL	MODEL NO 2281		BY	DATE	APPROVED BY	DATE
	SEE ENGRG SPECIFICATIONS No	DWN	7-8-77	E ENGR	
FINISH	TOL EX AS NOTED .XX ± .010 FRAC ± 1/64 .XXX ± .005 ANG. ± 1°30' FINISH 125	CHK		M ENGR	
	SCALE — SHT 1 OF 1	E C CONTROL		MFG ENGR	6/6/79
		TITLE I/O CABLE 2281			
		220-0161	C	6482-143	5
		WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

E81-2869 C

NO	REVISION	BY	DATE	CHK'D	APP'D
0	ORIG. RELEASE	ZW	7/7/77	MH	7/8/77
1	REV PER ECN# 7012 T.R.P. 9-16-77	RW	9-16-77	MH	9-16-77
2	REV PER ECN# 7911 TRP 12-30-77	TRP	12-30-77	MH	12-30-77
3	REVISED PER ECN# 8040 & 8041	TRP	2-2-78	MH	2-2-78
4	REV. PER ECN# 8607	TRP	6-15-78	MH	6-15-78
5	REV PER ECN# 8867	TRP	10-13-78	MH	10-13-78

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MILLIMETERS IN PARENTHESIS. TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

DO NOT SCALE

CONN 350-0060

| | | |

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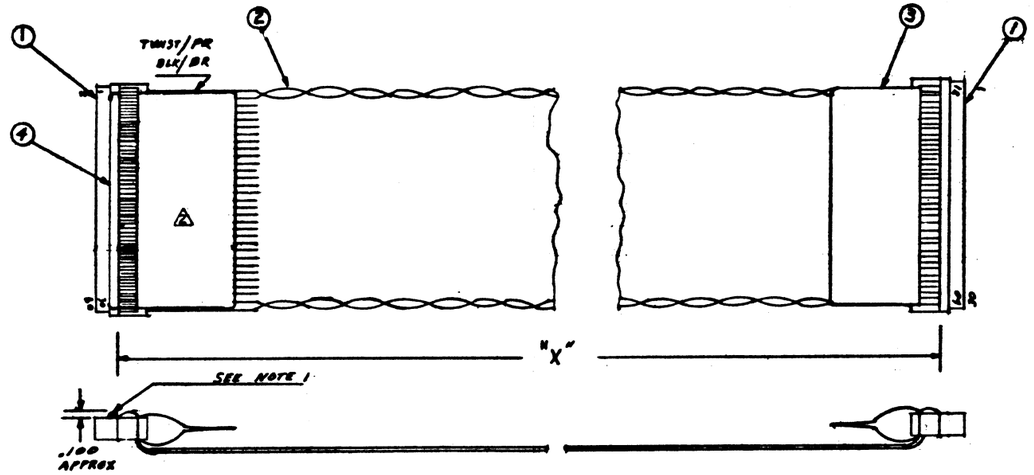
MILLIMETERS IN PARENTHESIS.
TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

DO NOT SCALE

HOLE LEGEND & TOLERANCES	
HOLE DIA	TOLERANCE
.0125 - .125	+ .003 - .001
.126 - .250	+ .004 - .001
.251 - .500	+ .005 - .001

SYM.	DESCRIPTION	QTY.
A		

FRONT VIEW



W. L. PART NO	"X" LENGTH
220-3031	10' ±2"
220-3032	5' ±2"
220-3041	15' ±2"

NOTE:
1. ADD ITEM 4 TO THIS SURFACE ONLY, ON 220-3041 ONLY

ON 220-

COPY
JUL 20 1979

QTY	ITEM	WANG PART NO.	DRAWING NO.	DESCRIPTION
N/R	4	660-0196		HOT MELT ADHESIVE 2000
2	3	350-4120		PULL TAB FOR FLAT CABLE
N/R	2	920-0070		FLAT CABLE 30 TWISTED PAIRS
2	1	350-3419		FLAT CABLE CONN. 60 POS.
NEXT ASSY.				

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	GD	5/31/77	E ENGR	
CHK			M ENGR	
			MFG. ENGR	

MATERIAL

MODEL NO. BOMEG CDC/300MEG CDC
SEE ENGRG SPECIFICATIONS
No.

FINISH

TOL EX AS NOTED
XX ± FRAC ±
XXX ± .100 ± FINISH √

TITLE
30 PAIR FLAT CABLE ASSEMBLY

SCALE	SHT 1 OF 1	SEE CHART	D	6482-188	3
		WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.

NO.	REVISIONS			
0	ORIG. RELEASE	5/31/77	GD	
1	REV PER ECO #0371 AS 12-15-77	12/15/77	JHM	
2	REV PER ECO #0371 AS 5-2-78	5/2/78	JHM	
3	REV PER ECO #0398 AS 7-5-78	7/5/78	JHM	

NOTE:
1. ADD ITEM 4 TO THIS SURFACE ONLY ON 220-3033-1 ONLY
2. ADD ITEM 4 OVER BARE CND WIRE 1 TYP BOTH ENDS
3. ON ITEM 3 BLK LINE GOES TOWARD PIN 1.
4. PULL TAB ON END "B" MUST HAVE A "D" DRAWN ON IT. USE A RED MARKS-A-LOT MARKER.
END "B"
END "A"
"X"
SEE NOTE 2
SEE NOTE 2 .100 APPROX.
STRIP OUTER JACKET + SHIELD 1/2" BOTH ENDS
FRONT VIEW
COPY
JUL 20 1979
W.L. PART NO. | "X" LENGTH
220-3033-1 | 15" ± 2"
220-3033-4 | 24" ± 2"
220-3033-5 | 3" ± 1"
660-0195 | 4 | A/R | HOT MELT ADHESIVE
350-4119 | 3 | 2 | PULL TAB FOR FLAT CABLE
426-0069 | 2 | A/R | FLAT CABLE | 26 COND. SHIELDED
350-0913 | 1 | 2 | CONNECTOR 26 POS
WANG PART NO | ITEM | QTY | NAME | DESCRIPTION
WANG LABORATORIES, INC.
APPROVED BY | DATE
E ENGR
M ENGR
MFG ENGR
E.C. CONTROL
MODEL NO
TITLE 26 CONDUCTOR SHIELDED FLAT CABLE ASSEMBLY
SEE DRAWING SPECIFICATIONS
MATERIAL
FINISH
SEE CHART
C 1482-/89
SCALE
SHT 1 OF 1
REVISION
ORC PER DWR #8322
ORC PER ECN #8193
REV PER DWR#
ECN# 11950
REVISED PER
ECN# 11950/11966
REVISED. DFA
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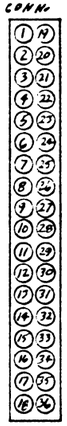
DO NOT SCALE

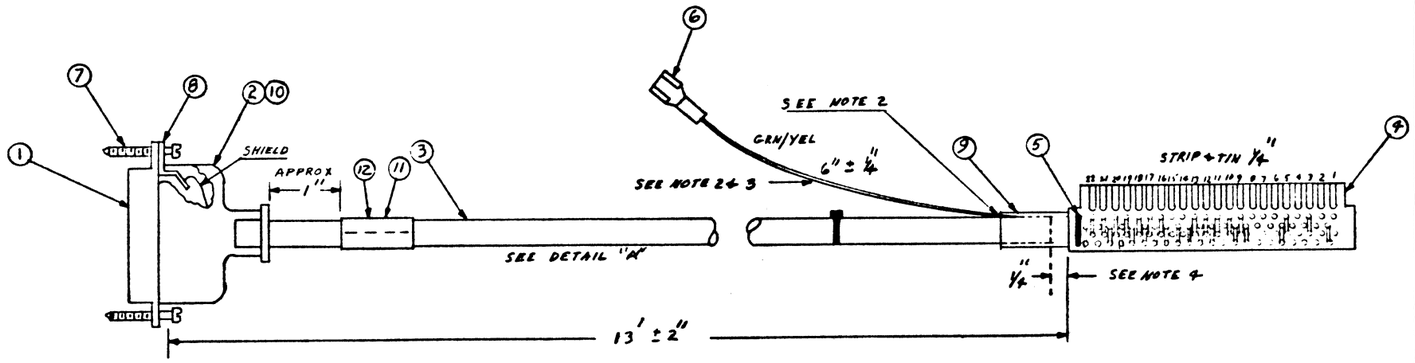
DIMENSIONS IN PARENTHESIS /CLEARANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

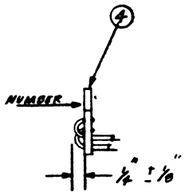
HOLE LEGEND & TOLERANCES			
HOLE DIA		TOLERANCE	
.0135 - .125		± .003	.001
.126 - .250		± .004	.001
.251 - .390		± .005	.001
SYM.	DESCRIPTION		QTY
A			

CONN.



REAR VIEW



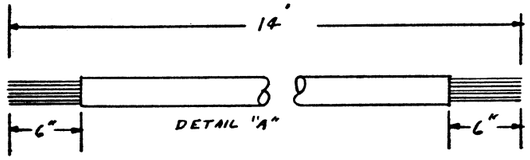


SIGNAL	CONN. PIN NO.		P.C. 6703
DATA STROBE	1		21
DATA 1	2		18
DATA 2	3		16
DATA 3	4		17
DATA 4	5		20
DATA 5	6		15
DATA 6	7		11
DATA 7	8		19
DATA 8	9		12
ACK LG	10		22
BUSY	11		3
PO	12		9
SLOT	13		F
±0V	14		Y
OSC XT	15		H
±0V	16		X
CHASSIS GND	17		4
+5VR	18		13

SIGNAL	CONN. PIN NO.		P.C. 6703
±0V	19		A
±0V	20		C
±0V	21		M
±0V	22		N
±0V	23		P
±0V	24		R
±0V	25		S
±0V	26		T
±0V	27		U
±0V	28		V
±0V	29		W
±0V	30		Z
IP	31		E
FAULT	32		B
±0V	33		K
WST	34		S
±0V	35		10
—	36		—

SEE NOTE 1

NOTES:
1. BUSS JUMPER ADDED FROM K TO M ON FINGER BOARD 6703. THIS WILL PERTAIN TO 220-0171 ONLY.
2. TIN CABLE DRAIN WIRE
3. GRN/YEL WIRE SOLDERED TO CABLE DRAIN WIRE
4. CABLE INSULATION AND FOIL SHOULD BE STRIPPED 1/4" FROM FINGER BOARD 6703
5. TIE EXTRA WIRE BACK AT FINGERBOARD END, AND FOLD BACK AT CONN. END.
6. GRN/YEL WIRE STRIP 1/4" TIN ONE SIDE ONLY



ECN NO. 11984 PENDING

COPY

JUL 20 1979

220-0171	220-0220	QTY.	ITEM	WANG PART NO.	DRAWING NO.	DESCRIPTION
1		12		606-0171-1		HEATSHRINK MARKER 3/8" DIA.
	1	11		606-0171		HEATSHRINK MARKER 3/8" DIA
	A/R	A/R		600-9012		WIRE #24 GA YEL SOLID TEFFLON 3/8" LONG
A/R	A/R	A/R		600-2054		WIRE #18 GA GRN/YEL
1	1	10		350-4228-G		STRAIN RELIEF COVER 36 POS GROOVE HALF
A/R	1	9		605-0132		SHRINK TUBING 1" LONG
1	1	8		458-0361		GROUND STRAP
2	2	7		350-4234		SCREW CAPTIVE
1	1	6		654-0948R		FASTON TERM. RED
2	2	5		605-1004		TY-RAP PAN-TY PLTIM-M
1	1	4		510-6703		PC BD 6703
A/R	NR	3		420-0054		CABLE 36 COND SHIELDED
1	1	2		350-4228-T		STRAIN RELIEF COVER 36 POS TONGUE HALF
1	1	1		350-2082		CONNECTOR MALE (CHAMP) 36 POS

NEXT ASSY.

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL

FINISH

MODEL NO. 77, PROM EMULATOR
SEE ENGRG. SPECIFICATIONS No.

TOL. EX. AS NOTED
XX ± FRAC ±
XXX ± ANG. ± FINISH √

SCALE FF SHT 1 OF 1

BY	DATE	APPROVED BY	DATE
DWN	7/17/79	E ENGR	
CHK		M ENGR	
		MFG ENGR	

TITLE: I/O CABLE PROM EMULATOR

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
SEE ABOVE	D	6782-192	5

D 6782-192

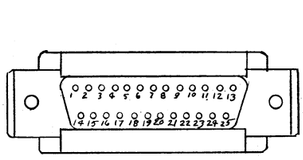
REVISION					
0	ORIG PER DWG #8367	2	PS	F.S.S.	G.D.
1	REVISED PER ECN #7982 APP. G.D. 220-38	1-13-78		4-13-78	5/15/78
2	REVISION PER ECN #8699 ADDED 220-0171				
3	REVISED PER ECN #8996 AS 5-9-78				
4	REVISED PER ECN #9129				
5	REV PER DWG #				

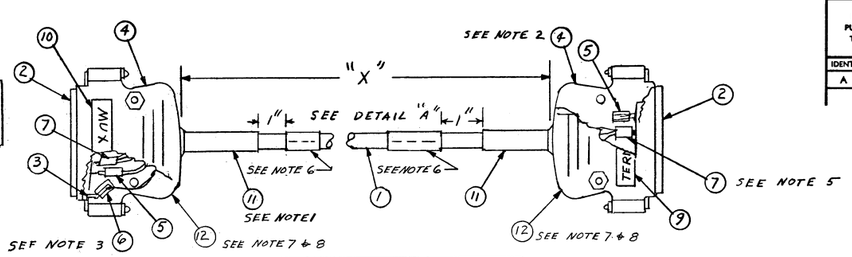
F-83

DO NOT SCALE

HOLE LEGEND		
DRILLED OR PUNCHED HOLE TOLERANCES:	HOLE DIA. .0135 to .125 .126 to .250 .251 to .500	TOL. +.003 -.001 +.004 -.001 +.005 -.001

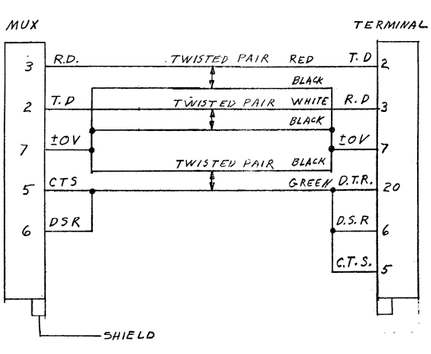
IDENT.	DESCRIPTION	QTY.
A		

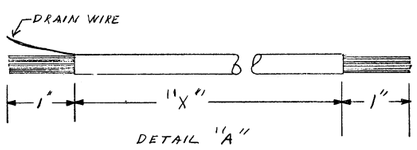




W. L. PART NO.	"X" LENGTH	SLEEVE MARKER
220-2236-25	25' ±3"	606-2236-25
120-2236-50	50' ±3"	606-2236-50
120-2236-1	100' ±3"	606-2236-1
120-2236-2	200' ±3"	606-2236-2
120-2236-3	300' ±3"	606-2236-3
120-2236-4	400' ±3"	606-2236-4
120-2236-5	500' ±1'	606-2236-5
120-2236-6	600' ±1'	606-2236-6
120-2236-7	700' ±1'	606-2236-7
120-2236-8	800' ±1'	606-2236-8
120-2236-9	900' ±1'	606-2236-9
120-2236-10	1000' ±3'	606-2236-10

NOTE:-
1. ASSEMBLE ITEM 11 TO ITEM 1 BEFORE WIRING
2. HARDWARE SUPPLIED WITH ITEM 4
3. USE SLEEVING ITEM 6 OVER DRAIN WIRE
4. SOLDER DRAIN WIRE TO ITEM 3
5. USE SLEEVING ITEM 7 OVER 3 BLACK WIRES
6. APPLY HEATSHRINK MARKER APPROX WHERE SHOWN (2 PER CABLE)
7. ITEM 12 NOT SHOWN.
8. ITEM 12 APPLIED AFTER INSPECTION
9. CUT OFF DRAIN WIRE ON TERMINAL END





DETAIL "A"

NEW 420-0101

WANG PART NO.	ITEM	QTY.	NAME	MATERIAL	DESCRIPTION
685-0099	12	2	BUBBLE BAG		5 1/4" X 4"
			HEATSHRINK MARKER		1/4" DIA
350-4102	11	2	#3 BUSHING		
615-1343	10	1	CABLE LABLE		MUX.
615-1394	9	1	CABLE LABLE		TERMINAL
660-0002	8	A/R	SOLDER		63/37 ALLOY
605-0000	7	2	SLEEVE		#10 TUBING 1/8" LONG
605-0002	6	1	SLEEVE		#15 TUBING 1" LONG
605-0002	5	N/R	SLEEVE		#15 TUBING 1/4" LONG
350-4215	4	2	CONNECTOR SHELL		CANNON # DB 51226-1
458-0361	3	1	GROUND LUG		CGB15-28
350-1030	2	2	CONNECTOR 25 POS		
420-0071	1	A/R	CABLE SHIELDED		3 TWISTED PAIR

WANG PART NO.	QTY. PER UNIT	FIRST USED ON	ASSY USED ON

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

MATERIAL	MODEL NO. 2236
	SEE ENGRG SPECIFICATIONS No.
FINISH	TOL. EX. AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG. ± 1°30' FINISH 125
SCALE FT	SHT 1 OF 1

BY	DATE	APPROVED BY	DATE
DWN LB	12-14-77	E ENGR	
CHK		M ENGR	
E. C. CONTROL		MFG ENGR	1/13/78

TITLE: 2236 DIRECT CABLE ASS'Y

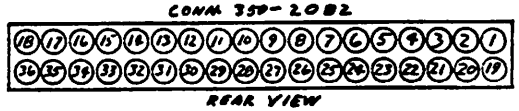
SEE CHART	C	6482-220	4
WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

022-2867 D

NO	REVISION	BY	DATE
0	ONE PER UNIT # 392	G.D.	8/22/78
1	REV PER ECN # 9129 AB 8-9-78	G.D.	8/22/78
2	REV PER ECN # 9254 AB 8-9-78	S.D.	3-13-79
3	REV PER ECN # 10498 APP'D: [illegible] 3-12-79	S.D.	3-13-79
4	REV PER ECN # 10601 APP'D: [illegible] 3-16-79	LB	3-16-79

DO NOT SCALE

CONN 359-2082



REAR VIEW

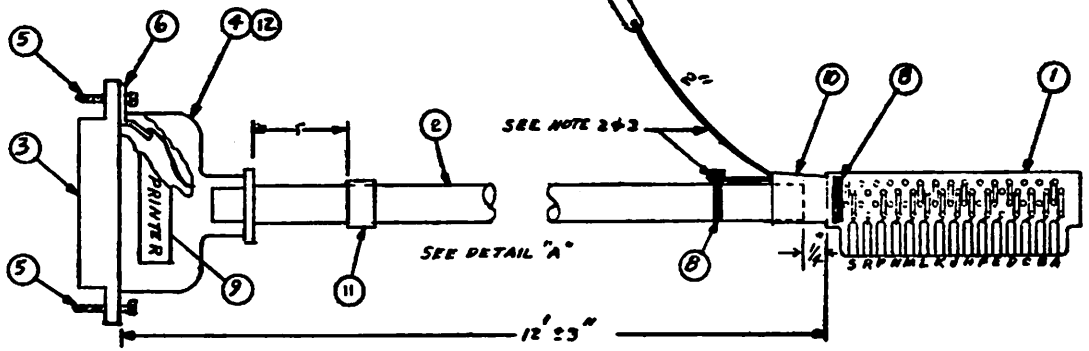
LEGEND

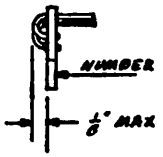
DRILLED OR PUNCHED HOLE TOLERANCES:

HOLE DIA.	TOL.
.0938 to .125	±.002
.126 to .350	±.003
.351 to .500	±.005

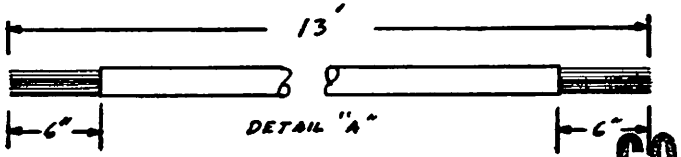
IDENT.	DESCRIPTION	QTY.
A		

CONN PIN NO.	WIRE COLOR	TWISTED PAIR	SIGNAL NAME	P.C. BD 5223C
1	RED	PAIR	DTA SYNC	A
19	GRN		±DV	1
2	RED	PAIR	DATA1	K
20	BRN		±DV	L
3	RED	PAIR	DATA2	H
21	GRY		±DV	J
4	RED	PAIR	DATA3	M
22	ORN		±DV	N
5	RED	PAIR	DATA4	P
23	BLU		±DV	S
6	ORN	PAIR	DATA5	E
24	WHT		±DV	D
7	GRN	PAIR	DATA6	C
25	YEL		±DV	B
8	ORN	PAIR	DATA7	5
26	BLK		±DV	F
9	GRN	PAIR	DATA8	7
27	YEL		±DV	F
10	GRN	PAIR	KERNLG	10
28	WHT		±DV	N
11	GRN	PAIR	BUSY	B
29	BLK		±DV	J
12	BLU	PAIR	—	—
30	YEL			
13	BLU	PAIR	±DV	L
31	BLK		PRIME	J
14	BLU	PAIR	—	—
32	WHT			
15	BRN	PAIR	—	—
33	WHT			
16	BRN	PAIR	±DV	
34	BLK			
17	GRY	PAIR	CN GND	4
35	WHT			
18	GRY	PAIR	+5VR	10
36	BLK			





NOTE:
1. SOLDER ITEM 7 TO DRAIN WIRE.
2. TIN DRAW WIRE FULL LENGTH
3. CUT EXTRA WIRES 2" LONG AND FOLD BACK SECURE UNDER TYRAP



COPY
JUL 20 1979

WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION
350-42336	12	1	STRAIN RELIEF COVER (GROOVE)		180° HALF
606-0181	11	1	HEATSHRINK MARKER		1/2" DIA.
660-0203		A/R	SOLDER		SN63-37
605-0020	10	A/R	HEAT SHRINK TUBING		3/4" LONG
615-1297	9	1	PRINTER CONN. LABEL		A5300-1072
605-1008	8	2	TYRAP		
654-1008	7	7	GROUND LUG		#8
458-0361	6	1	GROUND STRAP		CC815-20
350-4234	5	2	SCREW CAPTIVE		
350-4233T	4	1	STRAIN RELIEF COVER (TONGUE)		180° HALF
350-2082	3	1	CONNECTOR 36POS (MALE)		
420-0058	2	A/R	CABLE 36CONDUCTOR T.P. SHIELDED		
510-5223C	1	1	P.C. BOARD 5223C		

ON PER UNIT	FIRST USED ON	ASSY USED ON

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	[illegible]	7/31/79	E ENGR	
CHK			M ENGR	
E C CONTROL			MFG ENGR	

MATERIAL

MODEL NO 2201L

SEE ENGRG SPECIFICATIONS No.

FINISH

TOL EX AS NOTED
XX ± .010 FRAC ± 1/64
XXX ± .005 ANG ± 1°30' FINISH √

SCALE — SHT 1 OF

TITLE I/O CABLE 2201L

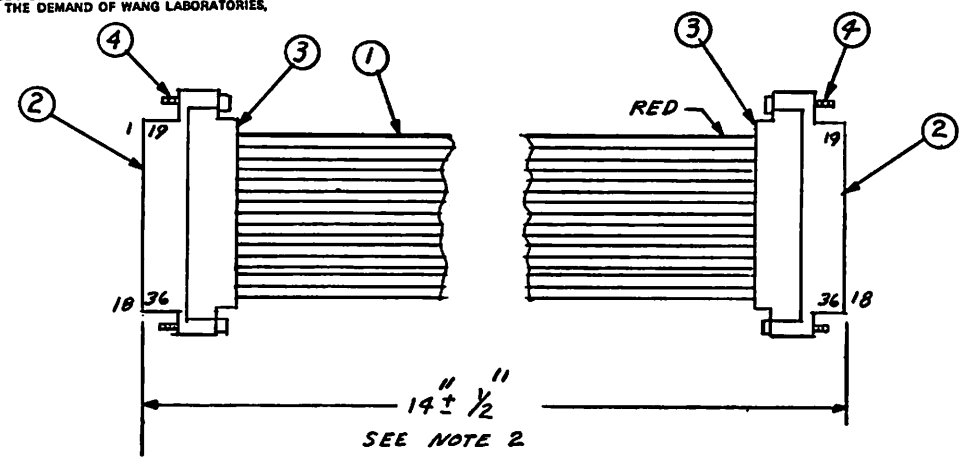
WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
220-0181	C	6482-226	Z

6482-226 D

REVISION	BY	DATE	APPROVED
ADD ITEM 2 SEE SHT 2	[illegible]	7/31/79	
REV. PER ECN 6482	[illegible]	7/31/79	
ADD ITEM 2	[illegible]	7/31/79	

"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF, AND ARE PROPRIETARY TO, WANG LABORATORIES, INC.; THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."

DO NOT SCALE



NOTE:

1. WIRE AS FOLLOWS WIRE 1 TO POS 19
   WIRE 2 TO POS 1
   WIRE 3 TO POS 20
2. PRECUT FLAT CABLE TO MEASURE 16" LONG
3. SPLIT CABLE BACK 3" EACH SIDE.
4. USE BUTTERFLY TO INSERT SINGLE WIRES TO CONN.
5. TEAR OFF LAST FOUR CONDUCTORS

COPY

JUL 20 1979

WANG PART NO.	ITEM	QTY	NAME	DESCRIPTION
350-4234	4	4	CAPTIVE SCREW	4-40 AMP
350-4225	3	4	STRAIN RELIEF 36 POS.	AMP.
350-2082	2	2	CONN. 36 POS PLUG ASSY	AMP. MALE
420-0045	1	A/R	FLAT CABLE	40 CONDUCTOR

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	JS	9/18/78	E ENGR	
CHK	G.D.	11/10/78	M ENGR	11/30/78
E. C. CONTROL			MFG ENGR	

MATERIAL

MODEL NO. 2260 BC

SEE ENGRG SPECIFICATIONS No.

TITLE 36 COND FLAT CABLE 2260BC

FINISH

TOL. EX. AS NOTED .XX ± .010 FRAC. ± 1/64 .XXX ± .005 ANG. ± 1°30' FINISH 125

SCALE — SHT 1 OF 1

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
220-3066	B	6482-320	0

NO.	REVISION	DATE	BY
0	ORG. PER PWR #2569	7/18/78	JS

B 6482-320

F-86

SINGLE BOARD UNITS ONLY

APPENDIX I

CPU/MEMORY PCB UPGRADE OPTIONS

I.1.1 INTRODUCTION

I.1.1.1 Scope and Purpose

The scope and purpose of this manual is to provide the Wang Customer Engineer with the information necessary to install, troubleshoot, and repair the Wang 2200 Computer System in the field. Familiarity with the Wang 2200 product line is recommended for effective use of this manual.

The 2200 Computer System is an interactive, multi-user, multi-task, disk-based computer system, utilizing VLSI [Very Large Scale Integration] technology. The 2200 Computer System supports up to 16 terminals and 16 jobs [partitions] concurrently as well as a wide range of peripheral devices, such as printers, plotters, disk drives, tape drives, and TC devices. Disk drive sharing for up to 15 additional CPUs is also available as an option.

By utilizing VLSI, the 2200 Computer System processor design is incorporated into a single chip. This allows the 2200 CPU, control memory, and user memory to reside on a single PC board. The two models of the 2200 Computer System offered are the 2200 MVP-128 that contains 128KB of Data Memory and the 2200 MVP-512 which contains 512KB of Data Memory. Both systems, however, contain 32K of Control Memory. In addition, these two existing 128KB or 512KB CPU PCBs may be upgraded to Enhanced CPU/Memory configurations via upgrade kits.

I.2.1 DIAGNOSTIC ERROR MESSAGES

I.2.1.1 AEDM Errors (Addressing Error in Data Memory)

NOTE

> When memory exceeds 512KB, the address information that is displayed for memory error at boot time is invalid.

This error is displayed as:

```
AEDM ss.aaaa ss.bbbb xx
```

Where:

```
  ss=Memory bank containing the error.
aaaa=Address of the data in error.
bbbb=Conflicting Address
  xx=XOR of the "expected" and
     "actually read" data.
```

This error indicates that writing to location "bbbb" seems to modify location "aaaa". The "1" bits in the "xx" field of the display indicate which bits have been modified. The error could also occur if a chip at location "aaaa" had a marginal failure.

I.2.1.2 BEDM Errors (Bit Error in Data Memory)

NOTE

When memory exceeds 512KB, the address information that is displayed for memory error at boot time is invalid.

This error is displayed as:

BEDM ss.aaaa xxyy

Where:
ss=Memory bank containing the error.
aaaa=Address of the data in error.
xxyy=XOR of the data "actually read" from data memory with the data that was "expected" to be there.

This error implies that a memory error was detected while reading data memory. The "1" bits in the "xxyy" field of the display indicate which bit[s] are not correct. If all the bits are zero, one of the two parity bits associated with the pair of bytes is incorrect.

I.2.1.3 PEDM Errors (Parity Error in Data Memory)

NOTE

When memory exceeds 512KB, the address information that is displayed for memory error at boot time is invalid.

This error is displayed as:

PEDM ss.aaaa

Where:
ss=Memory bank containing the error.
aaaa=Data Memory Address at the time of the error. This is probably, but not necessarily, the address of the memory location with bad parity.

This error implies that bad parity was detected during a read of an 8-bit User/Data Memory.

I.2.1.4 REDM Errors (Read Error in Data Memory)

NOTE

When memory exceeds 512KB, the address information that is displayed for memory error at boot time is invalid.

This error is displayed as:

REDM ss.aaaa xx

Where:
ss=Memory bank containing the error.
aaaa=Address of the data in error.
xx=XOR of the data in memory with the data that was expected to be there.

This error implies that a memory error was detected while reading User/Data memory. The "1" bits on the "xx" field of the display indicate which bits are not correct. If all the bits are zero, a bit in the other byte of the pair of bytes is incorrect.

I.2.1.5 VEDM Errors (Verify Error in Data Memory)

NOTE

When memory exceeds 512KB, the address information that is displayed for memory error at boot time is invalid.

This error is displayed as:

VEDM ss.aaaa

Where:
ss=Memory bank containing the error.
aaaa=Address of the data in error.

This error is reported to a system program being given control after loading, or when memory is verified in response to RESET or CLEAR being executed. The area of User/Data Memory used for storing constants [BASIC verb tables, math constants, messages] does not verify correctly.

I.3.1 INSTALLING OPTIONS

I.3.1.1 Existing 2200 CPU/Memory PCB Upgrades

Existing 128KB or 512KB CPU PCB users have the option of direct swap-out replacement of current 128KB or 512KB CPU PCBs for the Enhanced CPU PCBs, by ordering Upgrade kits as follows:

Kit Name	Kit P/N	Kit Description	Enhanced CPU PCB P/N
UJ 5057	289-0969	128KB PCB to 512KB PCB	210-8937-B
UJ 5065	289-0968	128KB PCB to 1MB PCB	210-8937-C
UJ 5066	289-0967	128KB PCB to 2MB PCB	210-8937-D
UJ 5067	289-0966	128KB PCB to 4MB PCB	210-8937-E
UJ 5068	289-0965	128KB PCB to 8MB PCB	210-8937-F
UJ 5069	289-0964	512KB PCB to 1MB PCB	210-8937-C
UJ 5070	289-0963	512KB PCB to 2MB PCB	210-8937-D
UJ 5071	289-0962	512KB PCB to 4MB PCB	210-8937-E
UJ 5072	289-0961	512KB PCB to 8MB PCB	210-8937-F

CPU/Memory PCB Replacement Instructions:

1) Power-down system (Ref. section 3.7).

2) Remove the existing 128KB or 512KB CPU PCB (Ref. section 7.1.1).

3) Install the Enhanced CPU PCB replacement (Ref. reverse steps of section 7.1.1).

4) Power-up system (Ref. reverse steps of section 3.7).

5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

I.3.1.2 Enhanced 2200 CPU/Memory PCB Upgrades

NOTE

When the accessed memory exceeds 512KB, Operating System Version 3.1 minimum is required.

NOTE

The Micro Diagnostic for Enhanced Memory Test is incorporated in the Operating System Release 3.1.

I.3.1.2 Enhanced 2200 CPU/Memory PCB Upgrades (Cont'd)

2200 CPU/Memory PCB Upgrade Kits:

MODEL NUMBER	DESCRIPTION
UJ-5057	128KB to 512KB Memory Upgrade
UJ-5059	1MB to 2MB Memory Upgrade
UJ-5060	1MB to 4MB Memory Upgrade
UJ-5061	1MB to 8MB Memory Upgrade
UJ-5062	2MB to 4MB Memory Upgrade
UJ-5063	2MB to 8MB Memory Upgrade
UJ-5064	4MB to 8MB Memory Upgrade
UJ-5065	128KB to 1MB Memory Upgrade
UJ-5066	128KB to 2MB Memory Upgrade
UJ-5067	128KB to 4MB Memory Upgrade
UJ-5068	128KB to 8MB Memory Upgrade
UJ-5069	512KB to 1MB Memory Upgrade
UJ-5070	512KB to 2MB Memory Upgrade
UJ-5071	512KB to 4MB Memory Upgrade
UJ-5072	512KB to 8MB Memory Upgrade

2200 CPU/Memory PCB Upgrade Kit Contents:

Each Upgrade Kit includes the following items:

- PAL chip specifically tailored to desired Upgrade Memory size
- Necessary quantity of additional SIMMs Memory Modules to accomplish the upgrade
- Operating System installed on diskette only

Enhanced CPU/Memory PCB Upgrade Installation Instructions:

Presently installed CPU/Memory PCBs may be upgraded to Enhanced CPU/Memory by ordering upgrade kits as follows:

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
128KB	512KB	UJ5057	289-0969	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:

1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 7.1.1).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-B (Ref. section 7.1.1).
4) Power-up system (Ref. reverse steps of section 3.7).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

Enhanced CPU/Memory PCB Upgrade Installation Instructions: (Cont'd)

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
128KB	1MB	UJ5065	289-0968	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 7.1.1).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-C (Ref. section 7.1.1).
4) Power-up system (Ref. reverse steps of section 3.7).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
128KB	2MB	UJ5066	289-0967	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 7.1.1).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-D (Ref. section 7.1.1).
4) Power-up system (Ref. reverse steps of section 3.7).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
128KB	4MB	UJ5067	289-0966	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 7.1.1).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-E (Ref. section 7.1.1).
4) Power-up system (Ref. reverse steps of section 3.7).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

Enhanced CPU/Memory PCB Upgrade Installation Instructions: (Cont'd)

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
128KB	8MB	UJ5068	289-0965	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 7.1.1).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-F (Ref. section 7.1.1).
4) Power-up system (Ref. reverse steps of section 3.7).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
512KB	1MB	UJ5069	289-0964	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 7.1.1).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-C (Ref. section 7.1.1).
4) Power-up system (Ref. reverse steps of section 3.7).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
512KB	2MB	UJ5070	289-0963	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:
1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 7.1.1).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-D (Ref. section 7.1.1).
4) Power-up system (Ref. reverse steps of section 3.7).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

Enhanced CPU/Memory PCB Upgrade Installation Instructions: (Cont'd)

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
512KB	4MB	UJ5071	289-0962	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:

1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 7.1.1).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-E (Ref. section 7.1.1).
4) Power-up system (Ref. reverse steps of section 3.7).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
512KB	8MB	UJ5072	289-0961	Kit includes new Enhanced CPU PCB.

To accomplish upgrade, perform following:

1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 7.1.1).
3) Install new Enhanced CPU/Memory PCB P/N 210-8937-F (Ref. section 7.1.1).
4) Power-up system (Ref. reverse steps of section 3.7).
5) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E to verify system operation (supports memory up to 8MB).

Enhanced CPU/Memory PCB Upgrade Installation Instructions: (Cont'd)

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
1MB	2MB	UJ5059	289-0960	Kit includes one (1) new PAL chip for memory addressing (P/N 377-3486) and two (2) 1MB x 9 SIMMs Modules (P/N 377-4513).

To accomplish upgrade, perform following:

1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 7.1.1).
3) Replace the PAL chip at PCB location L2 with the PAL chip supplied in kit (Ref. Figure I-1).
4) Remove the four (4) 256KB SIMMs Modules (Ref. Figures I-1 and I-2).
5) Insert two (2) 1MB SIMMs Modules from the kit into the first two (2) empty SIMMs sockets starting at the bottom of the SIMMs connectors (Ref. Figures I-1 and I-3).
6) Position jumper J2 correctly to reflect the 1MB SIMMs Module installation (Ref. Figure I-4).
7) Install the CPU/Memory PCB (Ref. section 7.1.1).
8) Power-up system (Ref. reverse steps of section 3.7).
9) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
1MB	4MB	UJ5060	289-0959	Kit includes one (1) new PAL chip for memory addressing (P/N 377-3487) and four (4) 1MB x 9 SIMMs Modules (P/N 377-4513).

To accomplish upgrade, perform following:

1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 7.1.1).
3) Replace the PAL chip at PCB location L2 with the PAL chip supplied in kit (Ref. Figure I-1).
4) Remove the four (4) 256KB SIMMs Modules (Ref. Figures I-1 and I-2).
5) Insert four (4) 1MB SIMMs Modules from the kit into the first four (4) empty SIMMs sockets starting at the bottom of the SIMMs connectors (Ref. Figures I-1 and I-3).
6) Position jumper J2 correctly to reflect the 1MB SIMMs Module installation (Ref. Figure I-4).
7) Install the CPU/Memory PCB (Ref. section 7.1.1).
8) Power-up system (Ref. reverse steps of section 3.7).
9) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E (supports memory up to 8MB).

Enhanced CPU/Memory PCB Upgrade Installation Instructions: (Cont'd)

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
1MB	8MB	UJ5061	289-0958	Kit includes one (1) new PAL chip for memory addressing (P/N 377-3488) and eight (8) 1MB x 9 SIMMs Modules (P/N 377-4513).

To accomplish upgrade, perform following:

1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 7.1.1).
3) Replace the PAL chip at PCB location L2 with the PAL chip supplied in kit (Ref. Figure I-1).
4) Remove the four (4) 256KB SIMMs Modules (Ref. Figures I-1 and I-2).
5) Insert eight (8) 1MB SIMMs Modules from the kit into the eight (8) empty SIMMs sockets at the bottom of the SIMMs PCB connectors (Ref. Figures I-1 and I-3).
6) Position jumper J2 correctly to reflect the 1MB SIMMs Module installation (Ref. Figure I-4).
7) Install the CPU/Memory PCB (Ref. section 7.1.1).
8) Power-up system (Ref. reverse steps of section 3.7).
9) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
2MB	4MB	UJ5062	289-0957	Kit includes one (1) new PAL chip for memory addressing (P/N 377-3487) and two (2) 1MB x 9 SIMMs Modules (P/N 377-4513).

To accomplish upgrade, perform following:

1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 7.1.1).
3) Replace the PAL chip at PCB location L2 with the PAL chip supplied in kit (Ref. Figure I-1).
4) Insert the two (2) additional 1MB x 9 SIMMs Modules from the kit into the first two (2) empty SIMMs sockets at the bottom of the SIMMs connectors (Ref. Figures I-1 and I-3).
5) Install the CPU/Memory PCB (Ref. section 7.1.1).
6) Power-up system (Ref. reverse steps of section 3.7).
7) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E (supports memory up to 8MB).

Enhanced CPU/Memory PCB Upgrade Installation Instructions: (Cont'd)

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
2MB	8MB	UJ5063	289-0956	Kit includes one (1) new PAL chip for memory addressing (P/N 377-3488) and six (6) 1MB x 9 SIMMs Modules (P/N 377-4513).

To accomplish upgrade, perform following:

1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref. section 7.1.1).
3) Replace the PAL chip at PCB location L2 with the PAL chip supplied in kit (Ref. Figure I-1).
4) Insert the six (6) additional 1MB x 9 SIMMs Modules from the kit into the first six (6) empty SIMMs sockets at the bottom of the SIMMs connectors (Ref. Figures I-1 and I-3).
5) Install the CPU/Memory PCB (Ref. section 7.1.1).
6) Power-up system (Ref. reverse steps of section 3.7).
7) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E (supports memory up to 8MB).

UPGRADE FROM	UPGRADE TO	UPGRADE KIT NUMBER	PART NUMBER	UPGRADE COMMENTS
4MB	8MB	UJ5064	289-0955	Kit includes one (1) new PAL chip for memory addressing (P/N 377-3488) and four (4) 1MB x 9 SIMMs Modules (P/N 377-4513).

To accomplish upgrade, perform following:

1) Power-down system (Ref. section 3.7).
2) Remove presently installed CPU/Memory PCB from system (Ref section 7.1.1).
3) Replace the PAL chip at PCB location L2 with the PAL chip supplied in kit (Ref. Figure I-1).
4) Insert the four (4) additional 1MB x 9 SIMMs Modules from the kit into the first four (4) empty SIMMs sockets at the bottom of the SIMMs connectors (Ref. Figures I-1 and I-3).
5) Install the CPU/Memory PCB (Ref. section 7.1.1).
6) Power-up system (Ref. reverse steps of section 3.7).
7) Run Diagnostic Package P/N 195-2956-0, Memory Diagnostic Revision 179E (supports memory up to 8MB).

I.3.1.2 Enhanced 2200 CPU/Memory PCB Upgrades (Cont'd)

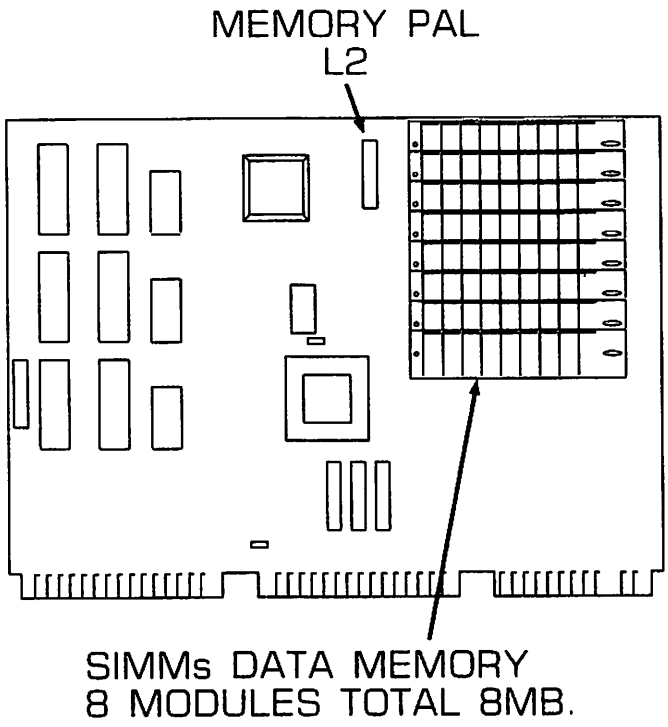


Figure I-1. Enhanced 2200 CPU/Memory PCB Components Layout

I.3.1.2 Enhanced 2200 CPU/Memory PCB Upgrades (Cont'd)

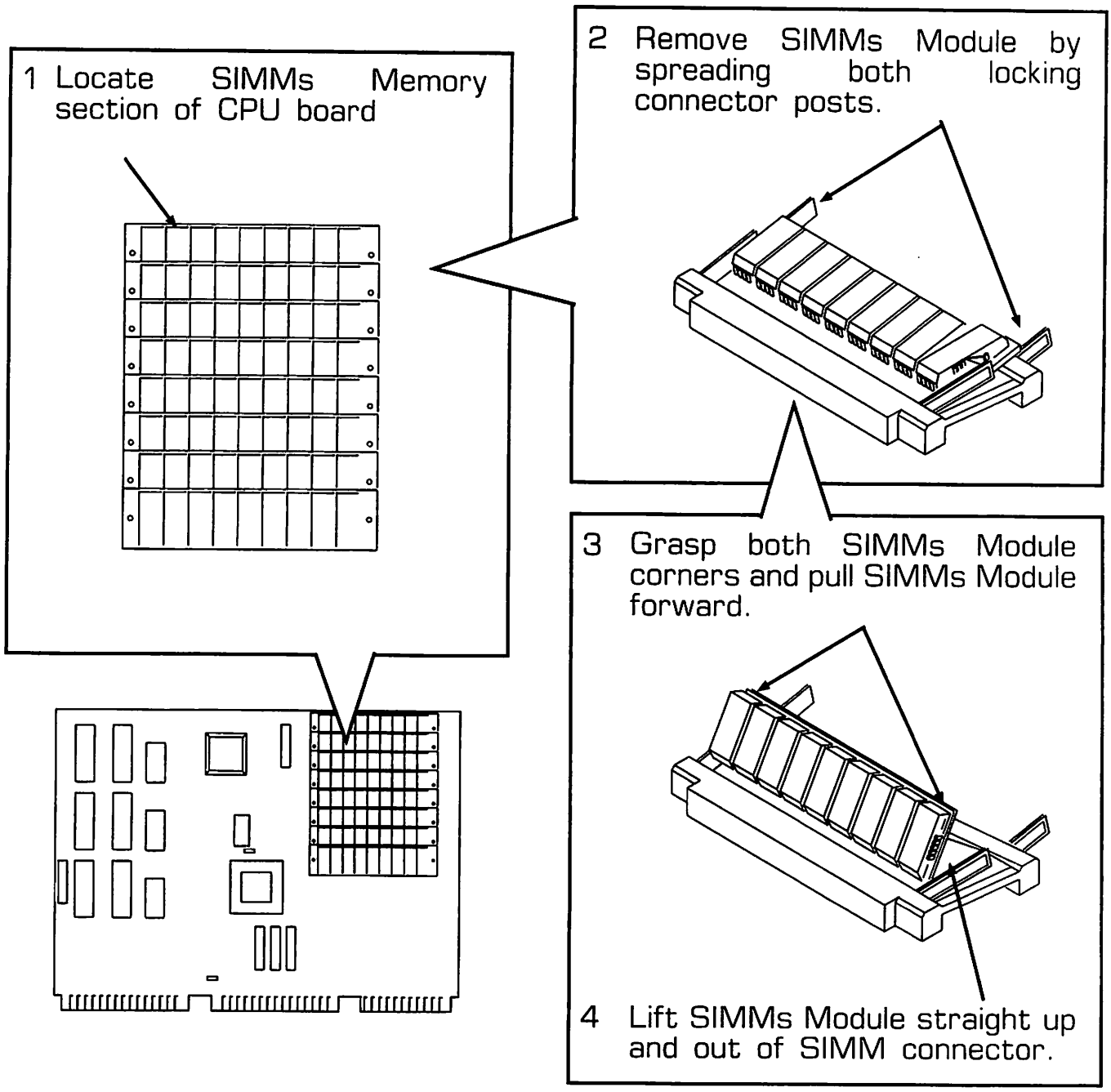


Figure I-2. Enhanced 2200 CPU/Memory PCB SIMMs Module Removal

I.3.1.2 Enhanced 2200 CPU/Memory PCB Upgrades (Cont'd)

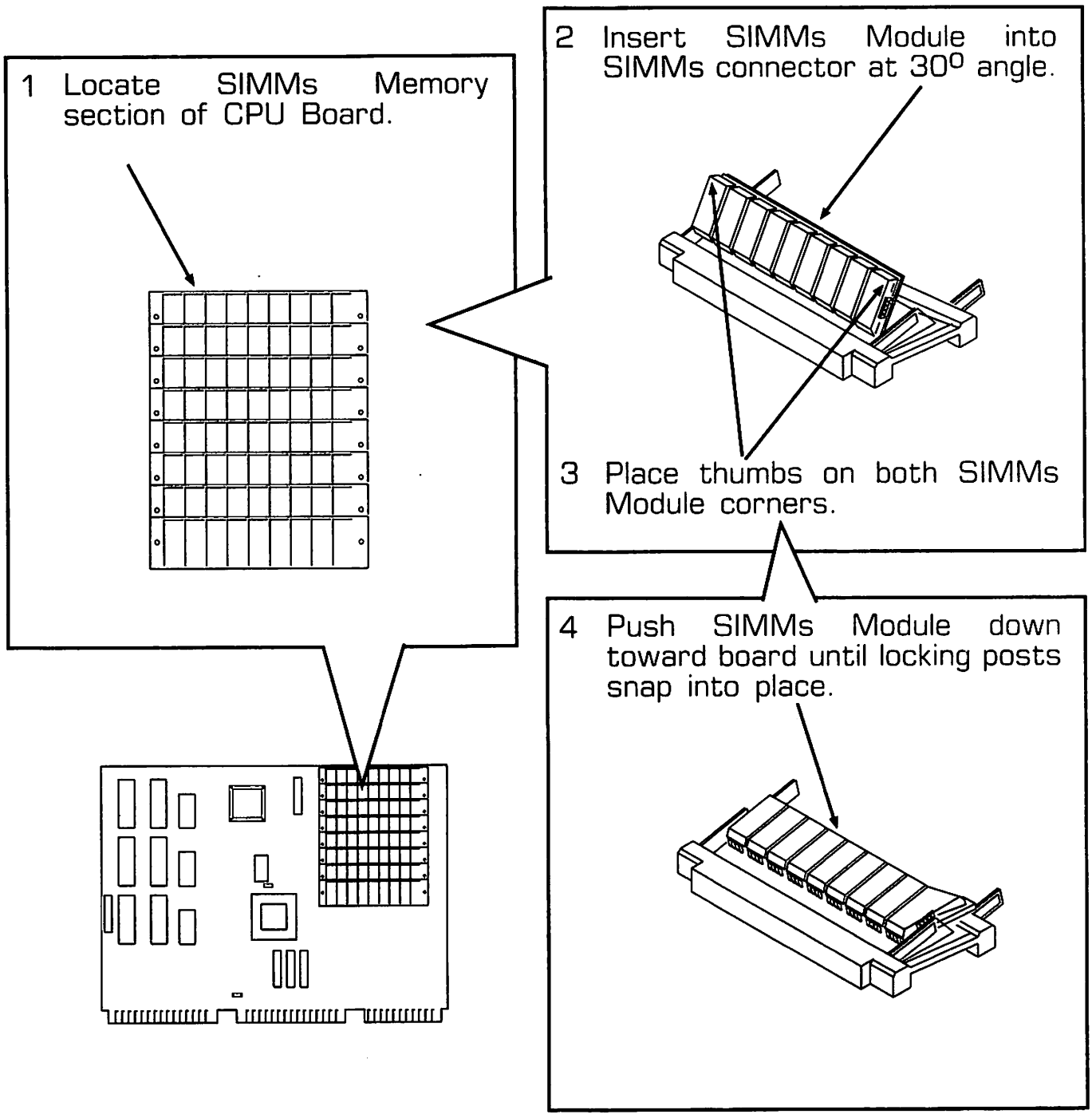


Figure I-3. Enhanced 2200 CPU/Memory SIMMs Module Insertion

I.3.1.2 Enhanced 2200 CPU/Memory PCB Upgrades (Cont'd)

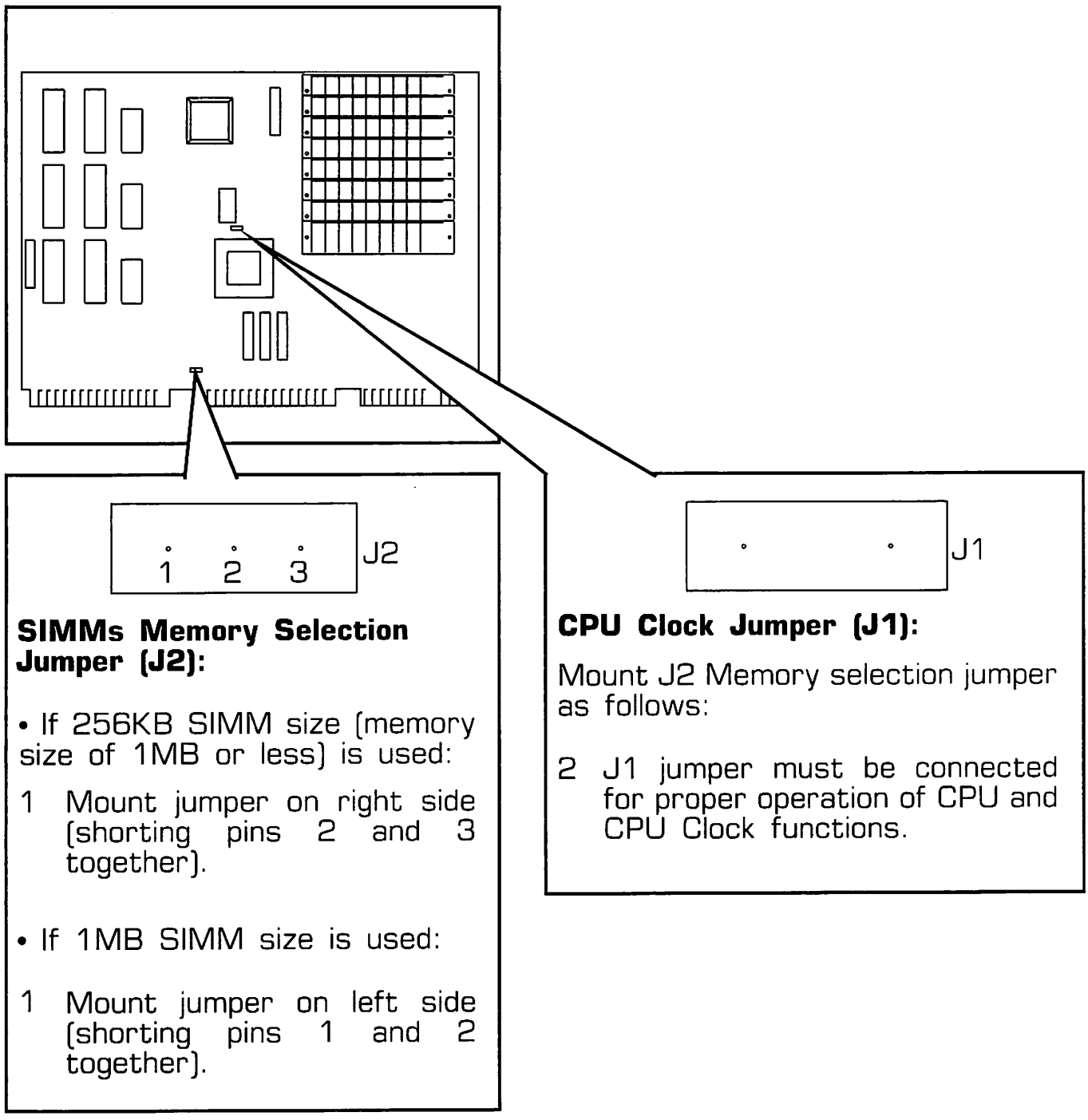


Figure I-4. Enhanced 2200 SIMMs CPU/Memory PCB Jumpers

I.4.1 FUNCTIONAL DESCRIPTION

I.4.1.1 Introduction

The overall operation of the Micro VP-1 and VP-2 is controlled by the CPU/Memory Board (P/N 210-8034-1, 210-8034-2 or 210-8937-A thru F). This new Enhanced CPU/Memory PCB increases the maximum system memory to 8MB. This increased memory allows the user to allocate up to 1MB for user partitions. Memory not allocated to user partitions will be reserved for RAMDISK. This section provides a brief description of this CPU.

I.4.2 CPU FUNCTIONAL THEORY

I.4.2.1 128KB Data Memory (2200 - Original CPU PCB)

With a 128K Data Memory configuration there are two banks, with 9 chips in each bank, for a total of 18 chips. Each chip contains 64K x 1 bit which produces 64K x 9 bits [8 data bits plus 1 parity bit] in each bank. Together the two banks produce 128K 8 bit bytes plus parity. Operation of the data memory is controlled by the Data Memory Controller chip.

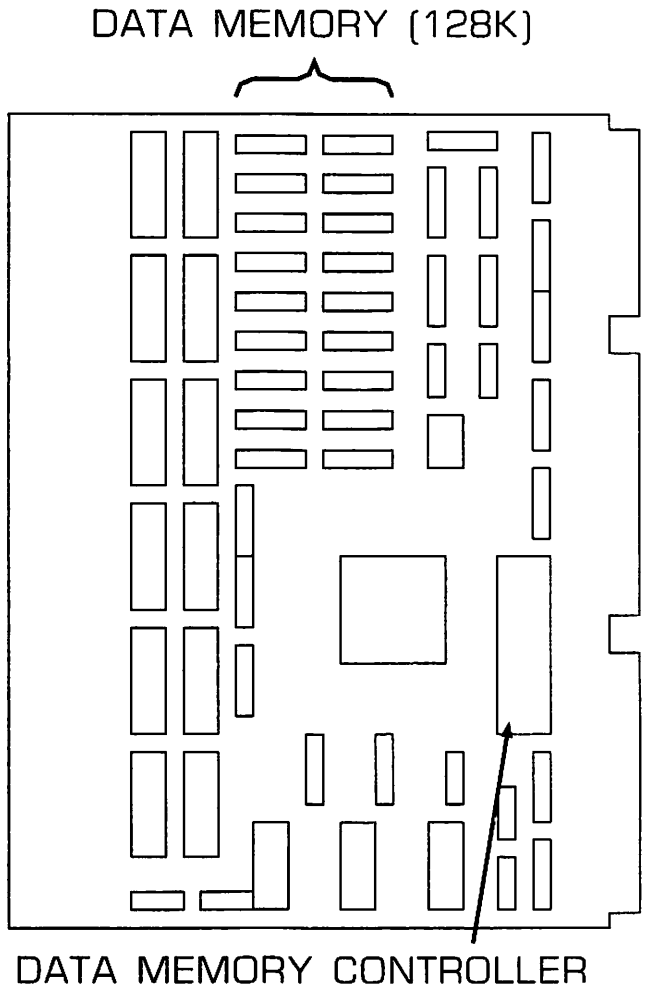


Figure I-5. 2200 Original CPU/Data Memory PCB (128KB)

I.4.2.2 128KB Data Memory (2200 - Enhanced CPU PCB)

With a 128K Data Memory configuration there are two 256KB SIMMs Modules, with 9 SIMMs chips on each module. Each SIMMs chip contains 256K x 1 bit which produces 256K x 9 bits [8 data bits plus 1 parity bit] on each module. Together the two SIMMs modules produce 128K 8 bit bytes plus parity. Data Memory addressing is accomplished by the PAL chip at CPU board location L2.

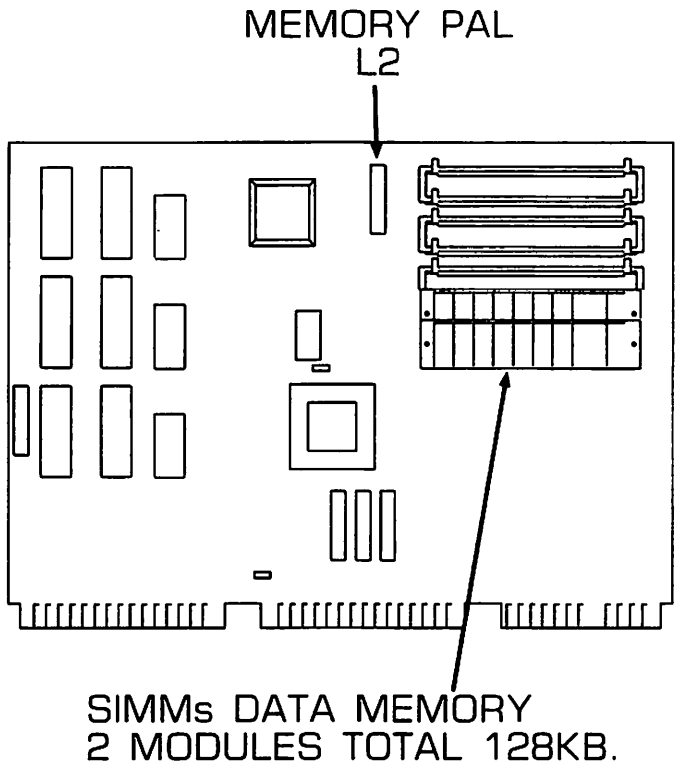


Figure I-6. 2200 Enhanced CPU/Data Memory PCB (128KB)

I.4.2.3 512KB Data Memory (2200 - Original CPU PCB)

With a 512K Data Memory configuration there are two banks, with 9 chips in each bank, for a total of 18 chips. Each chip contains 256K x 1 bit which produces 256K x 9 bits [8 data bits plus 1 parity bit] in each bank. Together the two banks produce 512K 8 bit bytes plus parity. Operation of the data memory is controlled by the Data Memory Controller chip.

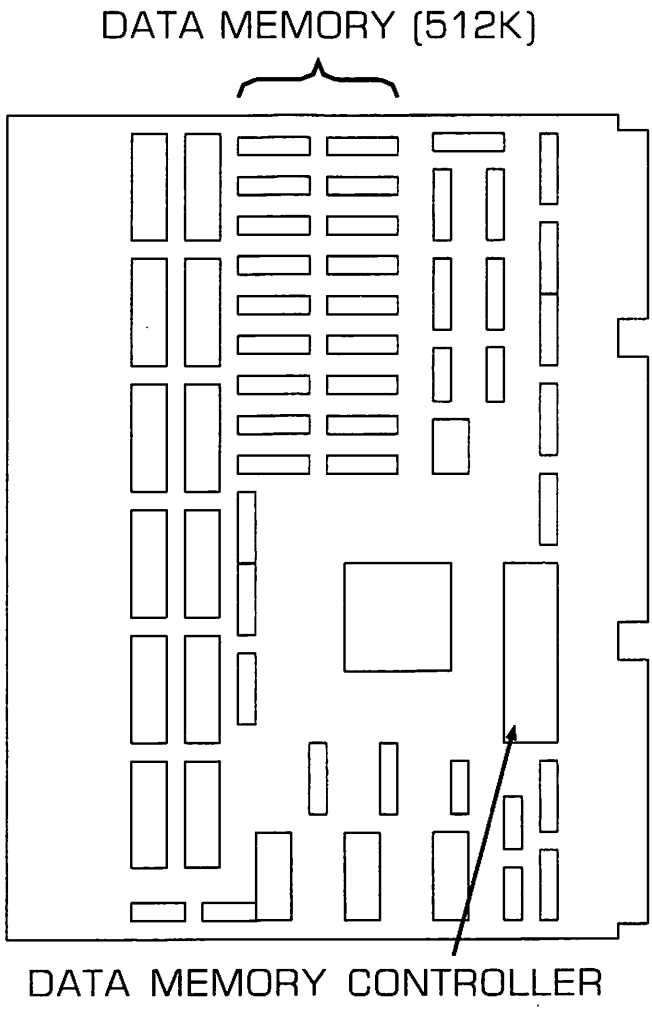


Figure I-7. 2200 Original CPU/Data Memory PCB (512KB)

I.4.2.4 512KB Data Memory (2200 - Enhanced CPU PCB)

With a 512K Data Memory configuration there are two 256K SIMMs Modules, with 9 SIMMs chips on each module. Each SIMMs chip contains 256K x 1 bit which produces 256K x 9 bits [8 data bits plus 1 parity bit] on each module. Together the two SIMMs modules produce 512K 8 bit bytes plus parity. Data Memory addressing is accomplished by the PAL chip at CPU board location L2.

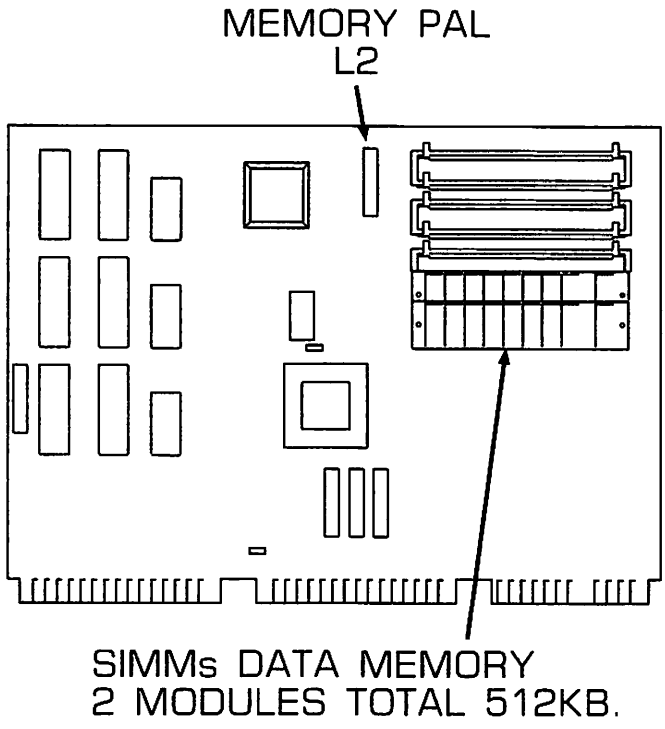


Figure I-8. 2200 Enhanced CPU/Data Memory PCB (512KB)

I.4.2.5 1MB Data Memory (2200 - Enhanced CPU PCB)

With a 1MB Data Memory configuration there are four 256K SIMMs Modules, with 9 SIMMs chips on each module. Each SIMMs chip contains 256K x 1 bit which produces 256K x 9 bits [8 data bits plus 1 parity bit] on each module. Together the four SIMMs modules produce 1MB 8 bit bytes plus parity. Data Memory addressing is accomplished by the PAL chip at CPU board location L2.

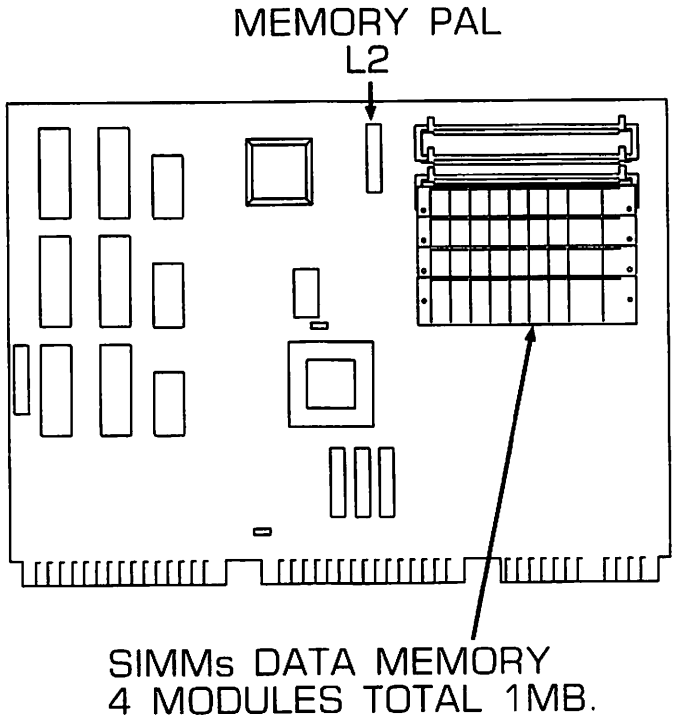


Figure I-9. 2200 Enhanced CPU/Data Memory PCB (1MB)

I.4.2.6 2MB Data Memory (2200 - Enhanced CPU PCB)

With a 2MB Data Memory configuration there are two 1MB SIMMs Modules, with 9 SIMMs chips on each module. Each SIMMs chip contains 1MB x 1 bit which produces 1MB x 9 bits [8 data bits plus 1 parity bit] on each module. Together the two SIMMs modules produce 2MB 8 bit bytes plus parity. Data Memory addressing is accomplished by the PAL chip at CPU board location L2.

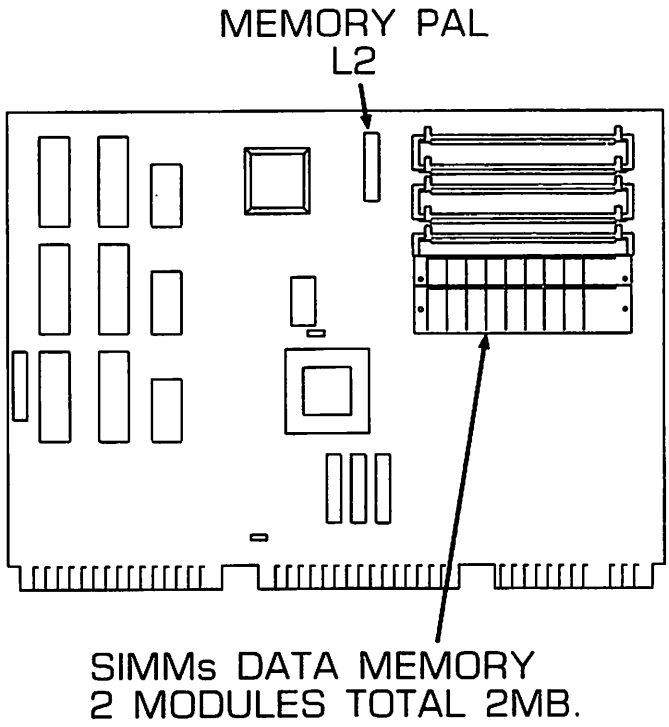


Figure I-10. 2200 Enhanced CPU/Data Memory PCB (2MB)

I.4.2.7 4MB Data Memory (2200 - Enhanced CPU PCB)

With a 4MB Data Memory configuration there are four 1MB SIMMs Modules, with 9 SIMMs chips on each module. Each SIMMs chip contains 1MB x 1 bit which produces 1MB x 9 bits [8 data bits plus 1 parity bit] on each module. Together the four SIMMs modules produce 4MB 8 bit bytes plus parity. Data Memory addressing is accomplished by the PAL chip at CPU board location L2.

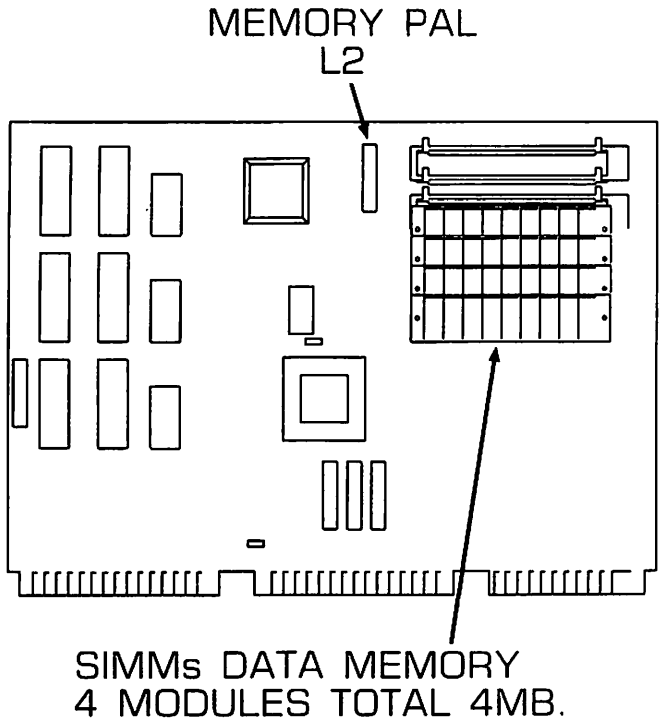


Figure I-11. 2200 Enhanced CPU/Data Memory PCB (4MB)

I.4.2.8 8MB Data Memory (2200 - Enhanced CPU PCB)

With a 8MB Data Memory configuration there are eight 1MB SIMMs Modules, with 9 SIMMs chips on each module. Each SIMMs chip contains 1MB x 1 bit which produces 1MB x 9 bits [8 data bits plus 1 parity bit] on each module. Together the eight SIMMs modules produce 8MB 8 bit bytes plus parity. Data Memory addressing is accomplished by the PAL chip at CPU board location L2.

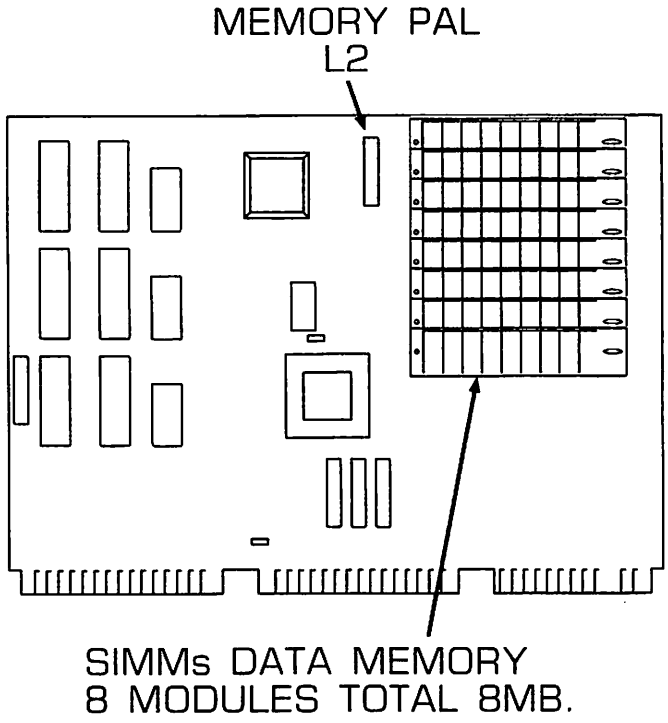


Figure I-12. 2200 Enhanced CPU/Data Memory PCB (8MB)

I.4.3 Memory Partitioning

When using the 512KB Memory, the maximum memory partition size is 28KB if all 16 partitions are used. When Main Memory is increased to 1MB, the maximum memory partition size will increase to 56KB.

I.4.4 Enhanced CPU/Memory Board Block Diagram

The Enhanced CPU/Memory Board Block Diagram is not included in this edition of the Micro VP Computer System Manual. This information will be provided in a subsequent edition.

Programmable Array Logic (PAL):

Data Memory Addressing is accomplished on the Enhanced CPU Board via PAL circuitry at CPU Board location L2. PAL logic chips are programmable 20 pin DIP packaged AND array that provides inputs to a fixed OR array. Based on proven fuseable-link technology, PALs solve three problem areas which are:

- Decreasing board space due to increasing board density
- Inventory reduction due to less need for logic chips
- PALs accept fast internal design changes limited to fuseable links

Programmable Array Logic (PAL) chips greatly enhance 32 bit design, performance and unique operation of 16 bit processors.

I.5.1 ILLUSTRATED PARTS

I.5.1.1 System Components (Sheet 1 of 3)

Item	Part Number	Description
1	210-8034-1	128KB CPU Board (Original CPU)
2	210-8034-2	512KB CPU Board (Original CPU)

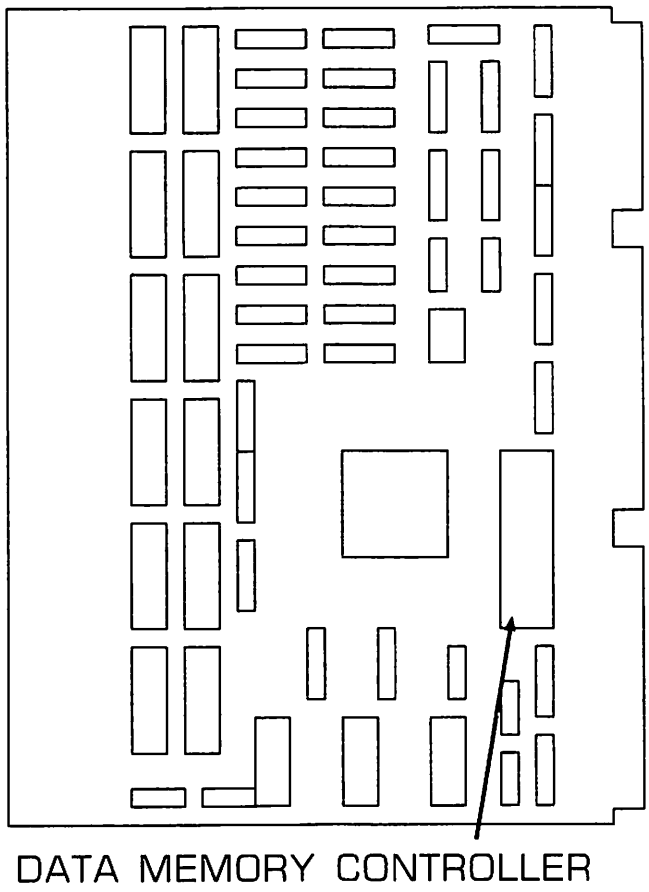


Figure I-13. 2200 Computer System Components

I.5.1.1 System Components (Sheet 2 of 3)

Item	Part Number	Description
3	210-8937-A	128KB CPU Board (Enhanced CPU Model)
4	210-8937-B	512KB CPU Board (Enhanced CPU Model)
5	210-8937-C	1MB CPU Board (Enhanced CPU Model)
6	210-8937-D	2MB CPU Board (Enhanced CPU Model)
7	210-8937-E	4MB CPU Board (Enhanced CPU Model)
8	210-8937-F	8MB CPU Board (Enhanced CPU Model)

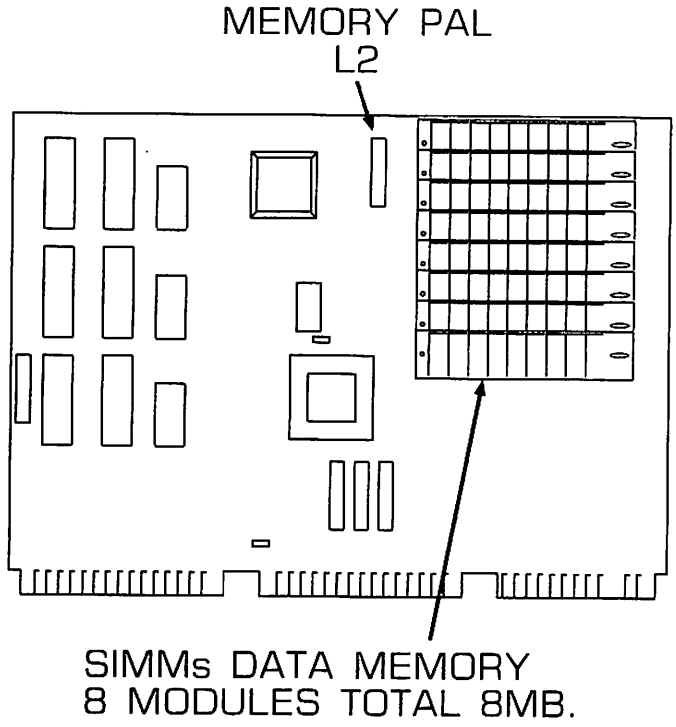


Figure I-14. 2200 Computer System Components

I.5.1.1 System Components (Sheet 3 of 3)

Item	Part Number	Description
9	377-4508	256KB SIMMs CPU Memory Module
10	377-4513	1MB SIMMs CPU Memory Module
11	377-3483	Memory PAL (L2) (128KB CPU Memory Board)
12	377-3484	Memory PAL (L2) (512KB CPU Memory Board)
13	377-3485	Memory PAL (L2) (1MB CPU Memory Board)
14	377-3486	Memory PAL (L2) (2MB CPU Memory Board)
15	377-3487	Memory PAL (L2) (4MB CPU Memory Board)
16	377-3488	Memory PAL (L2) (8MB CPU Memory Board)

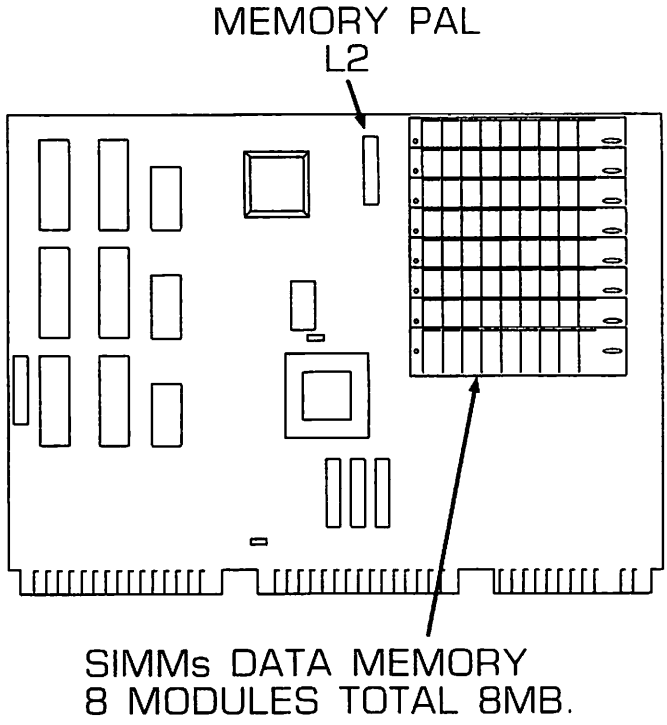


Figure I-15. 2200 Computer System Components

North America:

Alabama
Birmingham
Mobile

Alaska
Anchorage

Arizona
Phoenix
Tucson

California
Fresno
Inglewood
Los Angeles
Sacramento
San Diego
San Francisco
San Mateo
Sunnyvale
Tustin
Ventura

Colorado
Denver

Connecticut
New Haven
Stamford
Wethersfield

District of Columbia
Washington

Florida
Jacksonville
Miami
Orlando
Tampa

Georgia
Atlanta

Hawaii
Honolulu

Illinois
Chicago
Morton
Park Ridge
Rock Island

Indiana
Indianapolis
South Bend

Kansas
Overland Park
Wichita

Kentucky
Louisville

Louisiana
Baton Rouge
Metairie

Maryland
Rockville
Towson

Massachusetts
Boston
Burlington
Littleton
Lowell
Tewksbury
Worcester

Michigan
Grand Rapids
Okemos
Southfield

Minnesota
Eden Prairie

Missouri
Creve Coeur

Nebraska
Omaha

Nevada
Reno

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New York City
Rochester
Syracuse

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Charlotte
Greensboro
Raleigh

Ohio
Cincinnati
Columbus
Middleburg Heights
Toledo

Oklahoma
Oklahoma City
Tulsa

Oregon
Beaverton
Eugene

Pennsylvania
Allentown
Camp Hill
Erie
Philadelphia
Pittsburgh
Wayne

Rhode Island
Cranston

South Carolina
Charleston
Columbia

Tennessee
Chattanooga
Knoxville
Memphis
Nashville

Texas
Austin
Dallas
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Wang do Brasil Computadores Ltda.
Rio de Janeiro
Sao Paulo

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Taipei, Taiwan

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Hong Kong

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Tokyo

Netherlands
Wang Nederland B.V.
Ijsselstein

New Zealand
Wang Computer Ltd.
Grey Lynn, Auckland

Panama
Wang de Panama (CPEC) S.A.
Panama

Republic of Singapore
Wang Computer Pte., Ltd.
Singapore

Republic of South Africa
Wang Computers (South Africa) (Pty.) Ltd.
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Durban
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Bern
Pully

West Germany
Wang Laboratories GmbH
Berlin
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Fellbach
Frankfurt/M.
Freiburg/Brsg.
Hamburg
Hannover
Kassel
Munich
Nuernberg
Stuttgart

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Dominican Republic
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Finland
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Iceland
India
Indonesia
Iran
Ireland
Israel
Italy
Jamaica
Japan
Jordan
Kenya
Korea
Lebanon
Liberia
Malaysia
Mexico
Morocco
Nicaragua
Nigeria
Norway
Pakistan
Peru
Philippines
Portugal
Saudi Arabia
Spain
Sri Lanka
Syria
Thailand
Tunisia
Turkey
United Arab Emirates
Venezuela
Yugoslavia

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